

# HD74LS374 ● Octal D-type Edge-triggered Flip-Flops (with three-state outputs)

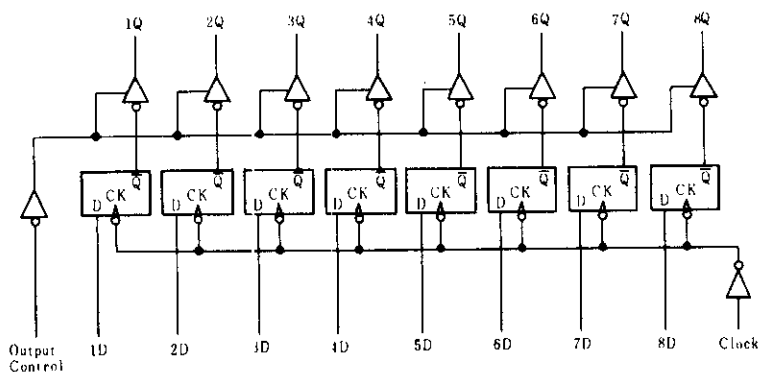
The HD74LS374, 8-bit registers features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The eight flip-flops are edge-triggered D-type flip-flops. On the positive transition the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

## ■FUNCTION TABLE

Inputs			Output
Output control	Clock	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
H	X	X	Z

Notes: H = high level, L = low level,  
X = irrelevant  
↑ = transition from low to high level  
 $Q_0$  = level of Q before the indicated steady-state input conditions were established  
Z = off (high-impedance) state of a three-state output

## ■BLOCK DIAGRAM

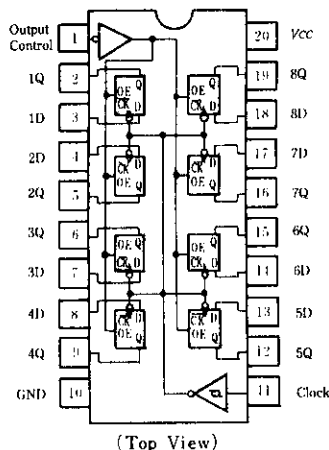


## ■RECOMMENDED OPERATING CONDITION

Item	Symbol	min	typ	max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.26	V
Output voltage	$V_{OH}$	—	—	5.5	V
Output current	$I_{OH}$	—	—	-2.6	mA
	$I_{OL}$	—	—	24	mA
Clock pulse width	$t_w$	15	—	—	ns
		15	—	—	
Data setup time	$t_{su}$	20 ↑	—	—	ns
Data hold time	$t_h$	3 ↑	—	—	ns

Note) ↑ : The arrow indicates the rising edge of clock pulse.

## ■PIN ARRANGEMENT



## ■ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	$V_{IH}$		2.0	—	—	V
	$V_{IL}$		—	—	0.8	V
Output voltage	$V_{OH}$	$V_{CC}=4.75\text{V}$ , $V_{IH}=2\text{V}$ , $V_{IL}=0.8\text{V}$ , $I_{OH}=-2.6\text{mA}$	2.4	—	—	V
	$V_{OL}$	$V_{CC}=4.75\text{V}$ , $V_{IH}=2\text{V}$ , $V_{IL}=0.8\text{V}$	$I_{OL}=12\text{mA}$	—	0.4	V
			$I_{OL}=24\text{mA}$	—	0.5	
	$I_{OZH}$	$V_{CC}=5.25\text{V}$ , $V_{IH}=2\text{V}$	$V_O=2.7\text{V}$	—	20	$\mu\text{A}$
	$I_{OZL}$		$V_O=0.4\text{V}$	—	-20	
Input current	$I_{IH}$	$V_{CC}=5.25\text{V}$ , $V_i=2.7\text{V}$	—	—	20	$\mu\text{A}$
	$I_{IL}$	$V_{CC}=5.25\text{V}$ , $V_i=0.4\text{V}$	—	—	-0.4	mA
	$I_i$	$V_{CC}=5.25\text{V}$ , $V_i=7\text{V}$	—	—	0.1	mA
Short-circuit output current	$I_{OS}$	$V_{CC}=5.25\text{V}$	-30	—	-130	mA
Supply current	$I_{CC}$	$V_{CC}=5.25\text{V}$ , $V_i=4.5\text{V}$ (Output control)	—	27	40	mA
Input clamp voltage	$V_{IK}$	$V_{CC}=4.75\text{V}$ , $I_{IK}=-18\text{mA}$	—	—	-1.5	V

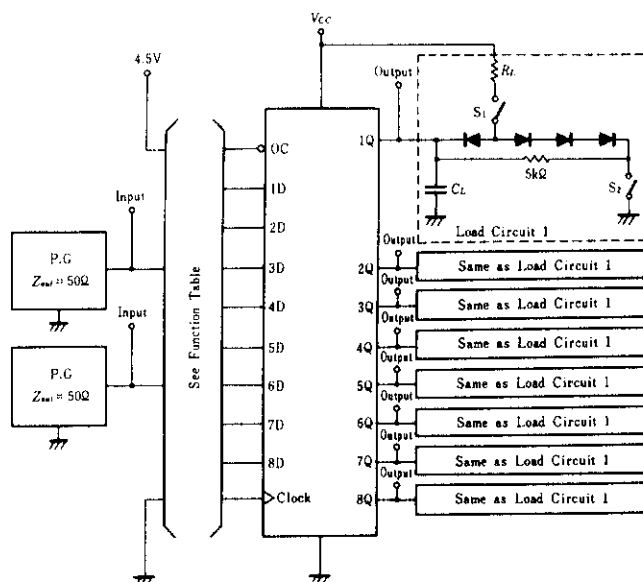
\*  $V_{CC}=5\text{V}$ ,  $T_a=25^\circ\text{C}$

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5\text{V}$ , $T_a=25^\circ\text{C}$ )

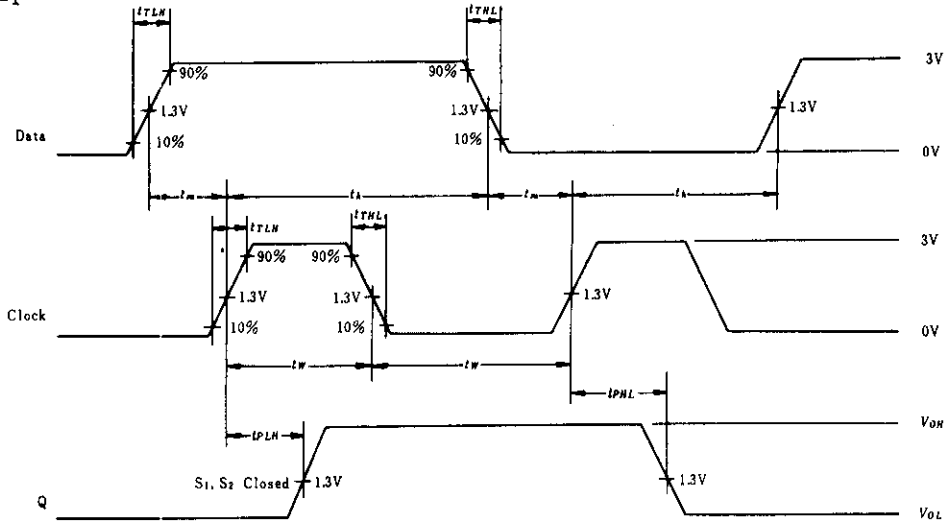
Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	$f_{max}$	Clock	Q	$C_L=45\text{pF}$ $R_L=667\Omega$	35	50	—	MHz
Propagation delay time	$t_{PLH}$	Clock	Q		—	15	28	ns
	$t_{PHL}$				—	19	28	
Output enable time	$t_{ZH}$	OC	Q		—	20	28	
	$t_{ZL}$				—	21	28	
Output disable time	$t_{HZ}$	OC	Q	$C_L=5\text{pF}$ $R_L=667\Omega$	—	12	20	
	$t_{LZ}$			—	14	25		

## ■TESTING METHOD

### Test Circuit

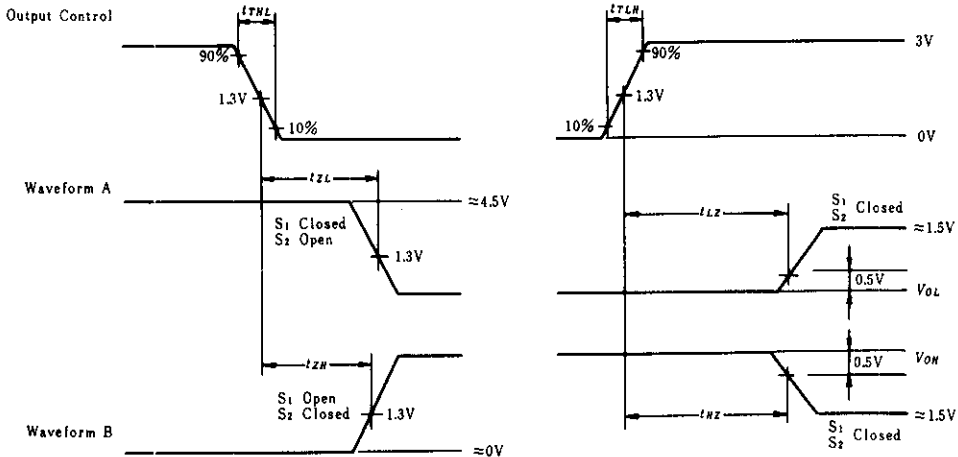


Waveform-1



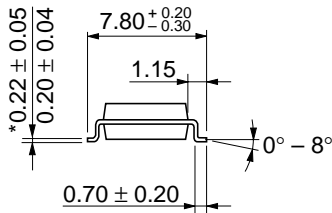
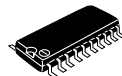
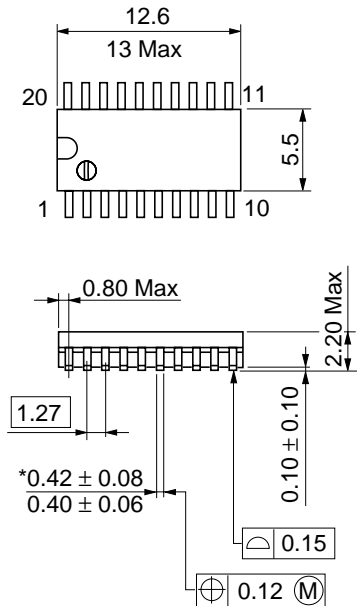
- Notes:
1. Input pulse;  $t_{TLH} = 15\text{ns}$ ,  $t_{THL} = 6\text{ns}$   
 Clock input;  $PRR = 1\text{MHz}$ , duty cycle 50%  
 Data input;  $PRR = 500\text{kHz}$ , duty cycle 50%  
 2.  $f_{max}$ ;  $t_{TLH} = 2.5\text{ns}$ ,  $t_{THL} = 2.5\text{ns}$

Waveform-2



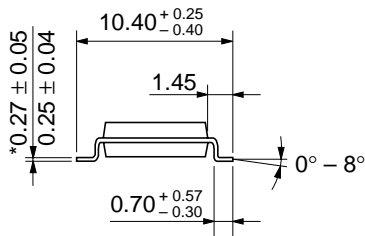
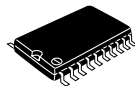
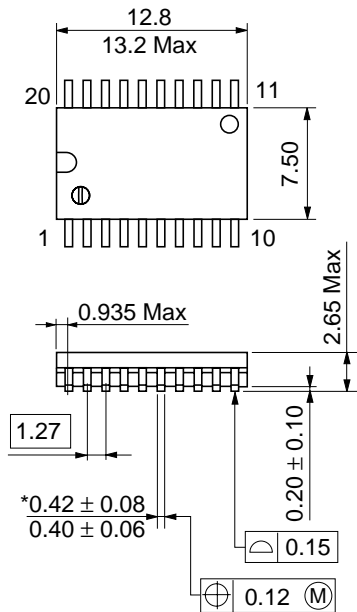
- Notes:
1. Input pulse;  $t_{TLH} = 15\text{ns}$ ,  $t_{THL} = 6\text{ns}$ ,  $PRR = 1\text{MHz}$ , duty cycle 50%
  2. Waveform A is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.





\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g



Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

\*Dimension including the plating thickness  
Base material dimension

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