

# HD74LS74A • Dual D-type Positive Edge-triggered Flip-Flops (with Preset and Clear)

## FUNCTION TABLE

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	$Q_0$	$\bar{Q}_0$

Notes) H; high level, L; low level, X; irrelevant

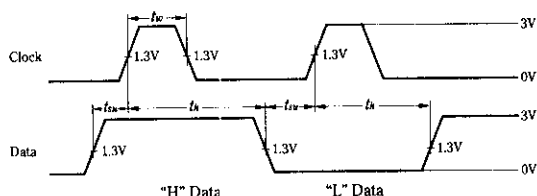
↑; transition from low to high level

$Q_0$ ; level of Q before the indicated steady-state conditions were established.

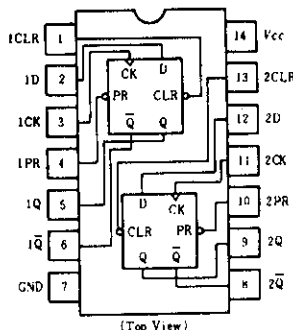
$\bar{Q}_0$ ; complement of  $Q_0$  or level of  $\bar{Q}$  before the indicated steady-state input conditions were established.

\*; This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

## TIMING DEFINITION



## PIN ARRANGEMENT



## RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	$f_{clock}$	0	—	25	MHz
Pulse width	Clock High	25	—	—	ns
	Clear/Preset	25	—	—	ns
Setup time	"H" Data	20↑	—	—	ns
	"L" Data	20↑	—	—	ns
Hold time	$t_h$	5↑	—	—	ns

Note) ↑; The arrow indicates the rising edge.

## ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item		Symbol	Test Conditions	min	typ*	max	Unit
Input voltage		$V_{IH}$		2.0	—	—	V
		$V_{IL}$		—	—	0.8	V
Output voltage		$V_{OH}$	$V_{CC}=4.75\text{V}$ , $V_{IH}=2\text{V}$ , $V_{IL}=0.8\text{V}$ , $I_{OH}=-400\mu\text{A}$	2.7	—	—	V
		$V_{OL}$	$V_{CC}=4.75\text{V}$ , $V_{IL}=0.8\text{V}$ , $V_{IH}=2\text{V}$	$I_{OL}=8\text{mA}$ $I_{OL}=4\text{mA}$	—	—	0.5 0.4
Input current	D	$I_{IH}$	$V_{CC}=5.25\text{V}$ , $V_I=2.7\text{V}$	—	—	20	$\mu\text{A}$
	Clear			—	—	40	
	Preset			—	—	40	
	Clock			—	—	20	
	D	$I_{IL}$	$V_{CC}=5.25\text{V}$ , $V_I=0.4\text{V}$	—	—	-0.4	mA
	Clear			—	—	-0.8	
	Preset			—	—	-0.8	
	Clock			—	—	-0.4	
	D	$I_I$	$V_{CC}=5.25\text{V}$ , $V_I=7\text{V}$	—	—	0.1	mA
	Clear			—	—	0.2	
	Preset			—	—	0.2	
	Clock			—	—	0.1	
Short-circuit output current		$I_{OS}$	$V_{CC}=5.25\text{V}$	-20	—	-100	mA
Supply current		$I_{CC}^{**}$	$V_{CC}=5.25\text{V}$	—	4	8	mA
Input clamp voltage		$V_{IK}$	$V_{CC}=4.75\text{V}$ , $I_{IN}=-18\text{mA}$	—	—	-1.5	V

\*  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$

\*\* With all outputs open,  $I_{CC}$  is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

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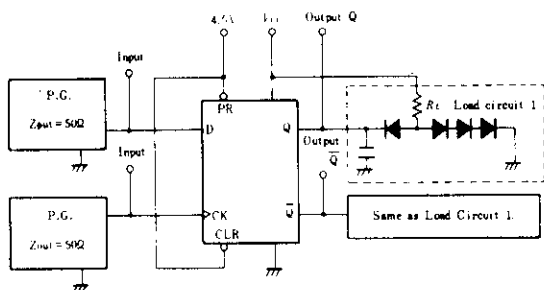
## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$ , $T_a=25^\circ C$ )

Item	Symbol	Inputs	Outputs	Test Condition	min	typ	max	Unit
Maximum clock frequency	$f_{max}$			$C_L=15pF$ , $R_L=2k\Omega$	25	33	—	MHz
Propagation delay time	$t_{PLH}$	Clock, Clear or Preset	Q, $\bar{Q}$	$C_L=15pF$ , $R_L=2k\Omega$	—	13	25	ns
	$t_{PHL}$				—	25	40	ns

## ■TESTING METHOD

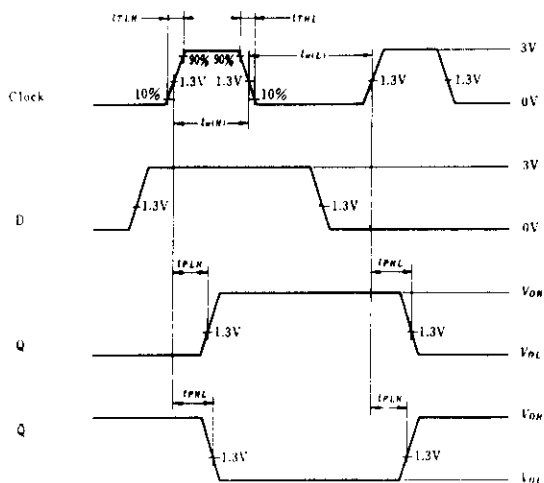
### 1) Test Circuit

#### 1.1) $f_{max}$ , $t_{PLH}$ , $t_{PHL}$ (Clock→Q, $\bar{Q}$ )



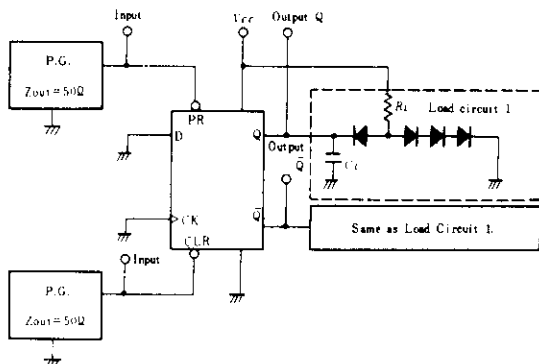
- Notes) 1. Test is put into the each flip-flop  
2. All diodes are 1S2074  $\oplus$ .  
3.  $C_L$  includes probe and jig capacitance.

### Waveform



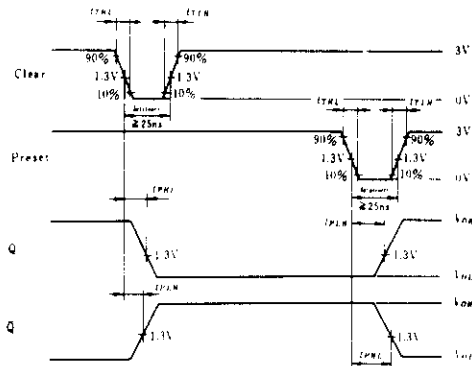
Note) Clock input pulse;  $t_{TLH} \leq 15ns$ ,  
 $t_{THL} \leq 6ns$ ,  $PRR=1MHz$ , duty  
cycle=50% and: for  $f_{max}$ ,  
 $t_{TLH} = t_{THL} \leq 2.5ns$ .

#### 1.2) $t_{PHL}$ , $t_{PLH}$ (Clear or Preset→Q, $\bar{Q}$ )

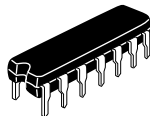
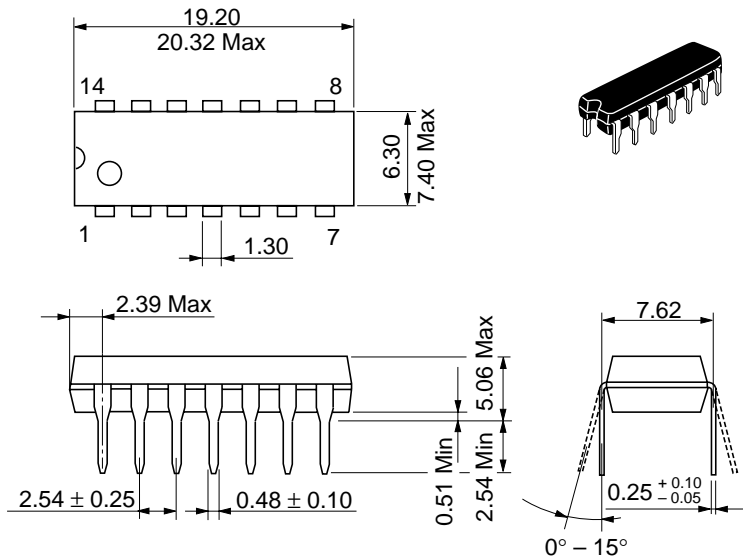


- Notes) 1. Test is put into the each flip-flop  
2. All diodes are 1S2074  $\oplus$ .  
3.  $C_L$  includes probe and jig capacitance.

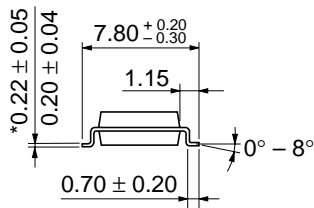
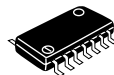
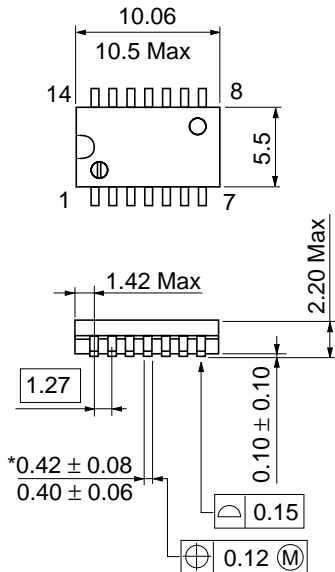
### Waveform



Note) Clear and preset input pulse;  
 $t_{TLH} \leq 15ns$ ,  $t_{THL} \leq 6ns$ ,  
 $PRR=1MHz$

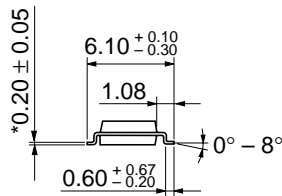
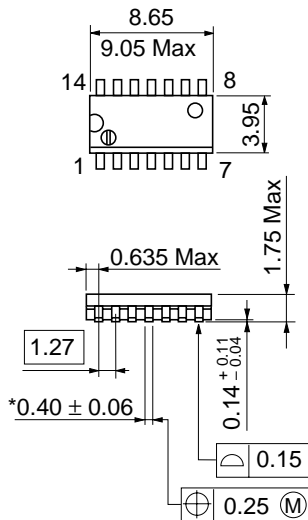


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

\*Dimension including the plating thickness  
Base material dimension



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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