

## 256K (32K x 8-bit) UV and OTP EPROM

### DESCRIPTION

The Hitachi HN27C256A is a 256-Kilobit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 32,768 x 8-bits.

The HN27C256A features fast address access times and low power dissipation. This combination makes the HN27C256A suitable for high speed microcomputer systems. The HN27C256A also offers high speed programming.

Hitachi's HN27C256A is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 28-pin Ceramic and Plastic DIP and 28-lead Plastic SOP packages.

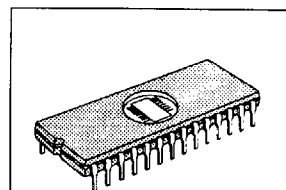
The Ceramic DIP package is erasable by exposure to Ultraviolet light. The Plastic DIP and SOP packaged devices are One-Time Programmable and once programmed, can not be rewritten.

### FEATURES

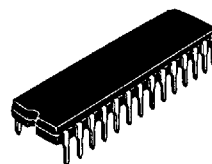
- Fast Access Times:
  - 100 ns/120ns/150 ns (max)
- Single Power Supply:
  - $V_{CC} = 5\text{ V} \pm 10\%$
- Low Power Dissipation:
  - Active Mode: 25 mW/MHz (typ)
  - Standby Mode: 5  $\mu$ W (typ)
- High Speed Programming
- Programming Power Supply:
  - $V_{PP} = 12.5\text{ V} \pm 0.5\text{ V}$
- Pin Arrangement:
  - JEDEC Standard Byte-Wide EPROM
- Packages:
  - 28-pin Ceramic DIP
  - 28-pin Plastic DIP
  - 28-lead Plastic SOP

### ORDERING INFORMATION

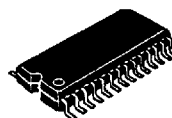
Type No.	Access Time	Package
HN27C256AG-10	100 ns	28-pin Ceramic DIP
HN27C256AG-12	120 ns	(DG-28)
HN27C256AP-12	120 ns	28-pin Plastic DIP
HN27C256AP-15	150 ns	(DP-28)
HN27C256AFP-12T	120 ns	28-lead Plastic SOP
HN27C256AFP-15T	150 ns	(FP-28DA)



(DG-28)



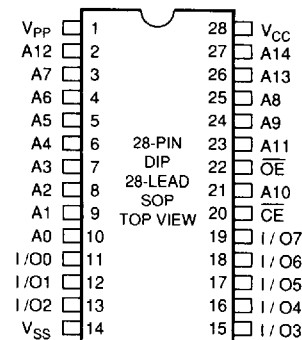
(DP-28)



(FP-28DA)

### PIN ARRANGEMENT

HN27C256AG/P Series  
HN27C256AFP Series

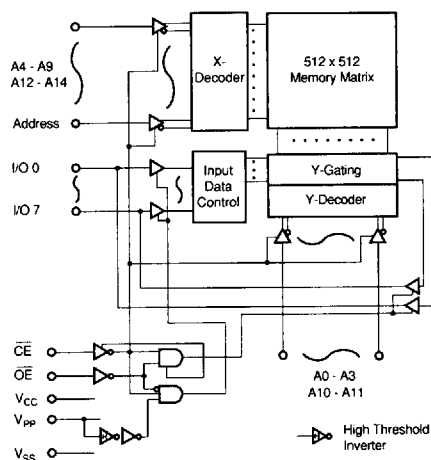


(PinD28 HN27C256A)

## PIN DESCRIPTION

Pin Name	Function
$A_0 - A_{14}$	Address
$I/O_0 - I/O_7$	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$V_{CC}$	Power Supply
$V_{PP}$	Programming Supply
$V_{SS}$	Ground

## BLOCK DIAGRAM



(BD.HN27C256H)

## MODE SELECTION

Mode	$V_{PP}$	$V_{CC}$	$\overline{CE}$	$\overline{OE}$	$A_9$	I/O
Read	$V_{CC}$	$V_{CC}$	$V_{IL}$	$V_{IL}$	X <sup>1</sup>	$D_{OUT}$
Output Disable	$V_{CC}$	$V_{CC}$	$V_{IL}$	$V_{IH}$	X	High-Z
Standby	$V_{CC}$	$V_{CC}$	$V_{IH}$	X	X	High-Z
Program	$V_{PP}$	$V_{CC}$	$V_{IL}$	$V_{IH}$	X	$D_{IN}$
Program Verify	$V_{PP}$	$V_{CC}$	$V_{IH}$	$V_{IL}$	X	$D_{OUT}$
Optional Verify	$V_{PP}$	$V_{CC}$	$V_{IL}$	$V_{IL}$	X	$D_{OUT}$
Program Inhibit	$V_{PP}$	$V_{CC}$	$V_{IH}$	$V_{IH}$	X	High-Z
Identifier	$V_{CC}$	$V_{CC}$	$V_{IL}$	$V_{IL}$	$V_H^2$	ID

- Notes: 1. X = Don't Care.  
2.  $11.5\text{ V} \leq V_H \leq 12.5\text{ V}$

**■ ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Value	Unit
Supply Voltage <sup>1</sup>	V <sub>CC</sub>	-0.6 to +7.0	V
Programming Voltage <sup>1</sup>	V <sub>PP</sub>	-0.6 to +13.5	V
All Input and Output Voltage <sup>1,2</sup>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.6 to +7.0	V
A <sub>9</sub> Input Voltage <sup>2</sup>	V <sub>ID</sub>	-0.6 to +13.5	V
Operating Temperature Range	T <sub>OPR</sub>	0 to +70	°C
Storage Temperature Range	T <sub>STG</sub>	-65 to +125 <sup>3</sup> -55 to +125 <sup>4</sup>	°C
Storage Temperature Under Bias	T <sub>BIAS</sub>	-10 to +80	°C

- Notes: 1. Relative to V<sub>SS</sub>.  
 2. V<sub>IN</sub>, V<sub>OUT</sub>, and V<sub>ID</sub> min = -1.0V for pulse width ≤ 50 ns.  
 3. HN27C256AG.  
 4. HN27C256AP and HN27C256AFP.

**■ CAPACITANCE (T<sub>a</sub> = 25°C, f = 1MHz)**

Item	Symbol	Typ.	Max.	Unit	Test Condition
Input Capacitance	C <sub>IN</sub>	4	8	pF	V <sub>IN</sub> = 0V
Output Capacitance	C <sub>OUT</sub>	8	12	pF	V <sub>OUT</sub> = 0V

**■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION**

(V<sub>CC</sub> = 5V ± 10%, V<sub>PP</sub> = V<sub>SS</sub> to V<sub>CC</sub>, T<sub>a</sub> = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I <sub>LI</sub>	-	-	2	μA	V <sub>IN</sub> = 0 V to V <sub>CC</sub>
Output Leakage Current	I <sub>LO</sub>	-	-	2	μA	V <sub>OUT</sub> = 0 V to V <sub>CC</sub>
Operating V <sub>CC</sub> Current	I <sub>CC1</sub>	-	-	30	mA	I <sub>OUT</sub> = 0 mA, $\overline{CE} = V_{IL}$
	I <sub>CC2</sub>	-	-	30	mA	I <sub>OUT</sub> = 0 mA, f = 10 MHz
	I <sub>CC3</sub>	-	5	15	mA	I <sub>OUT</sub> = 0 mA, f = 1 MHz
Standby V <sub>CC</sub> Current	I <sub>SB</sub>	-	-	1	mA	$\overline{CE} = V_{IH}$
V <sub>PP</sub> Current	I <sub>PP1</sub>	-	1	20	μA	V <sub>PP</sub> = 5.5 V
Input Voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> + 1 <sup>2</sup>	V	
	V <sub>IL</sub>	-0.3 <sup>1</sup>	-	0.8	V	
Output Voltage	V <sub>OH</sub>	2.4	-	-	V	I <sub>OH</sub> = 1.0 mA
	V <sub>OL</sub>	-	-	0.45	V	I <sub>OL</sub> = 2.1 mA

- Notes: 1. V<sub>IL</sub> min = -1.0 V for pulse width ≤ 50 ns.  
 2. V<sub>IH</sub> max = V<sub>CC</sub> + 1.5 V for pulse width ≤ 20 ns.  
 If V<sub>IH</sub> is over the specified maximum value, Read operation can not be guaranteed.

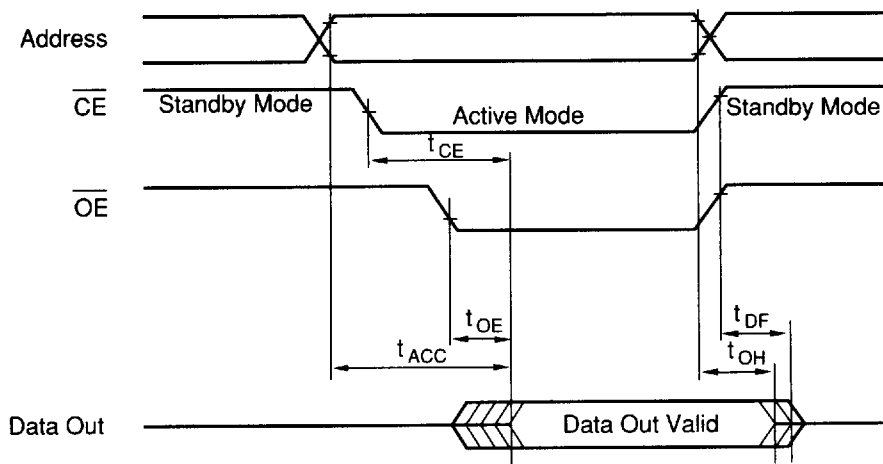
**4**

**■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION**
 $(V_{CC} = 5V \pm 10\%, V_{PP} = V_{CC}, T_a = 0 \text{ to } 70^\circ\text{C})$ 
**Test Conditions**

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times:  $\leq 10 \text{ ns}$
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V / 2.0 V

Item	Symbol	-10		-12		-15		Unit	Test Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
Address Access Time	$t_{ACC}$	-	100	-	120	-	150	ns	$\overline{CE} = \overline{OE} = V_{IL}$
Chip Enable Access Time	$t_{CE}$	-	100	-	120	-	150	ns	$\overline{OE} = V_{IL}$
Output Enable Access Time	$t_{OE}$	-	60	-	60	-	70	ns	$\overline{CE} = V_{IL}$
Output Disable to High-Z <sup>1</sup>	$t_{DF}$	0	35	0	40	0	50	ns	$\overline{CE} = V_{IL}$
Output Hold to Address Change	$t_{OH}$	5	-	5	-	5	-	ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note: 1.  $t_{DF}$  is defined as the time at which the output becomes an open circuit and data is no longer driven.

**■ READ TIMING WAVEFORM**


(TD.R.HN27C256A)

**■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS**
 $(V_{CC} = 6.0\text{ V} \pm 0.25\text{ V}, V_{PP} = 12.5\text{ V} \pm 0.5\text{ V}, T_a = 25^\circ\text{C} \pm 5^\circ\text{C})$ 

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	$I_{LI}$	-	-	2	$\mu\text{A}$	$V_{IN} = 0\text{ V to } V_{CC}$
Operating $V_{CC}$ Current	$I_{CC}$	-	-	30	$\text{mA}$	
Operating $V_{PP}$ Current	$I_{PP}$	-	-	30	$\text{mA}$	$\overline{CE} = V_{IL}$
Input Voltage <sup>3</sup>	$V_{IH}$	2.2	-	$V_{CC} + .5$ <sup>6</sup>	$\text{V}$	
	$V_{IL}$	- 0.1 <sup>5</sup>	-	0.8	$\text{V}$	
Output Voltage	$V_{OH}$	2.4	-	-	$\text{V}$	$I_{OH} = -400\text{ }\mu\text{A}$
	$V_{OL}$	-	-	0.45	$\text{V}$	$I_{OH} = 2.1\text{ mA}$

- Notes:
- $V_{CC}$  must be applied before  $V_{PP}$  and removed after  $V_{PP}$ .
  - $V_{PP}$  must not exceed 13 V, including overshoot.
  - Device reliability may be adversely affected if the device is installed or removed while  $V_{PP} = 12.5\text{ V}$ .
  - Do not change  $V_{PP}$  from  $V_{IL}$  to 12.5 V or 12.5 V to  $V_{IL}$  when  $\overline{CE} = \text{low}$ .
  - $V_{IL}$  min = -0.6 V for pulse width  $\leq 20\text{ ns}$ .
  - If  $V_{IH}$  is over the specified maximum value, programming operation can not be guaranteed.

**■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS**
 $(V_{CC} = 6.0\text{ V} \pm 0.25\text{ V}, V_{PP} = 12.5\text{ V} \pm 0.5\text{ V}, T_a = 25^\circ\text{C} \pm 5^\circ\text{C})$ 
**Test Conditions**

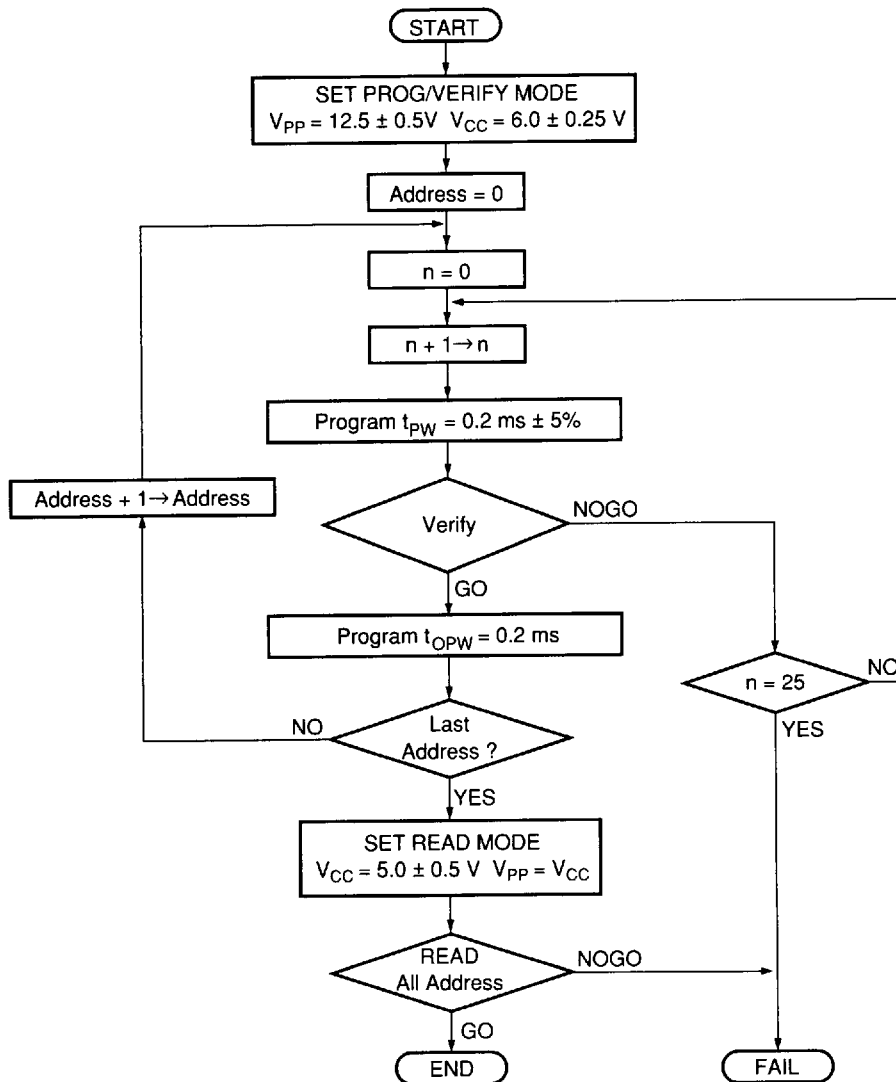
- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times:  $\leq 20\text{ ns}$
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	$t_{AS}$	2	-	-	$\mu\text{s}$	
Address Hold Time	$t_{AH}$	0	-	-	$\mu\text{s}$	
Data Setup Time	$t_{DS}$	2	-	-	$\mu\text{s}$	
$V_{PP}$ Setup Time	$t_{VPS}$	2	-	-	$\mu\text{s}$	
$V_{CC}$ Setup Time	$t_{VCS}$	2	-	-	$\mu\text{s}$	
Output Enable Setup Time	$t_{OES}$	2	-	-	$\mu\text{s}$	
Output Disable Time	$t_{DF}$	0	-	130	$\text{ns}$	
$\overline{CE}$ Initial Programming Pulse Width	$t_{PW}$	0.95	1.0	1.05	$\text{ms}$	
$\overline{CE}$ Overprogramming Pulse Width	$t_{OPW}$	2.85	-	78.75	$\text{ms}$	
Data Valid from Output Enable Time	$t_{OE}$	0	-	150	$\text{ns}$	

- Note:
- $t_{DF}$  is defined as the time at which the output becomes an open circuit and data is no longer driven.

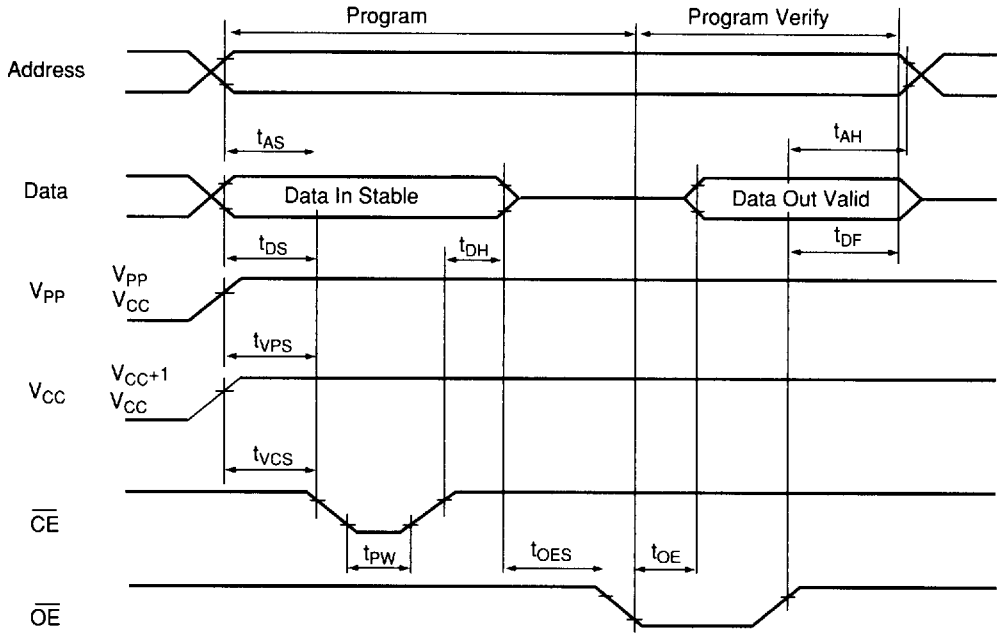
**FAST HIGH-RELIABILITY PROGRAMMING FLOWCHART**

The Hitachi HN27C256A can be programmed with the Fast High-Reliability Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data. This algorithm theoretically provides one-tenth the programming time of the conventional High Performance Programming algorithm.



(FC.P.HN27C256A)

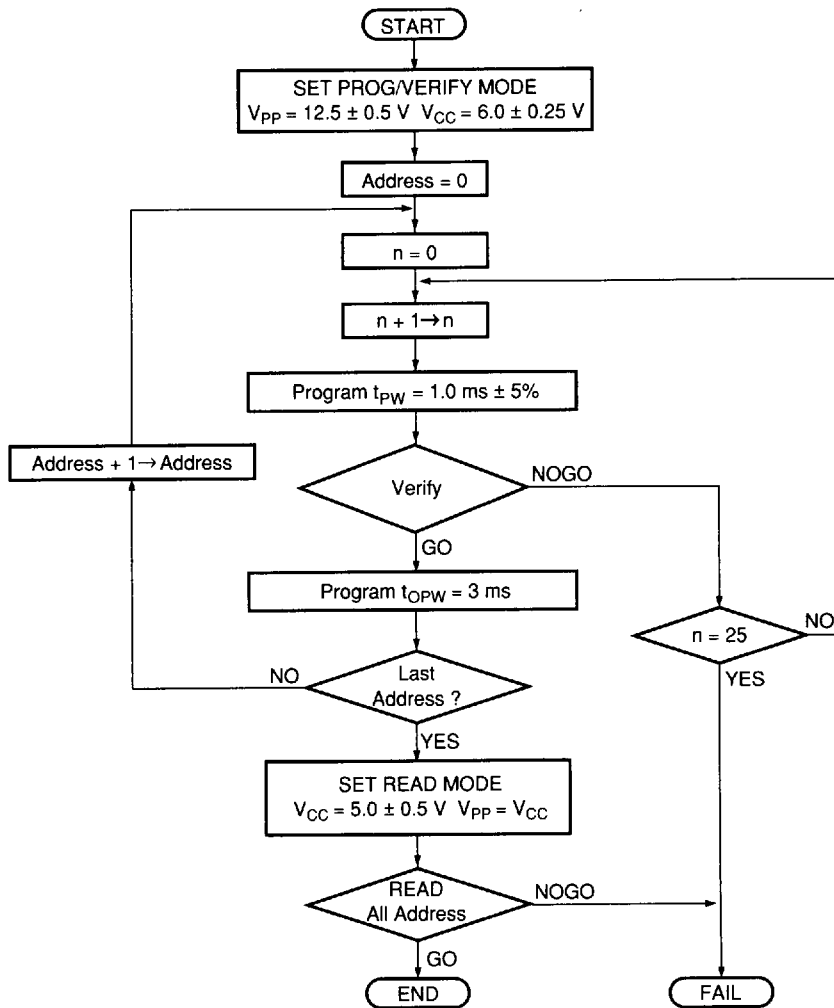
■ FAST HIGH-RELIABILITY PROGRAMMING TIMING WAVEFORM



(TD.P.HN27C256A)

**■ HIGH PERFORMANCE PROGRAMMING FLOWCHART**

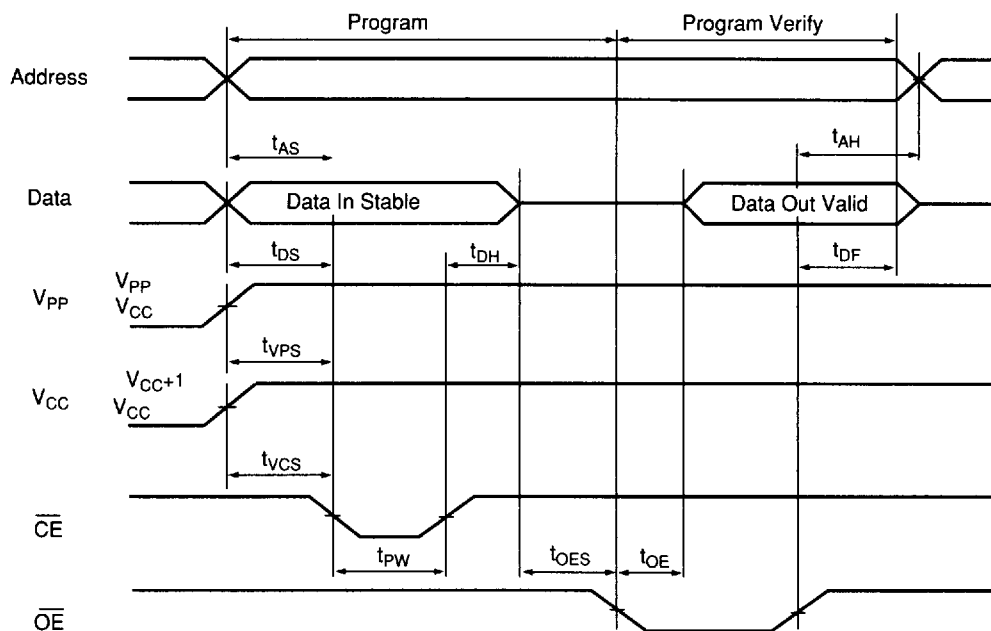
The Hitachi HN27C256A can be programmed with the High Performance Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.PP.HN27C256A)



## ■ HIGH PERFORMANCE PROGRAMMING TIMING WAVEFORM



(TD.PP.HN27C256A)

## ■ ERASING THE HN27C256A

The Hitachi HN27C256A Ceramic DIP package allow the device to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm<sup>2</sup>.

## ■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

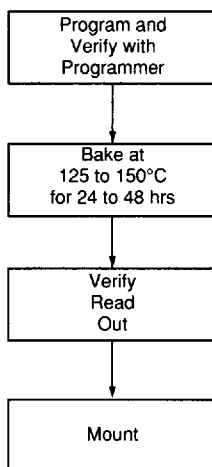
## ■ HN27C256A SERIES IDENTIFIER CODE

Identifier	A <sub>0</sub>	I/O <sub>7</sub>	I/O <sub>6</sub>	I/O <sub>5</sub>	I/O <sub>4</sub>	I/O <sub>3</sub>	I/O <sub>2</sub>	I/O <sub>1</sub>	I/O <sub>0</sub>	Hex Data
Manufacturer Code	V <sub>IL</sub>	0	0	0	0	0	1	1	1	07
Device Code	V <sub>IH</sub>	0	0	1	1	0	0	0	1	31

- Notes: 1. A<sub>9</sub> = 12.0 V ± 0.5V  
 3. A<sub>1</sub>-A<sub>8</sub>, A<sub>10</sub>-A<sub>14</sub>,  $\overline{CE}$ ,  $\overline{OE}$  = V<sub>IL</sub>

## ■ HN27C256AP/FP RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27C256A plastic packages, please make the following screening (baking without bias) shown below:



(RSC.EPROM)