# IC41C16105S
# IC41LV16105S

## 1M x 16 (16-MBIT) DYNAMIC RAM WITH FAST PAGE MODE

### FEATURES

- TTL compatible inputs and outputs; tristate I/O
- Refresh Interval: 1,024 cycles/16 ms,
  1,024 cycles / 128ms Self Refresh
- Refresh Mode: $\overline{RAS}$-Only, $\overline{CAS}$-before-$\overline{RAS}$ (CBR), Hidden, and Self Refresh
- JEDEC standard pinout
- Single power supply:
  5V ± 10% (IC41C16105S)
  3.3V ± 10% (IC41LV16105S)
- Byte Write and Byte Read operation via two $\overline{CAS}$
- Industrail temperature range -40°C to 85°C

### DESCRIPTION

The *ICSI* IC41C16105S and IC41LV16105S are 1,048,576 x 16-bit high-performance CMOS Dynamic Random Access Memories. Fast Page Mode allows 1,024 random accesses within a single row with access cycle time as short as 20 ns per 16-bit word. The Byte Write control, of upper and lower byte, makes the IC41C16105S ideal for use in 16-, 32-bit wide data bus systems.

These features make the IC41C16105S and IC41LV16105S ideally suited for high-bandwidth graphics, digital signal processing, high-performance computing systems, and peripheral applications.

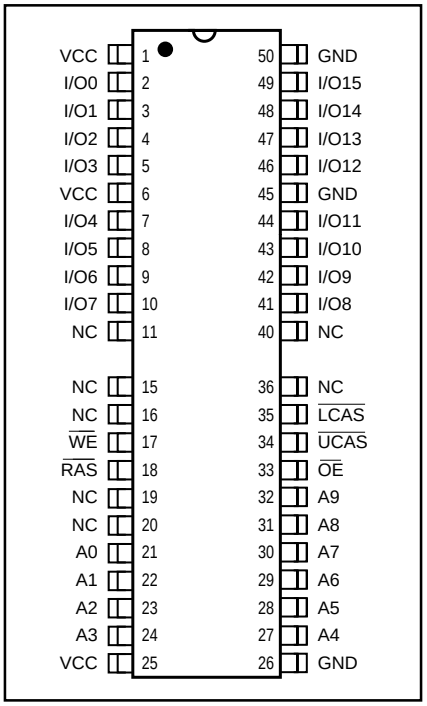
The IC41C16105S and IC41LV16105S are packaged in a 42-pin 400mil SOJ and 400mil 44- (50-) pin TSOP-2.

### KEY TIMING PARAMETERS

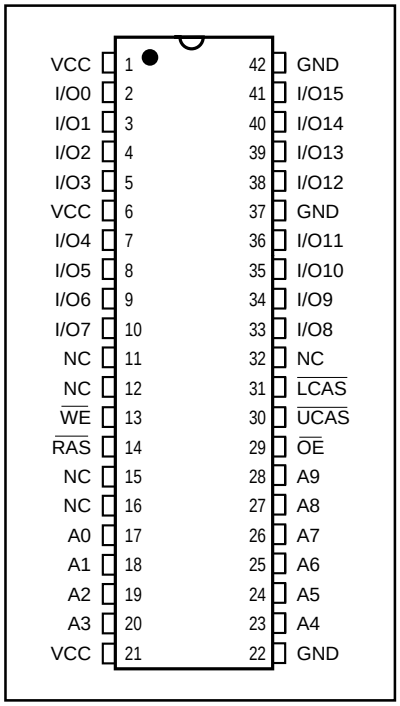
| Parameter | -50 | -60 | Unit |
|---|---|---|---|
| Max. $\overline{RAS}$ Access Time ($t_{RAC}$) | 50 | 60 | ns |
| Max. $\overline{CAS}$ Access Time ($t_{CAC}$) | 13 | 15 | ns |
| Max. Column Address Access Time ($t_{AA}$) | 25 | 30 | ns |
| Min. Fast Page Mode Cycle Time ($t_{PC}$) | 20 | 25 | ns |
| Min. Read/Write Cycle Time ($t_{RC}$) | 84 | 104 | ns |

### PIN CONFIGURATIONS

44(50)-Pin TSOP-2



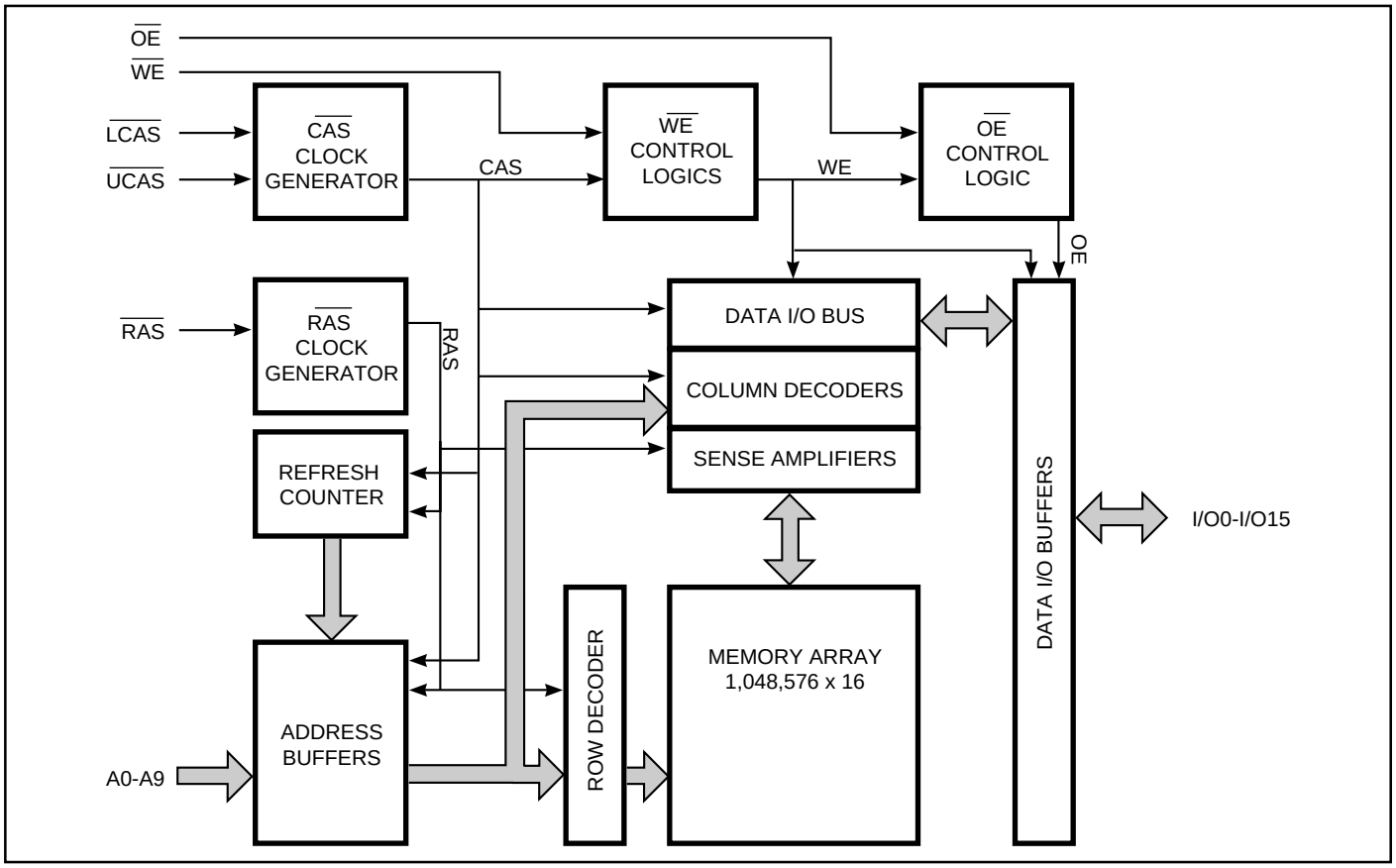

42-Pin SOJ




### PIN DESCRIPTIONS

| | |
|---|---|
| A0-A9 | Address Inputs |
| I/O0-15 | Data Inputs/Outputs |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{UCAS}$ | Upper Column Address Strobe |
| $\overline{LCAS}$ | Lower Column Address Strobe |
| Vcc | Power |
| GND | Ground |
| NC | No Connection |

## FUNCTIONAL BLOCK DIAGRAM



## TRUTH TABLE

| Function | | $\overline{RAS}$ | $\overline{LCAS}$ | $\overline{UCAS}$ | $\overline{WE}$ | $\overline{OE}$ | Address tR/tC | I/O |
|---|---|---|---|---|---|---|---|---|
| Standby | | H | H | H | X | X | X | High-Z |
| Read: Word | | L | L | L | H | L | ROW/COL | DOUT |
| Read: Lower Byte | | L | L | H | H | L | ROW/COL | Lower Byte, DOUT<br>Upper Byte, High-Z |
| Read: Upper Byte | | L | H | L | H | L | ROW/COL | Lower Byte, High-Z<br>Upper Byte, DOUT |
| Write: Word (Early Write) | | L | L | L | L | X | ROW/COL | DIN |
| Write: Lower Byte (Early Write) | | L | L | H | L | X | ROW/COL | Lower Byte, DIN<br>Upper Byte, High-Z |
| Write: Upper Byte (Early Write) | | L | H | L | L | X | ROW/COL | Lower Byte, High-Z<br>Upper Byte, DIN |
| Read-Write[1,2] | | L | L | L | H→L | L→H | ROW/COL | DOUT, DIN |
| Hidden Refresh | Read[2] | L→H→L | L | L | H | L | ROW/COL | DOUT |
| | Write[1,3] | L→H→L | L | L | L | X | ROW/COL | DOUT |
| $\overline{RAS}$-Only Refresh | | L | H | H | X | X | ROW/NA | High-Z |
| CBR Refresh[4] | | H→L | L | L | X | X | X | High-Z |

Notes:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{LCAS}$ or $\overline{UCAS}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{LCAS}$ or $\overline{UCAS}$ active).
3. EARLY WRITE only.
4. At least one of the two $\overline{CAS}$ signals must be active ($\overline{LCAS}$ or $\overline{UCAS}$).

## Functional Description

The IC41C16105S and IC41LV16105S is a CMOS DRAM optimized for high-speed bandwidth, low power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 10 address bits. These are entered ten bits (A0-A9) at a time. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address is latched by the Column Address Strobe ($\overline{CAS}$). $\overline{RAS}$ is used to latch the first ten bits and $\overline{CAS}$ is used the latter ten bits.

The ICS41C16105S and IC41LV16105S has two $\overline{CAS}$ controls, $\overline{LCAS}$ and $\overline{UCAS}$. The $\overline{LCAS}$ and $\overline{UCAS}$ inputs internally generates a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 1M x 16 DRAMs. The key difference is that each $\overline{CAS}$ controls its corresponding I/O tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$ and $\overline{RAS}$). $\overline{LCAS}$ controls I/O0 through I/O7 and $\overline{UCAS}$ controls I/O8 through I/O15.

The IC41C16105S and IC41LV16105S $\overline{CAS}$ function is determined by the first $\overline{CAS}$ ($\overline{LCAS}$ or $\overline{UCAS}$) transitioning LOW and the last transitioning back HIGH. The two $\overline{CAS}$ controls give the IS41C16105L and IS41LV16105L both BYTE READ and BYTE WRITE cycle capabilities.

## Memory Cycle

A memory cycle is initiated by bring $\overline{RAS}$ LOW and it is terminated by returning both $\overline{RAS}$ and $\overline{CAS}$ HIGH. To ensures proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum $t_{RAS}$ time has expired. A new cycle must not be initiated until the minimum precharge time $t_{RP}$, $t_{CP}$ has elapsed.

## Read Cycle

A read cycle is initiated by the falling edge of $\overline{CAS}$ or $\overline{OE}$, whichever occurs last, while holding $\overline{WE}$ HIGH. The column address must be held for a minimum time specified by $t_{AR}$. Data Out becomes valid only when $t_{RAC}$, $t_{AA}$, $t_{CAC}$ and $t_{OEA}$ are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

## Write Cycle

A write cycle is initiated by the falling edge of $\overline{CAS}$ and $\overline{WE}$, whichever occurs last. The input data must be valid at or before the falling edge of $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

## Refresh Cycle

To retain data, 1,024 refresh cycles are required in each 16 ms period. There are two ways to refresh the memory.

1. By clocking each of the 1,024 row addresses (A0 through A9) with $\overline{RAS}$ at least once every 16 ms. Any read, write, read-modify-write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated by the falling edge of $\overline{RAS}$, while holding $\overline{CAS}$ LOW. In $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, an internal 10-bit counter provides the row addresses and the external address inputs are ignored.

$\overline{CAS}$-before-$\overline{RAS}$ is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

## Self Refresh Cycle

The Self Refresh allows the user a dynamic refresh, data retention mode at the extended refresh period of 128 ms. i.e., 125 $\mu$s per row when using distributed CBR refreshes. The feature also allows the user the choice of a fully static, low power data retention mode. The optional Self Refresh feature is initiated by performing a CBR Refresh cycle and holding $\overline{RAS}$ LOW for the specified $t_{RAS}$.

The Self Refresh mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of $t_{RP}$. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting Self Refresh.

However, if the DRAM controller utilizes a $\overline{RAS}$-only or burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

## Power-On

After application of the $V_{CC}$ supply, an initial pause of 200 $\mu$s is required followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ signal).

During power-on, it is recommended that $\overline{RAS}$ track with $V_{CC}$ or be held at a valid $V_{IH}$ to avoid current surges.

## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Parameters | | Rating | Unit |
|---|---|---|---|---|
| $V_T$ | Voltage on Any Pin Relative to GND | 5V | –1.0 to +7.0 | V |
| | | 3.3V | –0.5 to +4.6 | |
| $V_{CC}$ | Supply Voltage | 5V | –1.0 to +7.0 | V |
| | | 3.3V | –0.5 to +4.6 | |
| $I_{OUT}$ | Output Current | | 50 | mA |
| $P_D$ | Power Dissipation | | 1 | W |
| $T_A$ | Commercial Operation Temperature | | 0 to +70 | °C |
| | Industrail Operation Temperature | | –40 to +85 | °C |
| $T_{STG}$ | Storage Temperature | | –55 to +125 | °C |

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

| Symbol | Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 5V | 4.5 | 5.0 | 5.5 | V |
| | | 3.3V | 3.0 | 3.3 | 3.6 | |
| $V_{IH}$ | Input High Voltage | 5V | 2.4 | — | $V_{CC}$ + 1.0 | V |
| | | 3.3V | 2.0 | — | $V_{CC}$ + 0.3 | |
| $V_{IL}$ | Input Low Voltage | 5V | –1.0 | — | 0.8 | V |
| | | 3.3V | –0.3 | — | 0.8 | |
| $T_A$ | Commercial Ambient Temperature | | 0 | — | 70 | °C |
| | Industrail Ambient Temperature | | –40 | — | 85 | °C |

## CAPACITANCE[1,2]

| Symbol | Parameter | Max. | Unit |
|---|---|---|---|
| $C_{IN1}$ | Input Capacitance: A0-A9 | 5 | pF |
| $C_{IN2}$ | Input Capacitance: $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$ | 7 | pF |
| $C_{IO}$ | Data Input/Output Capacitance: I/O0-I/O15 | 7 | pF |

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A$ = 25°C, f = 1 MHz,

## ELECTRICAL CHARACTERISTICS[1]

(Recommended Operating Conditions unless otherwise noted.)

| Symbol | Parameter | Test Condition | Speed | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Leakage Current | Any input 0V ≤ $V_{IN}$ ≤ Vcc<br>Other inputs not under test = 0V | | –5 | 5 | µA |
| $I_{IO}$ | Output Leakage Current | Output is disabled (Hi-Z)<br>0V ≤ $V_{OUT}$ ≤ Vcc | | –5 | 5 | µA |
| $V_{OH}$ | Output High Voltage Level | $I_{OH}$ = –5.0 mA (5V)<br>$I_{OH}$ = –2.0 mA (3.3V) | | 2.4 | — | V |
| $V_{OL}$ | Output Low Voltage Level | $I_{OL}$ = 4.2 mA (5V)<br>$I_{OL}$ = 2.0 mA (3.3V) | | — | 0.4 | V |
| $I_{CC1}$ | Standby Current: TTL | $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ ≥ $V_{IH}$ Commerical | 5V | — | 2 | mA |
| | | | 3.3V | — | 1 | |
| | | Extended & Idustrial | 5V | — | 3 | mA |
| | | | 3.3V | — | 2 | |
| $I_{CC2}$ | Standby Current: CMOS | $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ ≥ $V_{CC}$ – 0.2V | 5V | — | 1 | mA |
| | | | 3.3V | — | 0.5 | |
| $I_{CC3}$ | Operating Current:<br>Random Read/Write[2,3,4]<br>Average Power Supply Current | $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$,<br>Address Cycling, $t_{RC}$ = $t_{RC}$ (min.) | -50 | — | 160 | mA |
| | | | -60 | — | 145 | |
| $I_{CC4}$ | Operating Current:<br>Fast Page Mode[2,3,4]<br>Average Power Supply Current | $\overline{RAS}$ = $V_{IL}$, $\overline{LCAS}$, $\overline{UCAS}$,<br>Cycling $t_{PC}$ = $t_{PC}$ (min.) | -50 | — | 90 | mA |
| | | | -60 | — | 80 | |
| $I_{CC5}$ | Refresh Current:<br>$\overline{RAS}$-Only[2,3]<br>Average Power Supply Current | $\overline{RAS}$ Cycling, $\overline{LCAS}$, $\overline{UCAS}$ ≥ $V_{IH}$<br>$t_{RC}$ = $t_{RC}$ (min.) | -50 | — | 160 | mA |
| | | | -60 | — | 145 | |
| $I_{CC6}$ | Refresh Current:<br>CBR[2,3,5]<br>Average Power Supply Current | $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ Cycling<br>$t_{RC}$ = $t_{RC}$ (min.) | -50 | — | 160 | mA |
| | | | -60 | — | 145 | |
| $I_{CCS}$ | Self Refresh Current | Self Refresh mode | 5V | — | 650 | µA |
| | | | 3.3V | — | 300 | |

Notes:

1. An initial pause of 200 µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the $t_{REF}$ refresh requirement is exceeded.
2. Dependent on cycle rates.
3. Specified values are obtained with minimum cycle time and the output open.
4. Column-address is changed once each Fast page cycle.
5. Enables on-chip refresh and address counters.

## AC CHARACTERISTICS[1,2,3,4,5,6]

(Recommended Operating Conditions unless otherwise noted.)

| Symbol | Parameter | -50 Min. | -50 Max. | -60 Min. | -60 Max. | Units |
|---|---|---|---|---|---|---|
| tRC | Random READ or WRITE Cycle Time | 84 | — | 104 | — | ns |
| tRAC | Access Time from $\overline{RAS}$[6, 7] | — | 50 | — | 60 | ns |
| tCAC | Access Time from $\overline{CAS}$[6, 8, 15] | — | 13 | — | 15 | ns |
| tAA | Access Time from Column-Address[6] | — | 25 | — | 30 | ns |
| tRAS | $\overline{RAS}$ Pulse Width | 50 | 10K | 60 | 10K | ns |
| tRP | $\overline{RAS}$ Precharge Time | 30 | — | 40 | — | ns |
| tCAS | $\overline{CAS}$ Pulse Width[26] | 8 | 10K | 10 | 10K | ns |
| tCP | $\overline{CAS}$ Precharge Time[9, 25] | 9 | — | 9 | — | ns |
| tCSH | $\overline{CAS}$ Hold Time [21] | 38 | — | 40 | — | ns |
| tRCD | $\overline{RAS}$ to $\overline{CAS}$ Delay Time[10, 20] | 12 | 37 | 14 | 45 | ns |
| tASR | Row-Address Setup Time | 0 | — | 0 | — | ns |
| tRAH | Row-Address Hold Time | 8 | — | 10 | — | ns |
| tASC | Column-Address Setup Time[20] | 0 | — | 0 | — | ns |
| tCAH | Column-Address Hold Time[20] | 8 | — | 10 | — | ns |
| tAR | Column-Address Hold Time (referenced to $\overline{RAS}$) | 30 | — | 40 | — | ns |
| tRAD | $\overline{RAS}$ to Column-Address Delay Time[11] | 10 | 25 | 12 | 30 | ns |
| tRAL | Column-Address to $\overline{RAS}$ Lead Time | 25 | — | 30 | — | ns |
| tRPC | $\overline{RAS}$ to $\overline{CAS}$ Precharge Time | 5 | — | 5 | — | ns |
| tRSH | $\overline{RAS}$ Hold Time[27] | 8 | — | 10 | — | ns |
| tRHCP | $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge | 37 | — | 37 | — | ns |
| tCLZ | $\overline{CAS}$ to Output in Low-Z[15, 29] | 0 | — | 0 | — | ns |
| tCRP | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time[21] | 5 | — | 5 | — | ns |
| tOD | Output Disable Time[19, 28, 29] | 3 | 15 | 3 | 15 | ns |
| tOE | Output Enable Time[15, 16] | — | 13 | — | 15 | ns |
| tOED | Output Enable Data Delay (Write) | 20 | — | 20 | — | ns |
| tOEHC | $\overline{OE}$ HIGH Hold Time from $\overline{CAS}$ HIGH | 5 | — | 5 | — | ns |
| tOEP | $\overline{OE}$ HIGH Pulse Width | 10 | — | 10 | — | ns |
| tOES | $\overline{OE}$ LOW to $\overline{CAS}$ HIGH Setup Time | 5 | — | 5 | — | ns |
| tRCS | Read Command Setup Time[17, 20] | 0 | — | 0 | — | ns |
| tRRH | Read Command Hold Time (referenced to $\overline{RAS}$)[12] | 0 | — | 0 | — | ns |
| tRCH | Read Command Hold Time (referenced to $\overline{CAS}$)[12, 17, 21] | 0 | — | 0 | — | ns |
| tWCH | Write Command Hold Time[17, 27] | 8 | — | 10 | — | ns |
| tWCR | Write Command Hold Time (referenced to $\overline{RAS}$)[17] | 40 | — | 50 | — | ns |
| tWP | Write Command Pulse Width[17] | 8 | — | 10 | — | ns |
| tWPZ | $\overline{WE}$ Pulse Widths to Disable Outputs | 10 | — | 10 | — | ns |
| tRWL | Write Command to $\overline{RAS}$ Lead Time[17] | 13 | — | 15 | — | ns |
| tCWL | Write Command to $\overline{CAS}$ Lead Time[17, 21] | 8 | — | 10 | — | ns |
| tWCS | Write Command Setup Time[14, 17, 20] | 0 | — | 0 | — | ns |
| tDHR | Data-in Hold Time (referenced to $\overline{RAS}$) | 39 | — | 39 | — | ns |

## AC CHARACTERISTICS (Continued)[1,2,3,4,5,6]

(Recommended Operating Conditions unless otherwise noted.)

| Symbol | Parameter | -50 Min. | -50 Max. | -60 Min. | -60 Max. | Units |
|---|---|---|---|---|---|---|
| $t_{ACH}$ | Column-Address Setup Time to $\overline{CAS}$ Precharge during WRITE Cycle | 15 | — | 15 | — | ns |
| $t_{OEH}$ | $\overline{OE}$ Hold Time from $\overline{WE}$ during READ-MODIFY-WRITE cycle[18] | 8 | — | 10 | — | ns |
| $t_{DS}$ | Data-In Setup Time[15, 22] | 0 | — | 0 | — | ns |
| $t_{DH}$ | Data-In Hold Time[15, 22] | 8 | — | 10 | — | ns |
| $t_{RWC}$ | READ-MODIFY-WRITE Cycle Time | 108 | — | 133 | — | ns |
| $t_{RWD}$ | $\overline{RAS}$ to $\overline{WE}$ Delay Time during READ-MODIFY-WRITE Cycle[14] | 64 | — | 77 | — | ns |
| $t_{CWD}$ | $\overline{CAS}$ to $\overline{WE}$ Delay Time[14, 20] | 26 | — | 32 | — | ns |
| $t_{AWD}$ | Column-Address to $\overline{WE}$ Delay Time[14] | 39 | — | 47 | — | ns |
| $t_{PC}$ | Fast Page Mode READ or WRITE Cycle Time[24] | 20 | — | 25 | — | ns |
| $t_{RASP}$ | $\overline{RAS}$ Pulse Width | 50 | 100K | 60 | 100K | ns |
| $t_{CPA}$ | Access Time from $\overline{CAS}$ Precharge[15] | — | 30 | — | 35 | ns |
| $t_{PRWC}$ | READ-WRITE Cycle Time[24] | 56 | — | 68 | — | ns |
| $t_{COH}$ | Data Output Hold after $\overline{CAS}$ LOW | 5 | — | 5 | — | ns |
| $t_{OFF}$ | Output Buffer Turn-Off Delay from $\overline{CAS}$ or $\overline{RAS}$[13,15,19, 29] | 1.6 | 12 | 1.6 | 15 | ns |
| $t_{WHZ}$ | Output Disable Delay from $\overline{WE}$ | 3 | 10 | 3 | 10 | ns |
| $t_{CLCH}$ | Last $\overline{CAS}$ going LOW to First $\overline{CAS}$ returning HIGH[23] | 10 | — | 10 | — | ns |
| $t_{CSR}$ | $\overline{CAS}$ Setup Time (CBR REFRESH)[30, 20] | 5 | — | 5 | — | ns |
| $t_{CHR}$ | $\overline{CAS}$ Hold Time (CBR REFRESH)[30, 21] | 8 | — | 10 | — | ns |
| $t_{ORD}$ | $\overline{OE}$ Setup Time prior to $\overline{RAS}$ during HIDDEN REFRESH Cycle | 0 | — | 0 | — | ns |
| $t_{REF}$ | Auto Refresh Period (1,024 Cycles) | — | 16 | — | 16 | ms |
| $t_T$ | Transition Time (Rise or Fall)[2, 3] | 1 | 50 | 1 | 50 | ns |

## AC TEST CONDITIONS

Output load: Two TTL Loads and 50 pF (Vcc = 5.0V ±10%)
One TTL Load and 50 pF (Vcc = 3.3V ±10%)

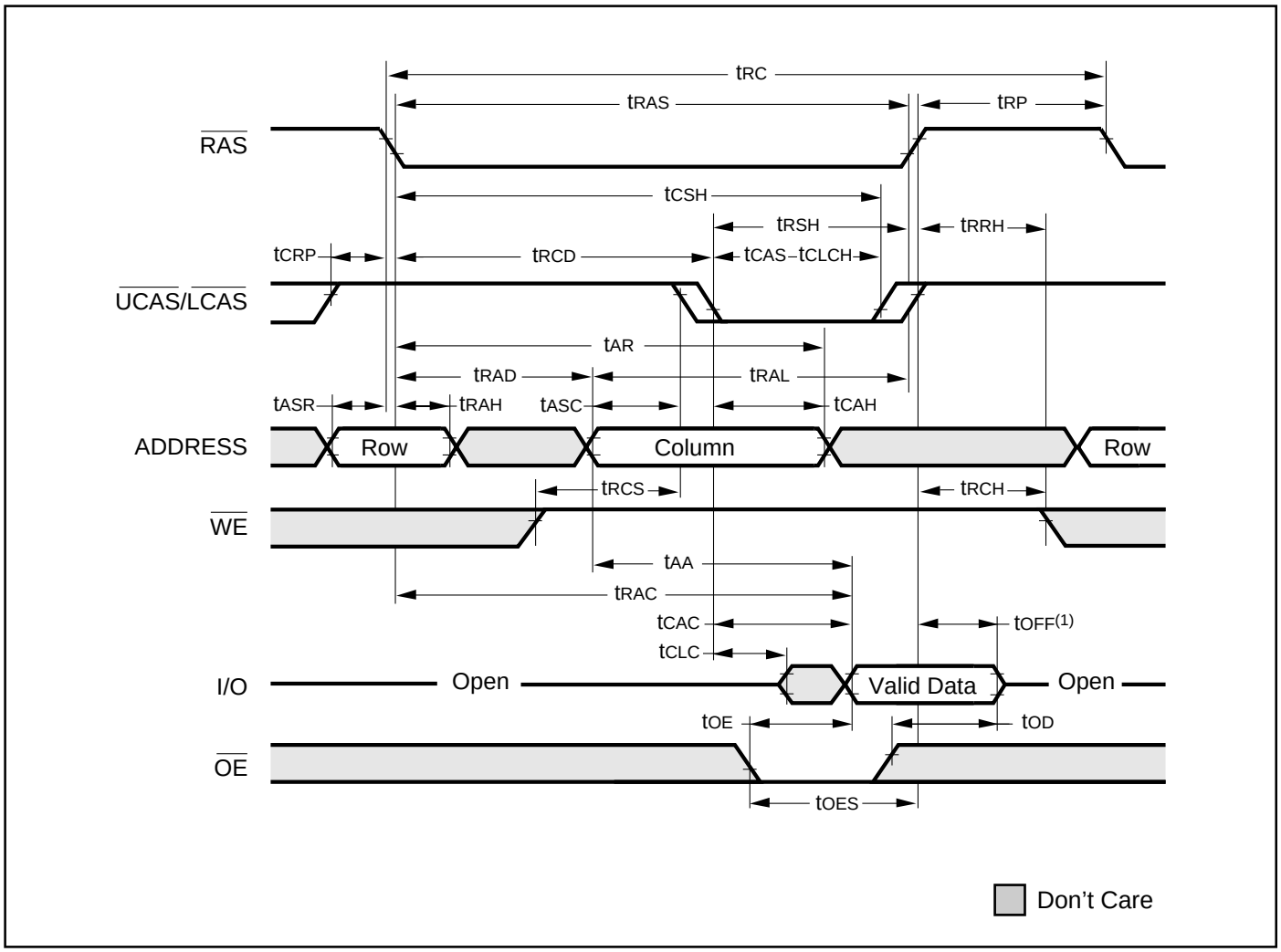
Input timing reference levels: $V_{IH}$ = 2.4V, $V_{IL}$ = 0.8V (Vcc = 5.0V ±10%);
$V_{IH}$ = 2.0V, $V_{IL}$ = 0.8V (Vcc = 3.3V ±10%)

Output timing reference levels: $V_{OH}$ = 2.0V, $V_{OL}$ = 0.8V (Vcc = 5V ±10%, 3.3V ±10%)

Notes:

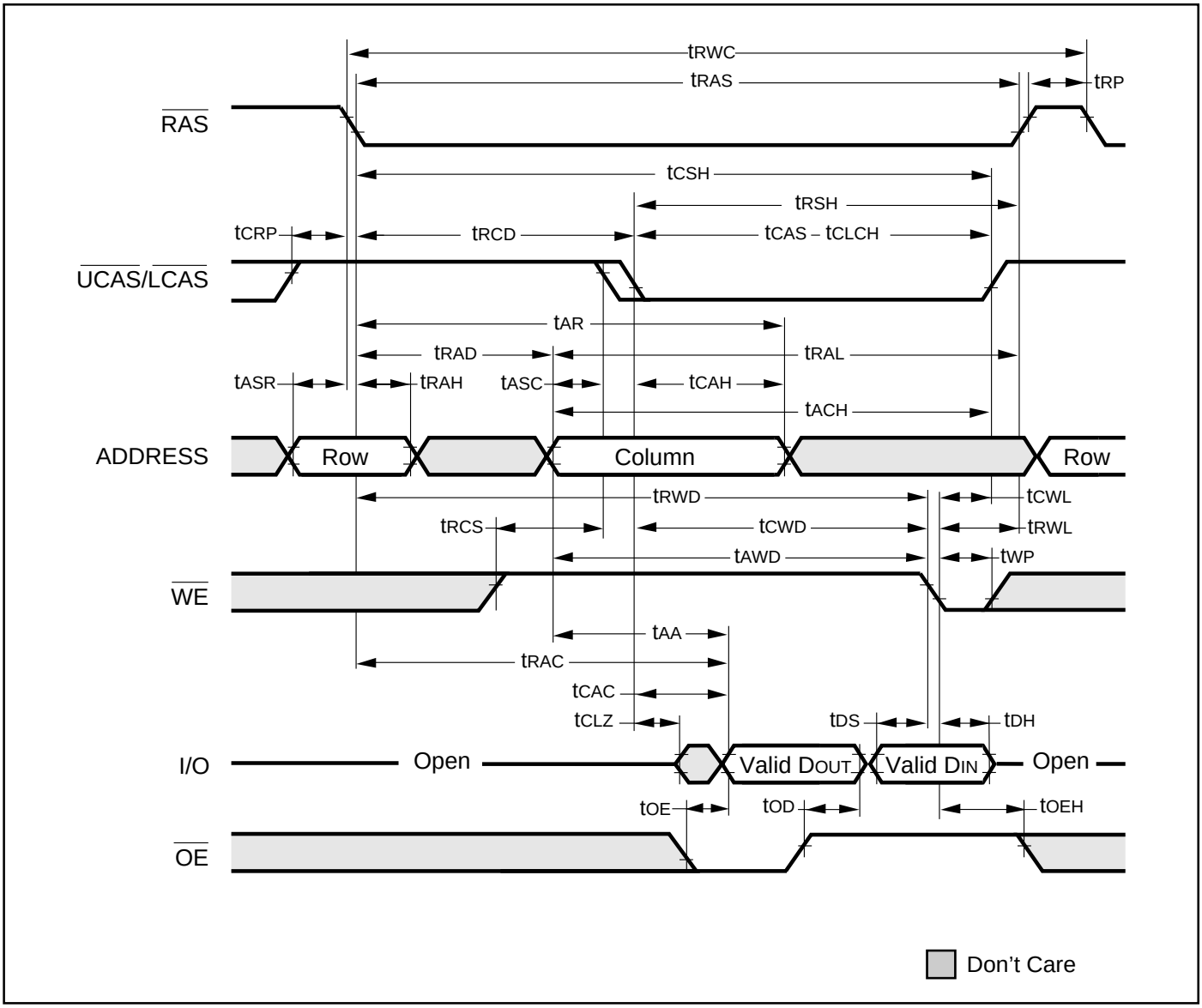
1. An initial pause of 200 $\mu$s is required after power-up followed by eight $\overline{RAS}$ refresh cycle ($\overline{RAS}$-Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the $t_{REF}$ refresh requirement is exceeded.
2. $V_{IH}$ (MIN) and $V_{IL}$ (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
4. If $\overline{CAS}$ and $\overline{RAS}$ = $V_{IH}$, data output is High-Z.
5. If $\overline{CAS}$ = $V_{IL}$, data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (MAX). If $t_{RCD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will increase by the amount that $t_{RCD}$ exceeds the value shown.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (MAX).
9. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed for $t_{CP}$.
10. Operation with the $t_{RCD}$ (MAX) limit ensures that $t_{RAC}$ (MAX) can be met. $t_{RCD}$ (MAX) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (MAX) limit, access time is controlled exclusively by $t_{CAC}$.
11. Operation within the $t_{RAD}$ (MAX) limit ensures that $t_{RCD}$ (MAX) can be met. $t_{RAD}$ (MAX) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$ (MAX) limit, access time is controlled exclusively by $t_{AA}$.
12. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a READ cycle.
13. $t_{OFF}$ (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to $V_{OH}$ or $V_{OL}$.
14. $t_{WCS}$, $t_{RWD}$, $t_{AWD}$ and $t_{CWD}$ are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If $t_{WCS} \geq t_{WCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (MIN), $t_{AWD} \geq t_{AWD}$ (MIN) and $t_{CWD} \geq t_{CWD}$ (MIN), the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to $V_{IH}$) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW result in a LATE WRITE ($\overline{OE}$-controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding $\overline{CAS}$ input, I/O0-I/O7 by $\overline{LCAS}$ and I/O8-I/O15 by $\overline{UCAS}$.
16. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, I/O goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as $\overline{WE}$ going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both $t_{OD}$ and $t_{OEH}$ met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back to LOW after $t_{OEH}$ is met.
19. The I/Os are in open during READ cycles once $t_{OD}$ or $t_{OFF}$ occur.
20. The first $\chi\overline{CAS}$ edge to transition LOW.
21. The last $\chi\overline{CAS}$ edge to transition HIGH.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. Last falling $\chi\overline{CAS}$ edge to first rising $\chi\overline{CAS}$ edge.
24. Last rising $\chi\overline{CAS}$ edge to next cycle's last rising $\chi\overline{CAS}$ edge.
25. Last rising $\chi\overline{CAS}$ edge to first falling $\chi\overline{CAS}$ edge.
26. Each $\chi\overline{CAS}$ must meet minimum pulse width.
27. Last $\chi\overline{CAS}$ to go LOW.
28. I/Os controlled, regardless $\overline{UCAS}$ and $\overline{LCAS}$.
29. The 3 ns minimum is a parameter guaranteed by design.
30. Enables on-chip refresh and address counters.

## READ CYCLE

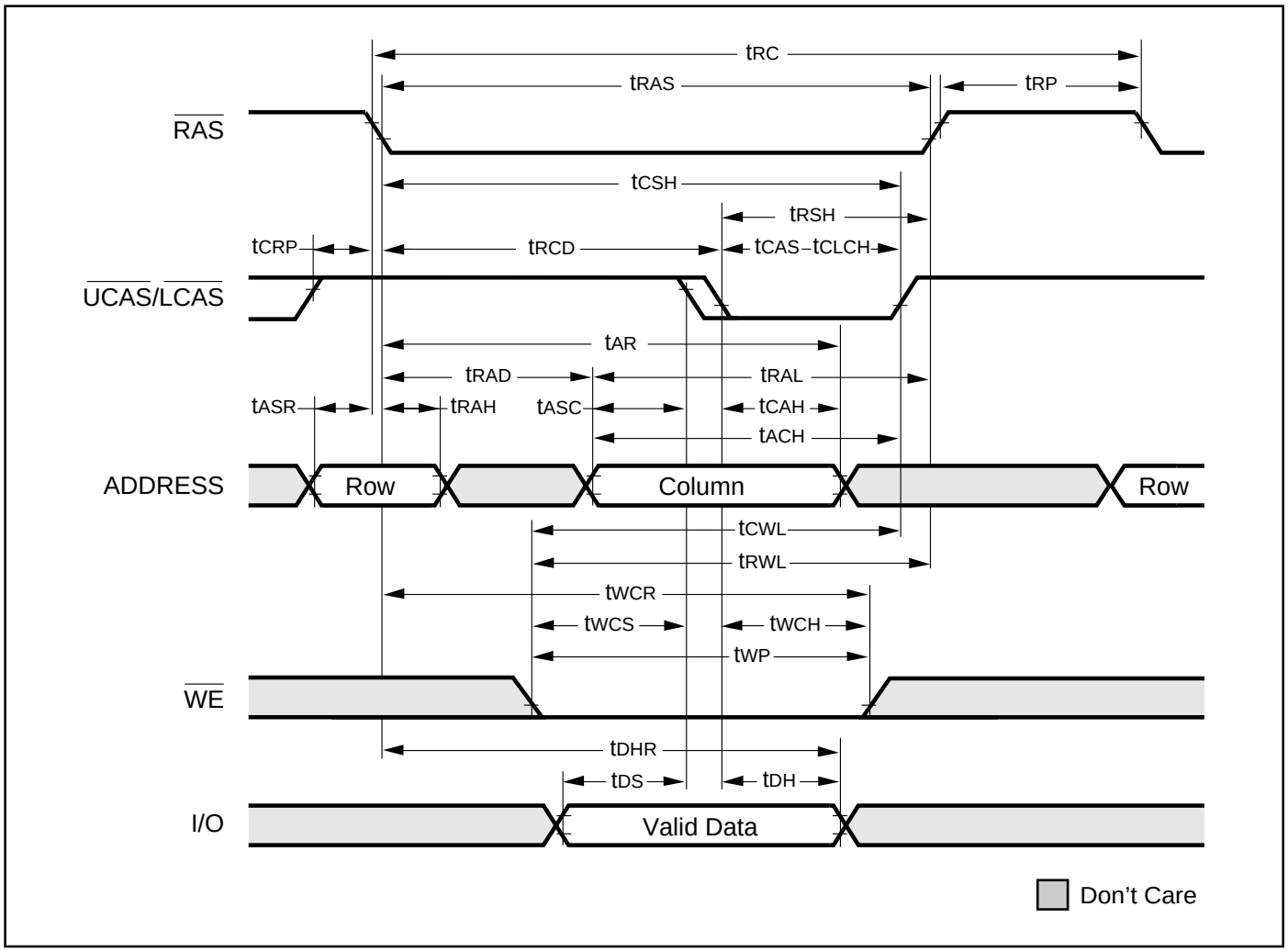



Note:
1. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

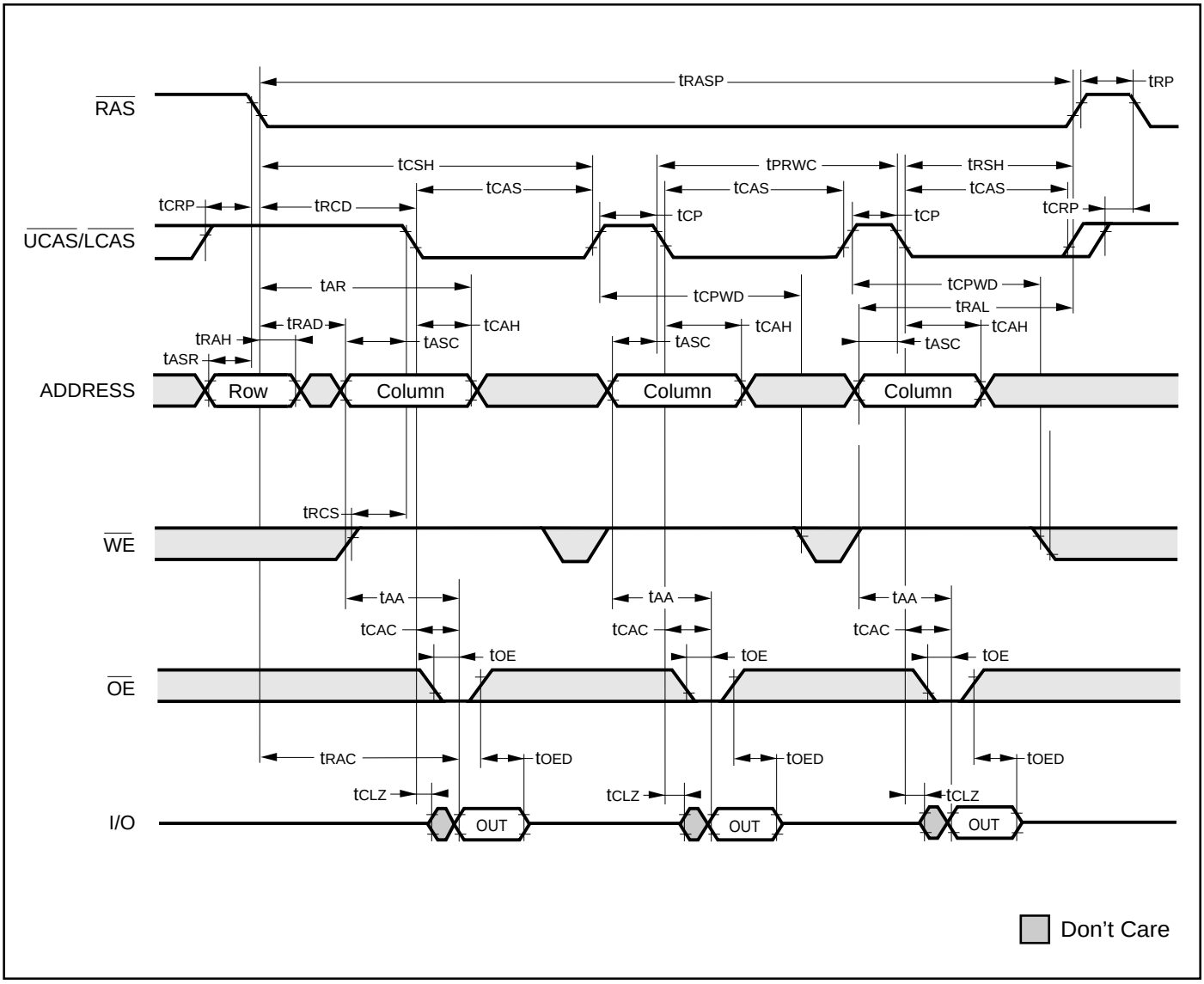
## READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)



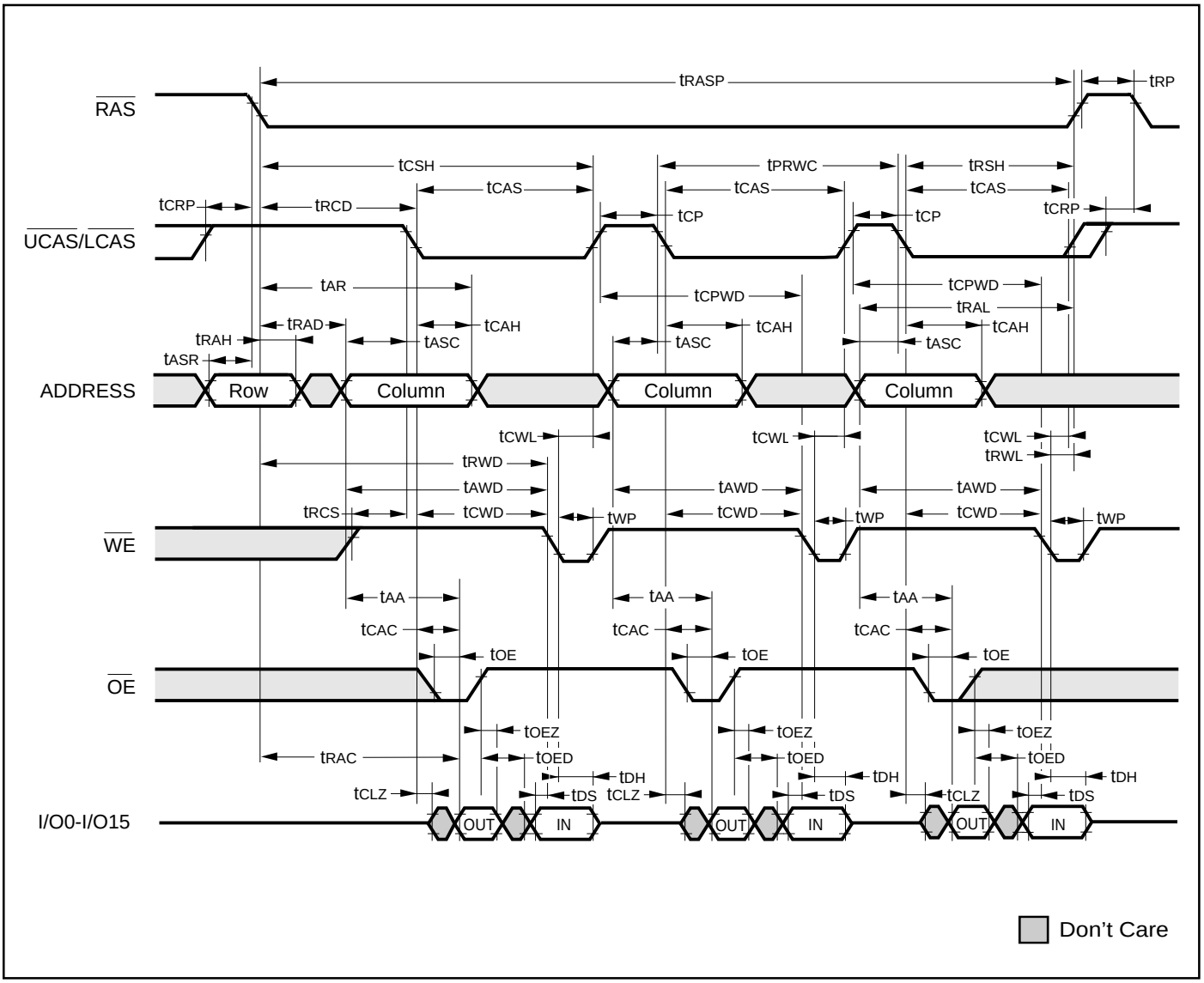
## EARLY WRITE CYCLE ($\overline{OE}$ = DON'T CARE)



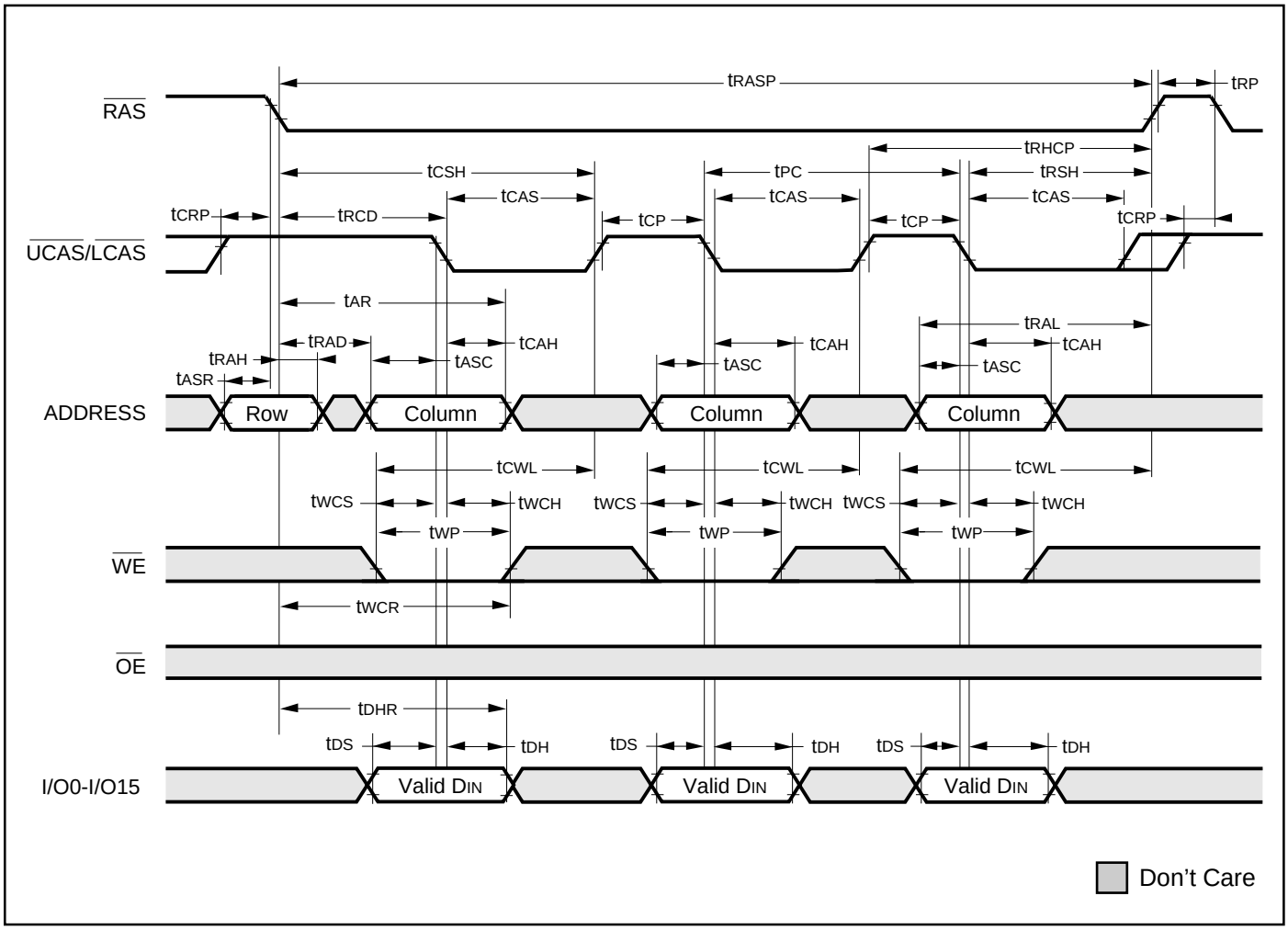
## FAST PAGE MODE READ CYCLE



## FAST PAGE MODE READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)

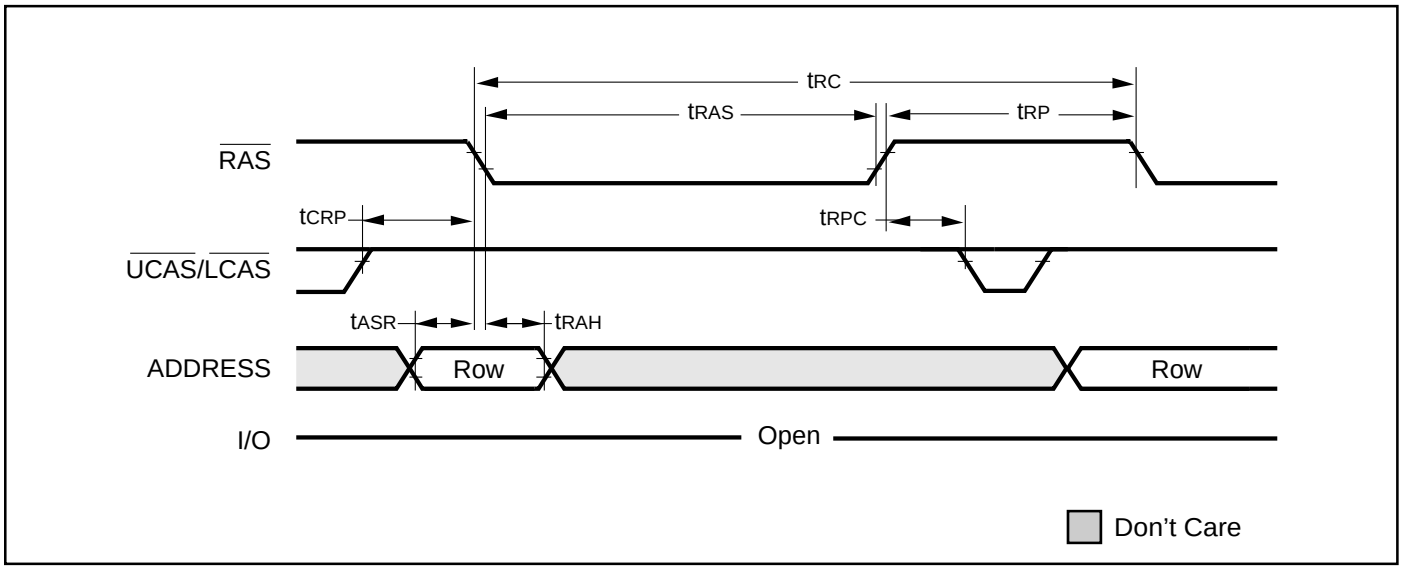


## FAST PAGE MODE EARLY WRITE CYCLE

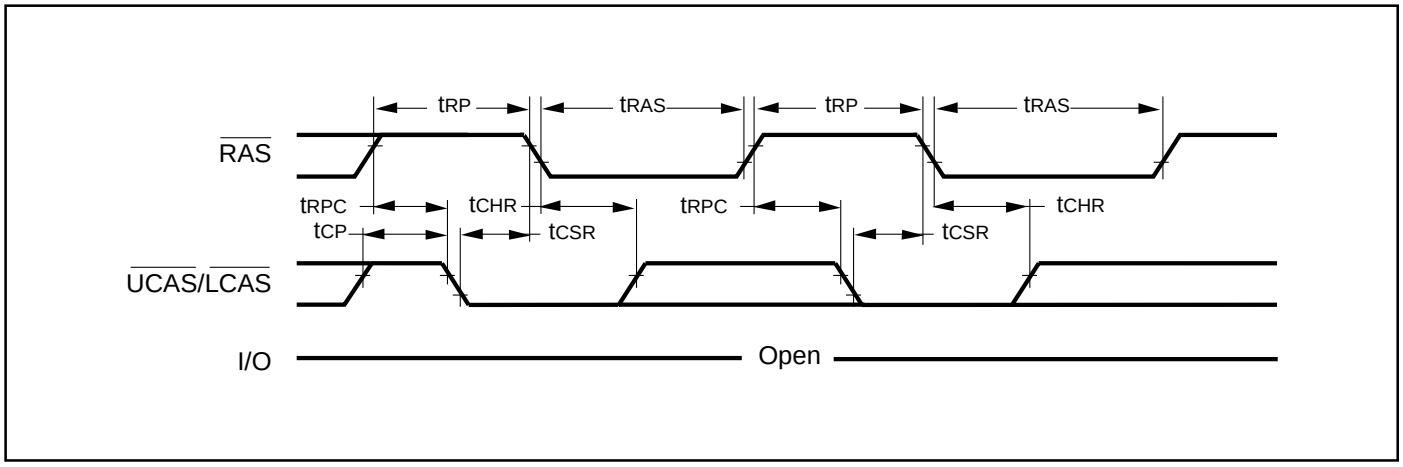



## AC WAVEFORMS

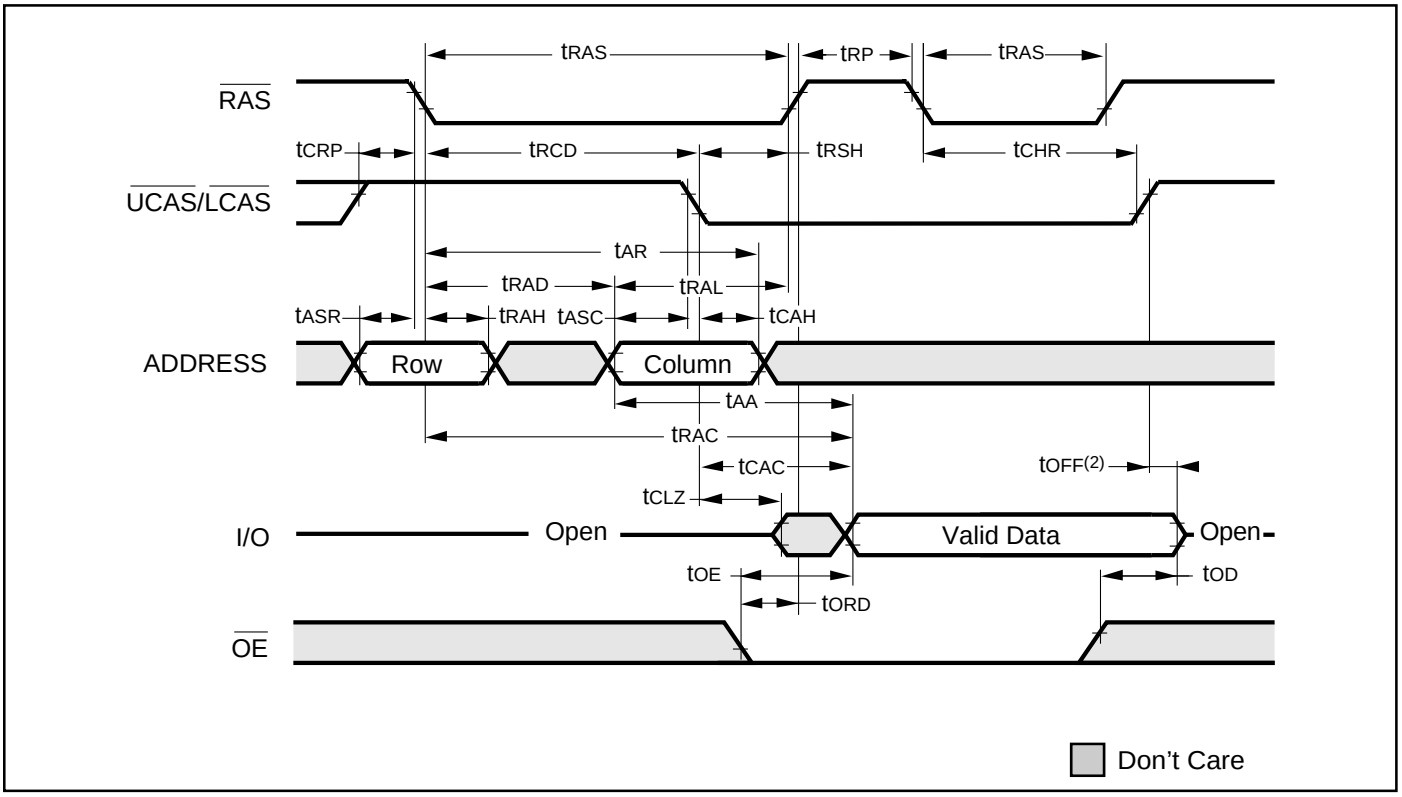
### RAS-ONLY REFRESH CYCLE (OE, WE = DON'T CARE)



## CBR REFRESH CYCLE (Addresses; WE, OE = DON'T CARE)

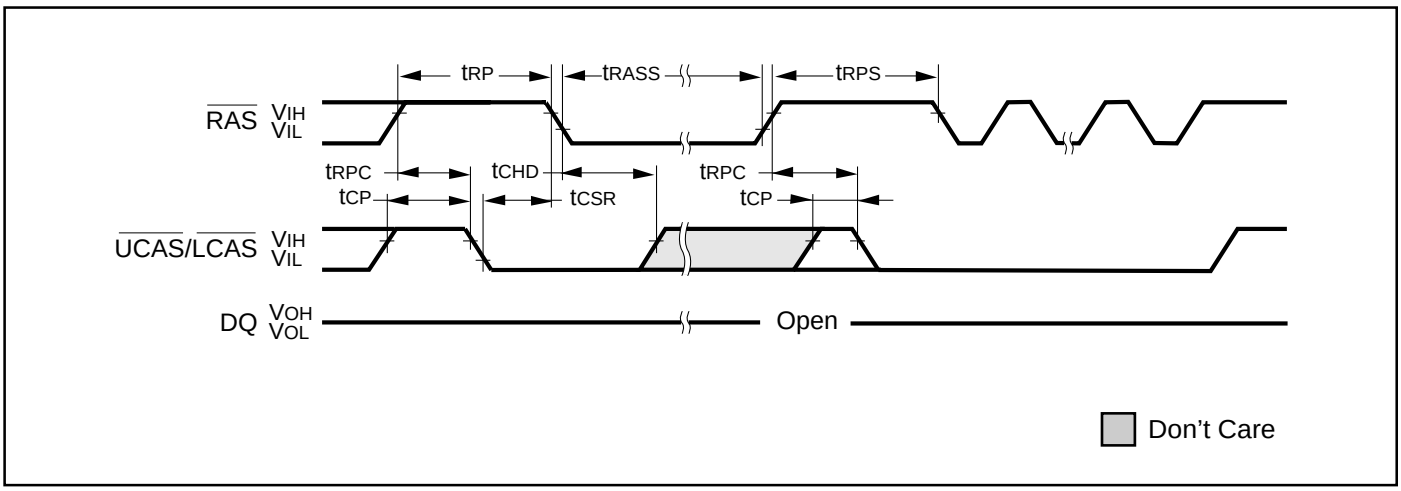



## HIDDEN REFRESH CYCLE(1) (WE = HIGH; OE = LOW)




Notes:
1. A Hidden Refresh may also be performed after a Write Cycle. In this case, WE = LOW and OE = HIGH.
2. tOFF is referenced from rising edge of RAS or CAS, whichever occurs last.

## SELF REFRESH CYCLE (Addresses : $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)




## TIMING PARAMETERS

| Symbol | -50 Min. | -50 Max. | -60 Min. | -60 Max. | Units |
|---|---|---|---|---|---|
| $t_{CHD}$ | 8 | — | 10 | — | ns |
| $t_{CP}$ | 9 | — | 9 | — | ns |
| $t_{CSR}$ | 5 | — | 5 | — | ns |
| $t_{RASS}$ | 100 | — | 100 | — | µs |
| $t_{RP}$ | 30 | — | 40 | — | ns |
| $t_{RPS}$ | 84 | — | 104 | — | ns |
| $t_{RPC}$ | 5 | — | 5 | — | ns |

## ORDERING INFORMATION: 5V
## Commercial Range: 0°C to 70°C

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 50 | IC41C16105S-50K | 400mil SOJ |
| | IC41C16105S-50T | 400mil TSOP-2 |
| 60 | IC41C16105S-60K | 400mil SOJ |
| | IC41C16105S-60T | 400mil TSOP-2 |

## ORDERING INFORMATION: 5V
## Industrial Temperature Range: –40°C to 85°C

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 50 | IC41C16105S-50KI | 400mil SOJ |
| | IC41C16105S-50TI | 400mil TSOP-2 |
| 60 | IC41C16105S-60KI | 400mil SOJ |
| | IC41C16105S-60TI | 400mil TSOP-2 |

ORDERING INFORMATION: 3.3V

Commercial Range: 0°C to 70°C

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 50 | IC41LV16105S-50K | 400mil SOJ |
| | IC41LV16105S-50T | 400mil TSOP-2 |
| 60 | IC41LV16105S-60K | 400mil SOJ |
| | IC41LV16105S-60T | 400mil TSOP-2 |

ORDERING INFORMATION: 3.3V

Industrial Temperature Range: –40°C to 85°C

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 50 | IC41LV16105S-50KI | 400mil SOJ |
| | IC41LV16105S-50TI | 400mil TSOP-2 |
| 60 | IC41LV16105S-60KI | 400mil SOJ |
| | IC41LV16105S-60TI | 400mil TSOP-2 |

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