Document Title

1M x 32 Bit x 4 Banks (128-MBIT) SDRAM

Revision History

Revision No	History	Draft Date	Remark
0A	Initial Draft	December 01,2003	
0B	Revise Page22 typo	December 21,2004	
0C	Revise p.22 data and p.28 typo	February 01,2005	

1M Words x 32 Bits x 4 Banks (128-MBIT) SYNCHRONOUS DYNAMIC RAM

FEATURES

· Concurrent auto precharge
· Clock rate:166/143/125 MHz
· Fully synchronous operation
· Internal pipelined architecture
· Four internal banks (1M x 32bit x 4bank)
· Programmable Mode
  -CAS#Latency:2 or 3
  -Burst Length:1,2,4,8,or full page
  -Burst Type:interleaved or linear burst
  -Burst-Read-Single-Write
· Burst stop function
· Individual byte controlled by DQM0-3
· Auto Refresh and Self Refresh
· 4096 refresh cycles/64ms
· Single +3.3V ±0.3V power supply
· Interface:LVTTL
· Package:400 x 875 mil,86 Pin TSOP-2,0.50mm Pin Pitch and 11x13mm, 90 Ball BGA, Ball pitch 0.8mm
· Pb-free package is available.

DESCRIPTION

The ***ICSI*** IC42S32400 and IC42S32400L is a high-speed CMOS configured as a quad 1M x 32 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal,CLK).

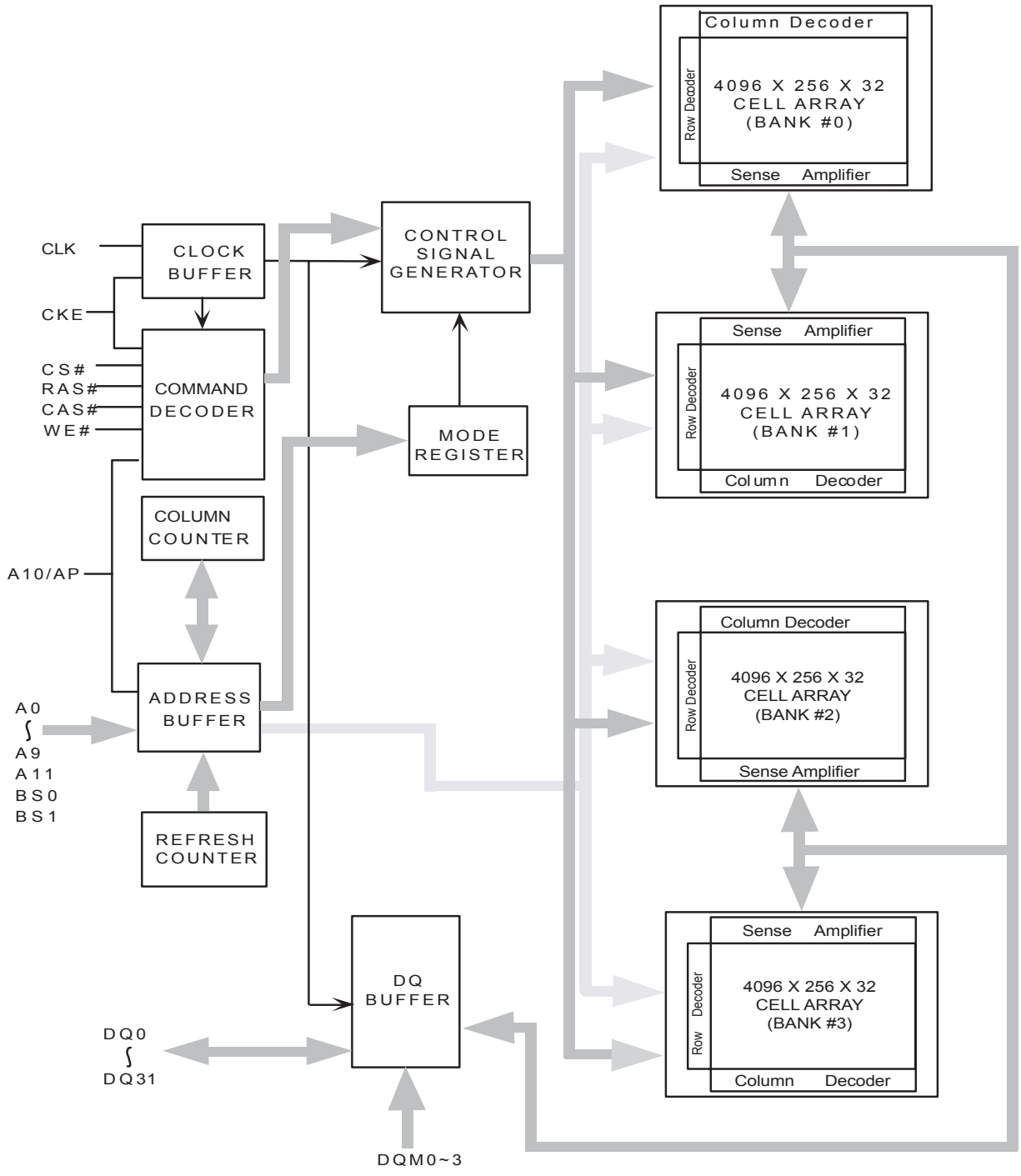
Each of the 1M x 32 bit banks is organized as 4096 rows by 256 columns by 32 bits.Read and write accesses start at a selected locations in a programmed sequence. Accesses begin with the registration of a BankActive command which is then followed by a Read or Write command

The ***ICSI*** IC42S32400 and IC42S32400L provides for programmable Read or Write burst lengths of 1,2,4,8,or full page, with a burst termination operation. An auto precharge function may be enable to provide a self-timed row precharge that is initiated at the end of the burst sequence.The refresh functions,either Auto or Self Refresh are easy to use.

By having a programmable mode register,the system can choose the most suitable modes to maximize its performance.

These devices are well suited for applications requiring high memory bandwidth.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Table 1.Pin Details of IC42S32400 and IC42S32400L

Symbol	Type	Description
CLK	**Input**	**Clock:**CLK is driven by the system clock.All SDRAM input signals are sampled on the positive edge of CLK.CLK also increments the internal burst counter and controls the output registers.
CKE	**Input**	**Clock Enable:**CKE activates(HIGH)and deactivates(LOW)the CLK signal.If CKE goes low synchronously with clock(set-up and hold time same as other inputs),the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low.When all banks are in the idle state,deactivating the clock controls the entry to the Power Down and Self Refresh modes.CKE is synchronous except after the device enters Power Down and Self Refresh modes,where CKE becomes asynchronous until exiting the same mode. The input buffers,including CLK,are disabled during Power Down and Self Refresh modes,providing low standby power.
BS0,BS1	**Input**	**Bank Select:**BS0 and BS1 defines to which bank the BankActivate,Read,Write,or BankPrecharge command is being applied.
A0-A11	**Input**	**Address Inputs:**A0-A11 are sampled during the BankActivate command (row address A0-A11)and Read/Write command (column address A0-A7 with A10 defining Auto Precharge) to select one location in the respective bank.During a Precharge command,A10 is sampled to determine if all banks are to be precharged (A10 =HIGH). The address inputs also provide the op-code during a Mode Register Set .
CS#	**Input**	**Chip Select:**CS#enables (sampled LOW)and disables (sampled HIGH)the command decoder.All commands are masked when CS#is sampled HIGH.CS#provides for external bank selection on systems with multiple banks.It is considered part of the command code.
RAS#	**Input**	**Row Address Strobe:**The RAS#signal defines the operation commands in conjunction with the CAS#and WE#signals and is latched at the positive edges of CLK.When RAS# and CS#are asserted “LOW”and CAS#is asserted “HIGH,”either the BankActivate command or the Precharge command is selected by the WE#signal.When the WE#is asserted “HIGH,”the BankActivate command is selected and the bank designated by BS is turned on to the active state.When the WE#is asserted “LOW,”the Precharge command is selected and the bank designated by BS is switched to the idle state after the precharge operation.
CAS#	**Input**	**Column Address Strobe:**The CAS#signal defines the operation commands in conjunction with the RAS#and WE#signals and is latched at the positive edges of CLK. When RAS#is held “HIGH”and CS#is asserted “LOW,”the column access is started by asserting CAS#”LOW.”Then,the Read or Write command is selected by asserting WE# “LOW”or “HIGH.”
WE#	**Input**	**Write Enable:**The WE#signal defines the operation commands in conjunction with the RAS#and CAS#signals and is latched at the positive edges of CLK.The WE#input is used to select the BankActivate or Precharge command and Read or Write command.
DQM0-3	**Input**	**Data Input/Output Mask:**DQM0-DQM3 are byte specific,nonpersistent I/O buffer controls. The I/O buffers are placed in a high-z state when DQM is sampled HIGH.Input data is masked when DQM is sampled HIGH during a write cycle.Output data is masked (two-clock latency)when DQM is sampled HIGH during a read cycle.DQM3 masks DQ31-DQ24,DQM2 masks DQ23-DQ16,DQM1 masks DQ15-DQ8,and DQM0 masks DQ7-DQ0.
DQ0-31	**Input/Output**	**Data I/O:**The DQ0-31 input and output data are synchronized with the positive edges of CLK.The I/Os are byte-maskable during Reads and Writes.

PIN FUNCTION

NC	**-**	**No Connect:**These pins should be left unconnected.
VDDQ	Supply	**DQ Power:**Provide isolated power to DQs for improved noise immunity.
VSSQ	Supply	**DQ Ground:**Provide isolated ground to DQs for improved noise immunity.
VDD	Supply	**Power Supply:**+3.3V ± 0.3V
VSS	Supply	**Ground**

PIN CONFIGURATIONS

86-Pin TSOP 2

Pin Assignment (Top View)

VDD	1	86	VSS
DQ0	2	85	DQ15
VDDQ	3	84	VSSQ
DQ1	4	83	DQ14
DQ2	5	82	DQ13
VSSQ	6	81	VDDQ
DQ3	7	80	DQ12
DQ4	8	79	DQ11
VDDQ	9	78	VSSQ
DQ5	10	77	DQ10
DQ6	11	76	DQ9
VSSQ	12	75	VDDQ
DQ7	13	74	DQ8
NC	14	73	NC
VDD	15	72	VSS
DQM0	16	71	DQM1
/WE	17	70	NC
/CAS	18	69	NC
/RAS	19	68	CLK
/CS	20	67	CKE
A11	21	66	A9
BS0	22	65	A8
BS1	23	64	A7
A10/AP	24	63	A6
A0	25	62	A5
A1	26	61	A4
A2	27	60	A3
DQM2	28	59	DQM3
VDD	29	58	VSS
NC	30	57	NC
DQ16	31	56	DQ31
VSSQ	32	55	VDDQ
DQ17	33	54	DQ30
DQ18	34	53	DQ29
VDDQ	35	52	VSSQ
DQ19	36	51	DQ28
DQ20	37	50	DQ27
VSSQ	38	49	VDDQ
DQ21	39	48	DQ26
DQ22	40	47	DQ25
VDDQ	41	46	VSSQ
DQ23	42	45	DQ24
VDD	43	44	VSS

90-Ball FBGA

	1	2	3	4	5	6	7	8	9
A	DQ26	DQ24	VSS				VDD	DQ23	DQ21
B	DQ28	VDDQ	VSSQ				VDDQ	VSSQ	DQ19
C	VSSQ	DQ27	DQ25				DQ22	DQ20	VDDQ
D	VSSQ	DQ29	DQ30				DQ17	DQ18	VDDQ
E	VDDQ	DQ31	NC				NC	DQ16	VSSQ
F	VSS	DQM3	A3				A2	DQM2	VDD
G	A4	A5	A6		(Top View)		A10	A0	A1
H	A7	A8	NC				NC	BA1	A11
J	CLK	CKE	A9				BA0	$\overline{CS}$	$\overline{RAS}$
K	DQM1	NC	NC				$\overline{CAS}$	$\overline{WE}$	DQM0
L	VDDQ	DQ8	VSS				VDD	DQ7	VSSQ
M	VSSQ	DQ10	DQ9				DQ6	DQ5	VDDQ
N	VSSQ	DQ12	DQ14				DQ1	DQ3	VDDQ
P	DQ11	VDDQ	VSSQ				VDDQ	VSSQ	DQ4
R	DQ13	DQ15	VSS				VDD	DQ0	DQ2

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CLK.Table 2 shows the truth table for the operation commands.

Table 2.Truth Table (Note (1),(2))

Command	State	CKEn-1	CKE	DQM(6)	BS0,1	A10	A11,A9-0	CS#	RAS#	CAS#	WE#
BankActivate	Idle (3)	H	X	X	V	Row address		L	L	H	H
BankPrecharge	Any	H	X	X	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	H	X	L	L	H	L
Write	Active (3)	H	X	X	V	L	Column address (A0 ~A7)	L	H	L	L
Write and Auto Precharge	Active (3)	H	X	X	V	H		L	H	L	L
Read	Active (3)	H	X	X	V	L	Column address (A0 ~A7)	L	H	L	H
Read and Autoprecharge	Active (3)	H	X	X	V	H		L	H	L	H
Mode Register	Set Idle	H	X	X		OP code		L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active(4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AutoRefresh	Idle	H	H	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle	L	H	X	X	X	X	H	X	X	X
	(SelfRefresh)							L	H	H	H
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Mode Entry	Any(5)	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any	L	H	X	X	X	X	H	X	X	X
	(PowerDown)							L	H	H	H
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Mask/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

Note:

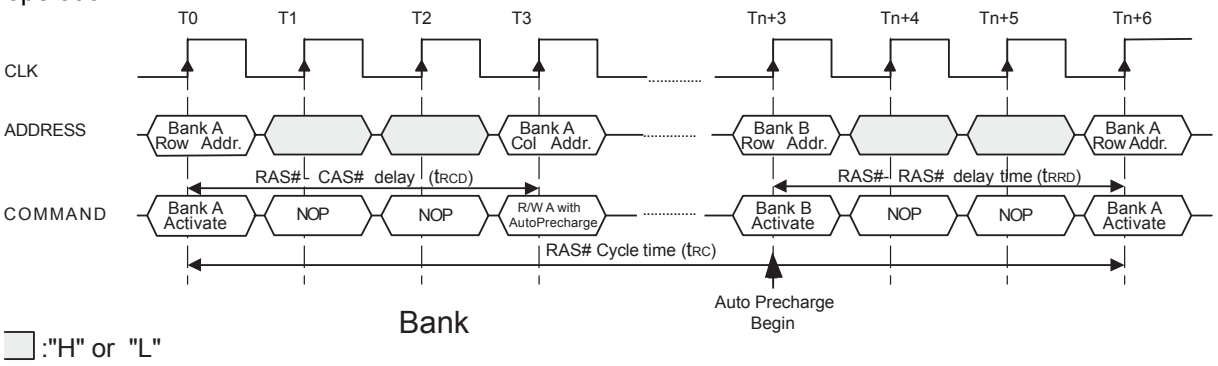
1. V =Valid,X =Don 't care,L =Logic low,H =Logic high
2. CKEn signal is input level when commands are provided.
   CKEn-1 signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BS signal.
4. Device state is 1,2,4,8,and full page burst operation.
5. Power Down Mode can not enter in the burst operation.
   When this command is asserted in the burst cycle,device state is clock suspend mode.
6. DQM0-3

Commands

1 BankActivate

(RAS#="L",CAS#="H",WE#="H",BS =Bank,A0-A11 =Row Address)

The BankActivate command activates the idle bank designated by the BS0,1 (Bank Select) signal.By latching the row address on A0 to A11 at the time of this command,the selected row access is initiated.The read or write operation in the same bank can occur after a time delay of tRCD(min.)from the time of bank activation.A subsequent BankActivate command to a different row in the same bank can only be issued after the previous active row has been precharged (refer to the following figure).The minimum time interval between successive BankActivate commands to the same bank is defined by tRC(min.).The SDRAM has four internal banks on the same chip and shares part of the internal circuitry to reduce chip area;therefore it restricts the back-to-back activation of the four banks.tRRD(min.)specifies the minimum time required between activating different banks. After this command is used,the Write command and the Block Write command perform the no mask write operation.



2 BankPrecharge command

(RAS#="L",CAS#="H",WE#="L",BS =Bank,A10 ="L")

The BankPrecharge command precharges the bank disignated by BS0,1 signal.The precharged bank is switched from the active state to the idle state.This command can be asserted anytime after tRAS(min.)is satisfied from the BankActivate command in the desired bank.The maximum time any bank can be active is specified by tRAS(max.).Therefore,the precharge function must be performed in any active bank within tRAS(max.).At the end of precharge,the precharged bank is still in the idle state and is ready to be activated again.

3 PrechargeAll command

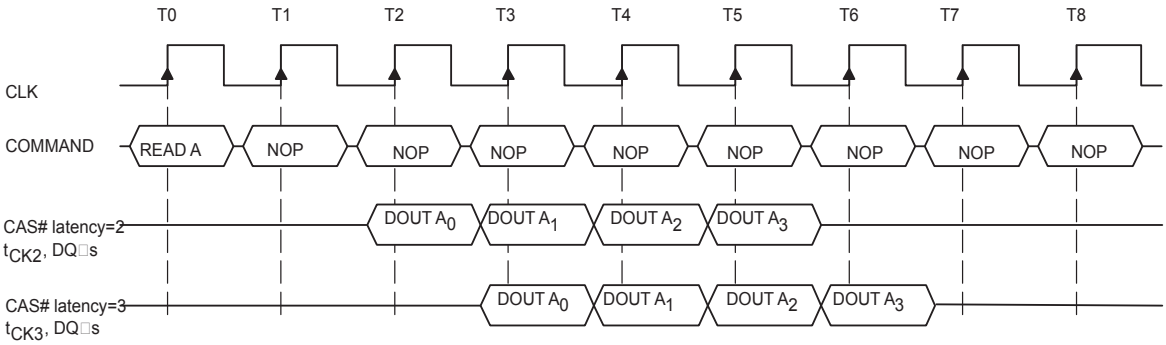
(RAS#=”L”,CAS#=”H”,WE#=”L”,BS =Don t care,A10 =”H”)

The PrechargeAll command precharges all the four banks simultaneously and can be issued even if all banks are not in the active state.All banks are then switched to the idle state.

4 Read command

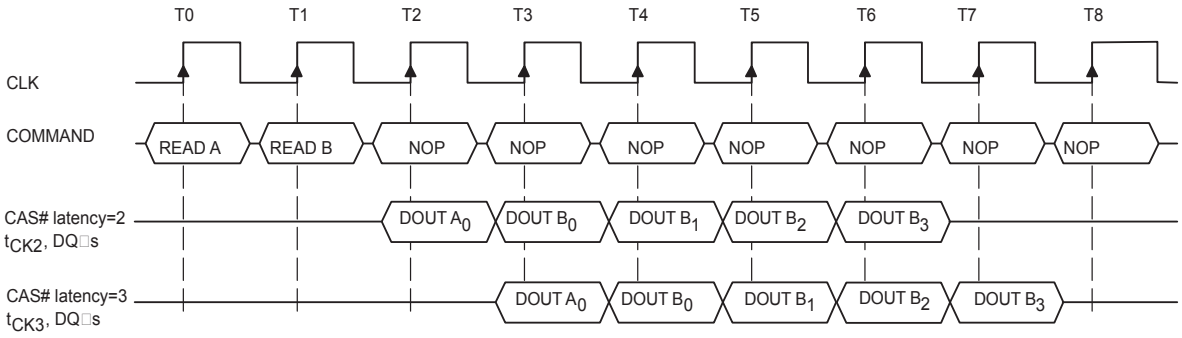
(RAS#=”H”,CAS#=”L”,WE#=”H”,BS =Bank,A10 =”L”,A0-A7 =Column Address)

The Read command is used to read a burst of data on consecutive clock cycles from an active row in an active bank.The bank must be active for at least tRCD(min.)before the Read command is issued.During read bursts, the valid data-out element from the starting column address will be available following the CAS#latency after the issue of the Read command.Each subsequent data- out element will be valid by the next positive clock edge (refer to the following figure).The DQs go into high-impedance at the end of the burst unless other command is initiated.The burst length,burst sequence,and CAS#latency are determined by the mode register which is already programmed.A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).



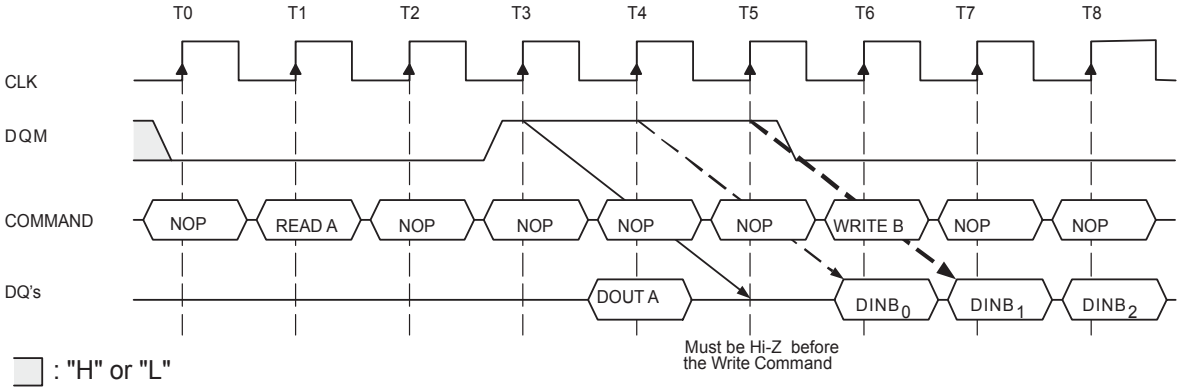
Burst Read Operation(Burst Length =4,CAS#Latency =2,3)

The read data appears on the DQs subject to the values on the DQM inputs two clocks earlier (i.e.DQM latency is two clocks for output buffers).A read burst without the auto precharge function may be interrupted by a subsequent Read or Write command to the same bank or the other active bank before the end of the burst length.It may be interrupted by a BankPrecharge/PrechargeAll command to the same bank too.The interrupt coming from the Read command can occur on any clock cycle following a previous Read command (refer to the following figure).

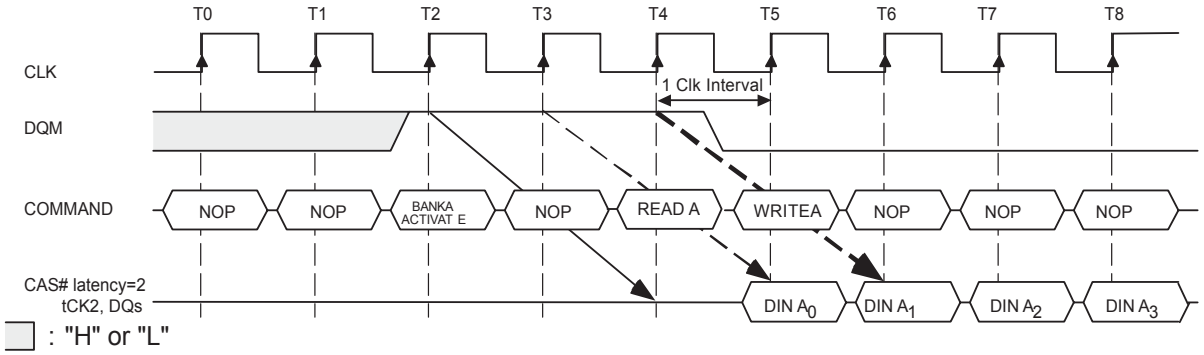


Read Interrupted by a Read (Burst Length =4,CAS#Latency =2,3)

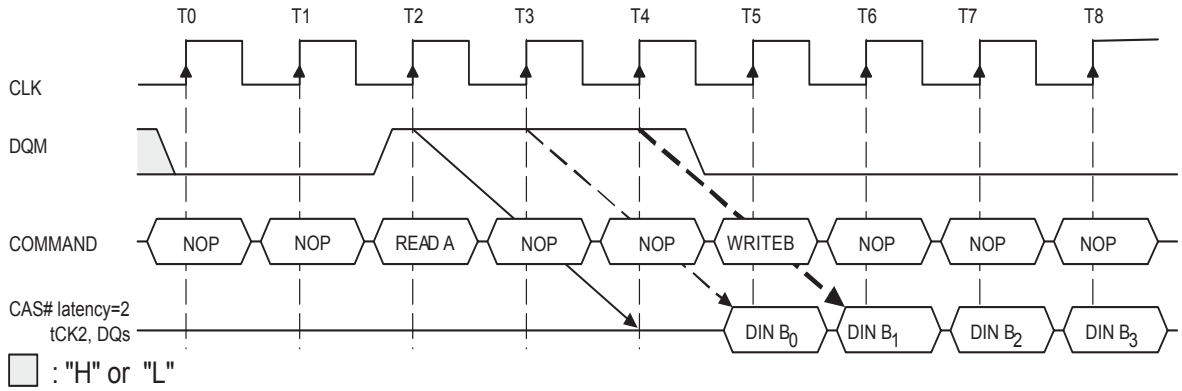
The DQM inputs are used to avoid I/O contention on the DQ pins when the interrupt comes from a Write command.The DQMs must be asserted (HIGH)at least two clocks prior to the Write command to suppress data-out on the DQ pins.To guarantee the DQ pins against I/O contention,a single cycle with high-impedance on the DQ pins must occur between the last read data and the Write command (refer to the following three figures).If the data output of the burst read occurs at the second clock of the burst write,the DQMs must be asserted (HIGH)at least one clock prior to the Write command to avoid internal bus contention.



Read to Write Interval (Burst Length = 4,CAS#Latency =3)

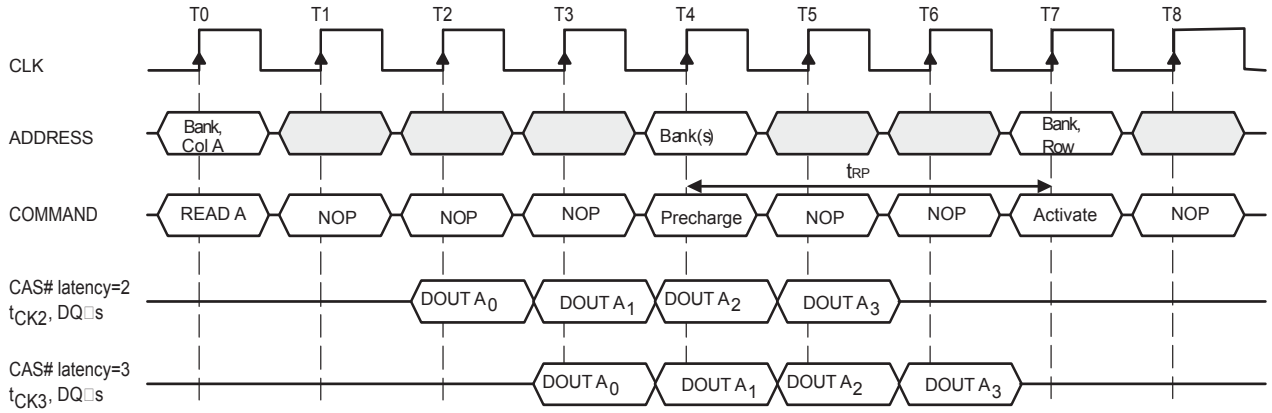


Read to Write Interval (Burst Length = 4,CAS#Latency =2)



Read to Write Interval (Burst Length = 4,CAS#Latency =2)

A read burst without the auto precharge function may be interrupted by a BankPrecharge/ PrechargeAll command to the same bank.The following figure shows the optimum time that BankPrecharge/PrechargeAll command is issued in different CAS#latency.

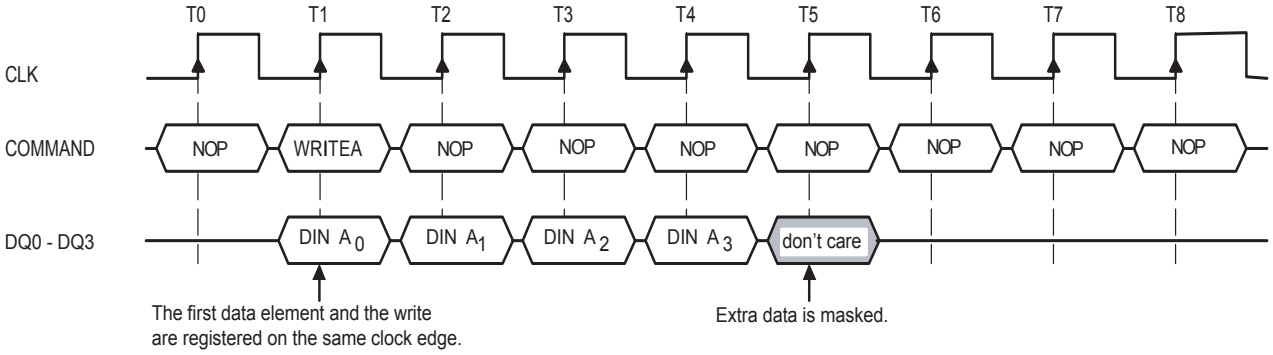


Read to Precharge (CAS#Latency =2,3)

5 Write command

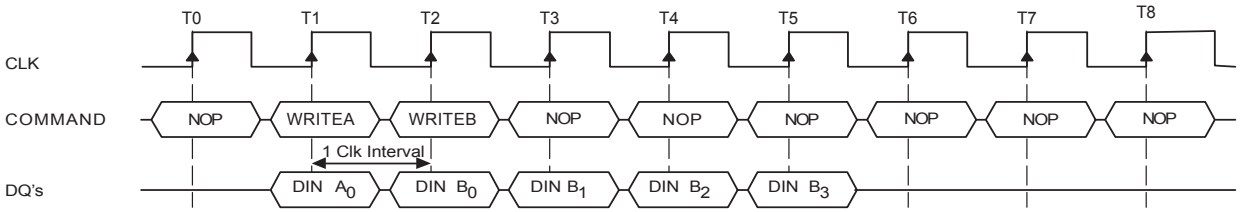
(RAS#="H",CAS#="L",WE#="L",BS =Bank,A10 ="L",A0-A7 =Column Address)

The Write command is used to write a burst of data on consecutive clock cycles from an active row in an active bank.The bank must be active for at least tRCD(min.)before the Write command is issued.During write bursts, the first valid data-in element will be registered coincident with the Write command.Subsequent data elements will be registered on each successive positive clock edge (refer to the following figure).The DQs remain with high-impedance at the end of the burst unless another command is initiated.The burst length and burst sequence are determined by the mode register,which is already programmed.A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).



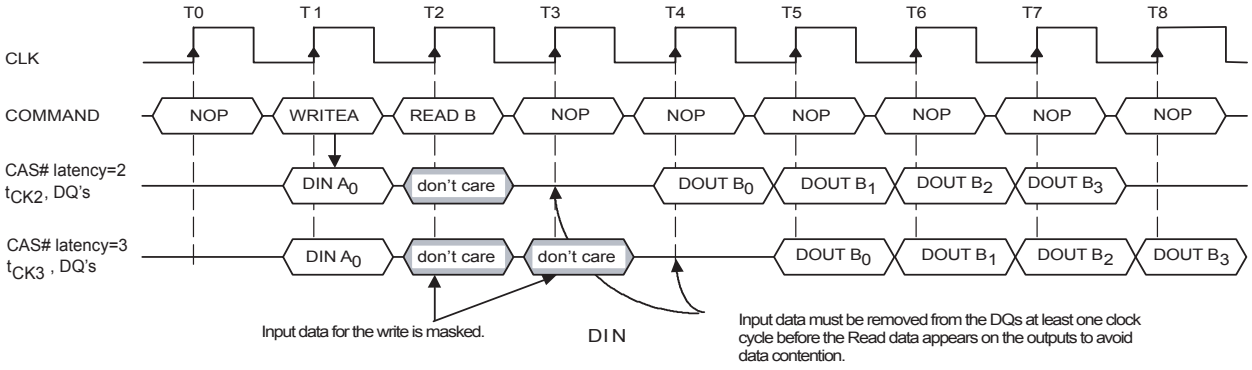
Burst Write Operation (Burst Length =4,CAS#Latency =2,3)

A write burst without the AutoPrecharge function may be interrupted by a subsequent Write, BankPrecharge/ PrechargeAll,or Read command before the end of the burst length.An interrupt coming from Write command can occur on any clock cycle following the previous Write command (refer to the following figure).



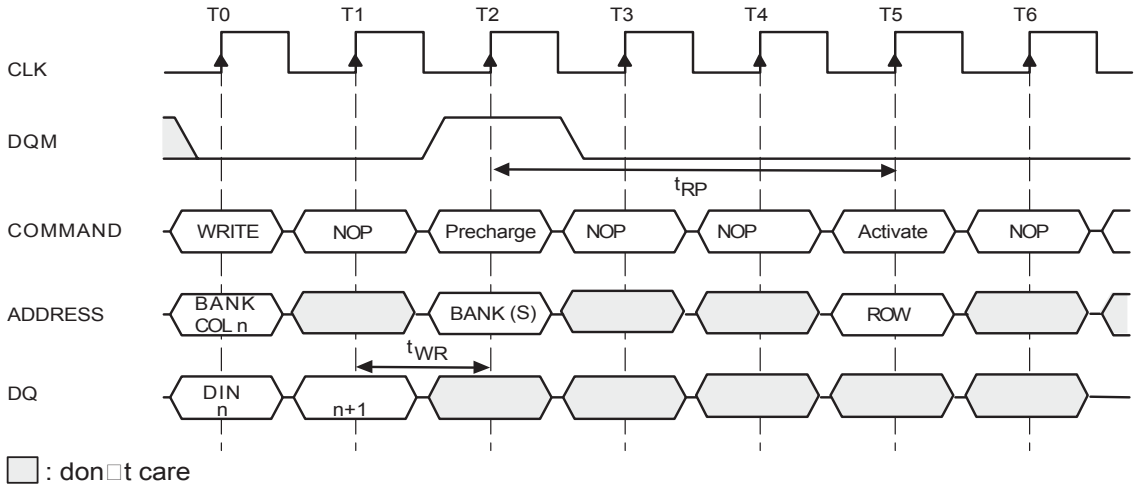
Write Interrupted by a Write (Burst Length =4,CAS#Latency =2,3)

The Read command that interrupts a write burst without auto precharge function should be issued one cycle after the clock edge in which the last data-in element is registered.In order to avoid data contention,input data must be removed from the DQs at least one clock cycle before the first read data appears on the outputs (refer to the following figure).Once the Read command is registered,the data inputs will be ignored and writes will not be executed.



Write Interrupted by a Read (Burst Length =4,CAS#Latency =2,3)

The BankPrecharge/PrechargeAll command that interrupts a write burst without the auto precharge function should be issued *m* cycles after the clock edge in which the last data-in element is registered,where *m* equals tWR/ tCK rounded up to the next whole number.In addition,the DQM signals must be used to mask input data,starting with the clock edge following the last data-in element and ending with the clock edge on which the BankPrecharge/ PrechargeAll command is entered (refer to the following figure).



Note: The DQMs can remain low in this example if the length of the write burst is 1 or 2.

Write to Precharge

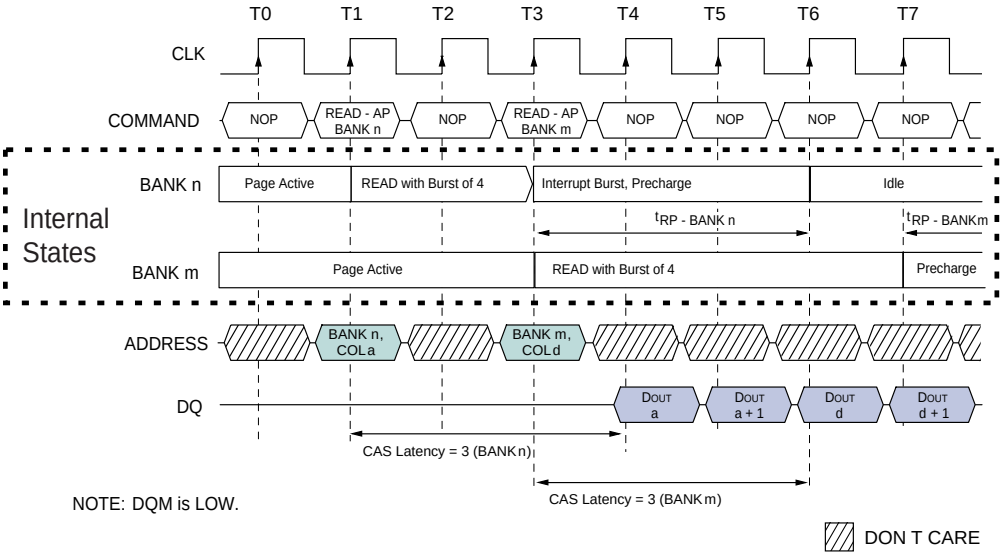
6 Concurrent Auto Precharge

An access command (READ or WRITE) to another bank while an access command with auto precharge enabled is executing is not allowed by SDRAMs, unless the SDRAM supports CONCURRENT AUTO PRECHARGE. ICSI SDRAMs support CONCURRENT AUTO PRECHARGE. Four cases where CONCURRENT AUTO PRECHARGE occurs are defined below.

READ with Auto Precharge

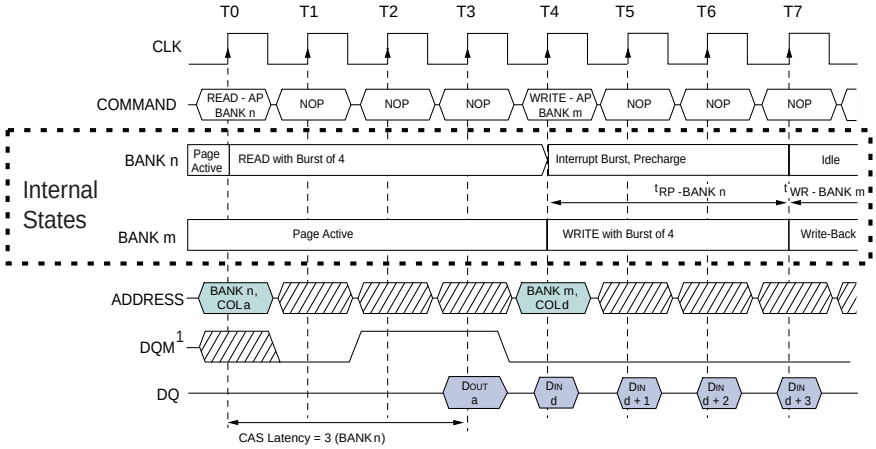
· Interrupted by a READ (with or without auto precharge): A READ to bank m will interrupt a READ on bank n, CAS latency later. The PRECHARGE to bank n will begin when the READ to bank m is regis-tered.

READ With Auto Precharge Interrupted by a READ



· Interrupted by a WRITE (with or without auto precharge): A WRITE to bank m will interrupt a READ on bank n when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank n will begin when the WRITE to bank m is registered.

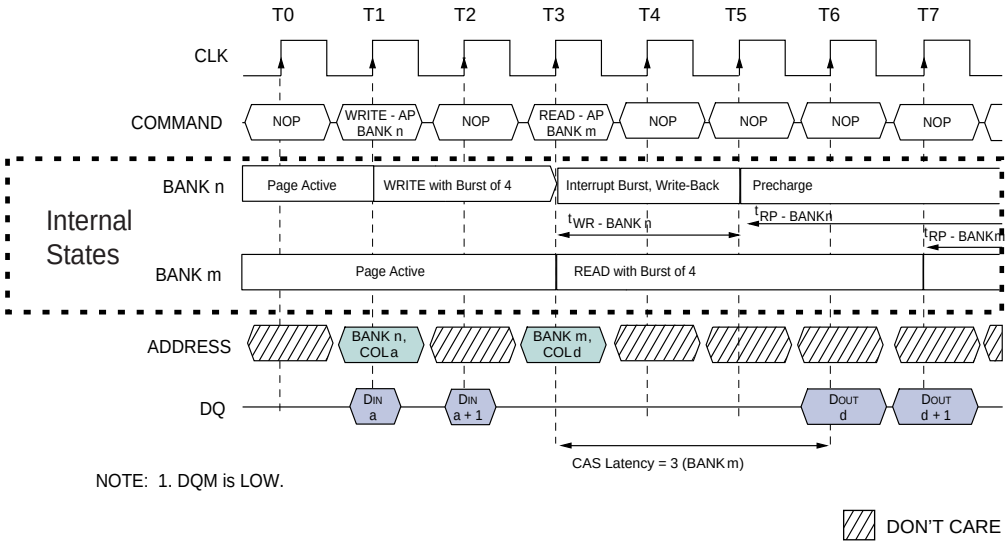
READ With Auto Precharge Interrupted by a WRITE



WRITE with Auto Precharge

· Interrupted by a READ (with or without auto precharge): A READ to bank m will interrupt a WRITE on bank n when registered, with the data-out ap- pearing CAS latency later. The PRECHARGE to bank n will begin after t WR is met, where t WR begins when the READ to bank m is registered. The last valid WRITE to bank n will be data-in registered one clock prior to the READ to bank m.

WRITE With Auto Precharge Interrupted by a READ

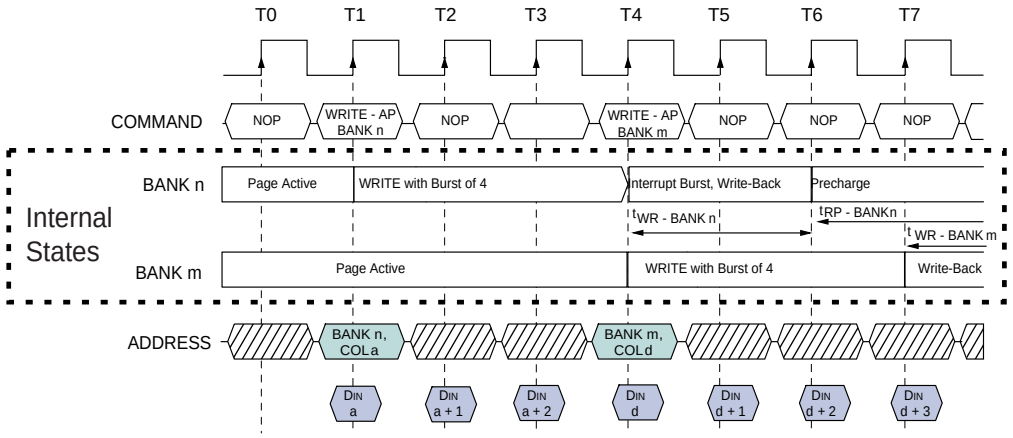


NOTE: 1. DQM is LOW.

DON'T CARE

· Interrupted by a WRITE (with or without auto precharge): A WRITE to bank m will interrupt a WRITE on bank n when registered. The PRECHARGE to bank n will begin after t WR is met, where t WR begins when the WRITE to bank m is registered. The last valid data WRITE to bank n will be data registered one clock prior to a WRITE to bank m.

WRITE With Auto Precharge Interrupted by a WRITE



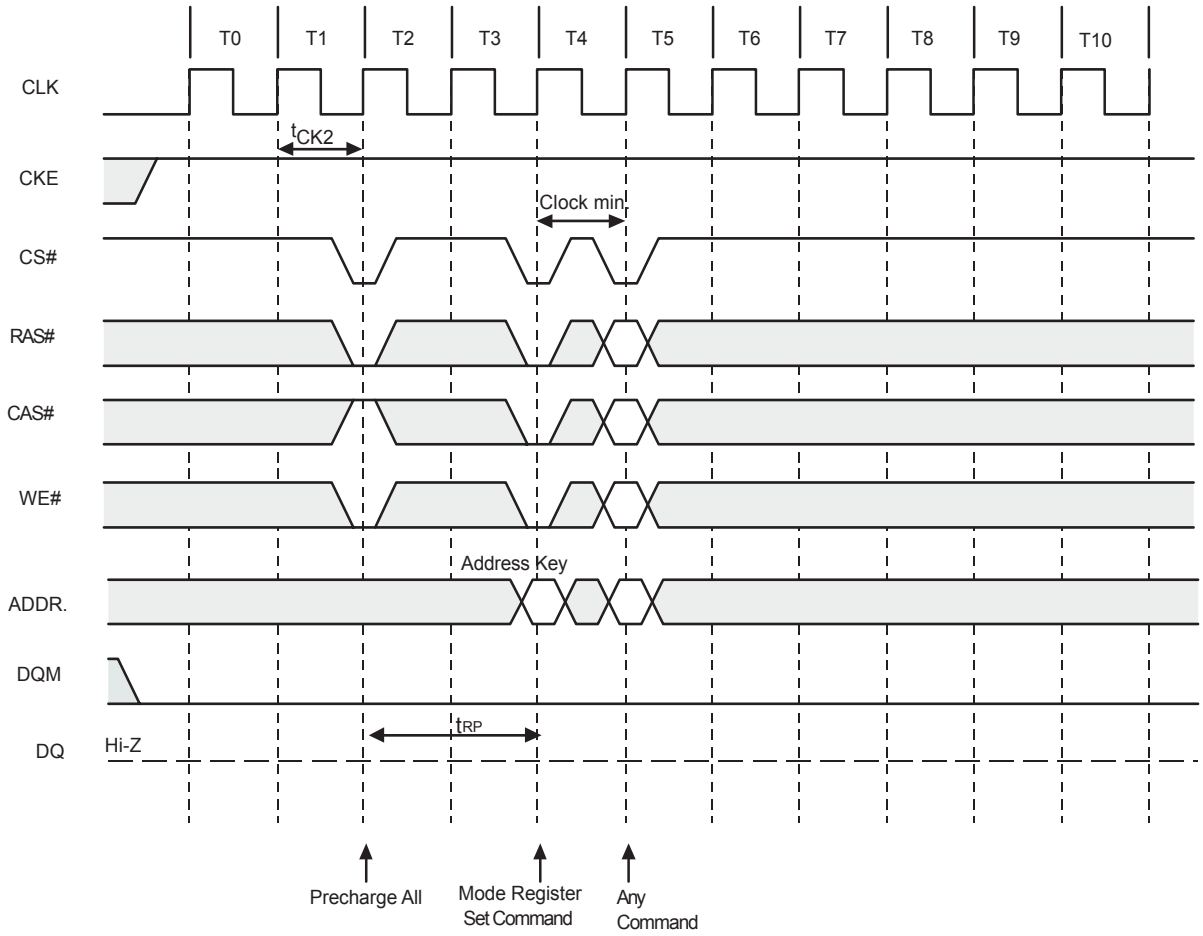
NOTE: 1. DQM is LOW.

DON'T CARE

7 Mode Register Set command

(RAS#="L",CAS#="L",WE#="L",BS0,1 and A11-A0 =Register Data)

The mode register stores the data for controlling the various operating modes of SDRAM.The Mode Register Set command programs the values of CAS#latency,Addressing Mode and Burst Length in the Mode register to make SDRAM useful for a variety of different applications.The default values of the Mode Register after power-up are undefined;therefore this command must be issued at the power-up sequence.The state of pins BS0,1 and A11~A0 in the same cycle is the data written to the mode register.One clock cycle is required to complete the write in the mode register (refer to the following figure).The contents of the mode register can be changed using the same command and the clock cycle requirements during operation as long as all banks are in the idle state.



Mode Register Set Cycle

The mode register is divided into various fields depending on functionality.

Address	BS0,1	A11/A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU*		WBL	Test Mode		CAS Latency			BT	Burst Length		

*Note:RFU (Reserved for future use)should stay 0 during MRS cycle.

- Burst Length Field (A2~A0)

  This field specifies the data length of column access using the A2~A0 pins and selects the Burst Length to be 2,4,8,or full page.

A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Full Page

- Burst Type Field (A3)

The Burst Type can be one of two modes,Interleave Mode or Sequential Mode.

A3	Burst Type
0	Sequential
1	Interleave

—Addressing Sequence of Sequential Mode

An internal column address is performed by increasing the address from the column address which is input to the device.The internal column address is varied by the Burst Length as shown in the following table.When the value of column address,(n +m),in the table is larger than 255,only the least significant 8 bits are effective.

Data n	0	1	2	3	4	5	6	7	-	255	256	257	-
Column Address	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7	-	n+255	n	n+1	-
Burst Length	2 words:												
	4 words:												
	8 words:												
	Full Page: Column address is repeated until terminated.												

- Addressing Sequence of Interleave Mode

A column access is started in the input column address and is performed by inverting the address bits in the sequence shown in the following table.

Data n	Column Address								Burst Length	
Data 0	A7	A6	A5	A4	A3	A2	A1	A0	4 words	8 words
Data 1	A7	A6	A5	A4	A3	A2	A1	A0#		
Data 2	A7	A6	A5	A4	A3	A2	A1#	A0		
Data 3	A7	A6	A5	A4	A3	A2	A1#	A0#		
Data 4	A7	A6	A5	A4	A3	A2#	A1	A0		
Data 5	A7	A6	A5	A4	A3	A2#	A1	A0#		
Data 6	A7	A6	A5	A4	A3	A2#	A1#	A0		
Data 7	A7	A6	A5	A4	A3	A2#	A1#	A0#		

- CAS#Latency Field (A6~A4)

This field specifies the number of clock cycles from the assertion of the Read command to the first read data.The minimum whole value of CAS#Latency depends on the frequency of CLK.The minimum whole value satisfying the following formula must be programmed into this field.

$t_{CAC}(min) <= CAS\#Latency \times t_{CK}$

A6	A5	A4	CAS#Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 clocks
0	1	1	3 clocks
1	X	X	Reserved

- Test Mode field (A8~A7)

  These two bits are used to enter the test mode and must be programmed to “00”in normal operation.

A8	A7	Test Mode
0	0	normal mode
0	1	Vendor Use Only
1	X	Vendor Use Only

- Write Burst Length (A9)

This bit is used to select the burst write length.

A9	Write Burst Length
0	Burst
1	Single Bit

8 No-Operation command

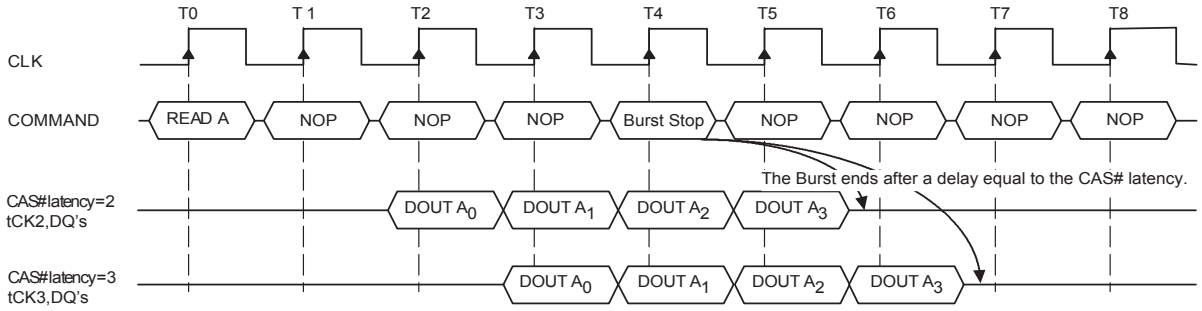
(RAS#=”H”,CAS#=”H”,WE#=”H”)

The No-Operation command is used to perform a NOP to the SDRAM which is selected (CS# is Low).This prevents unwanted commands from being registered during idle or wait states.

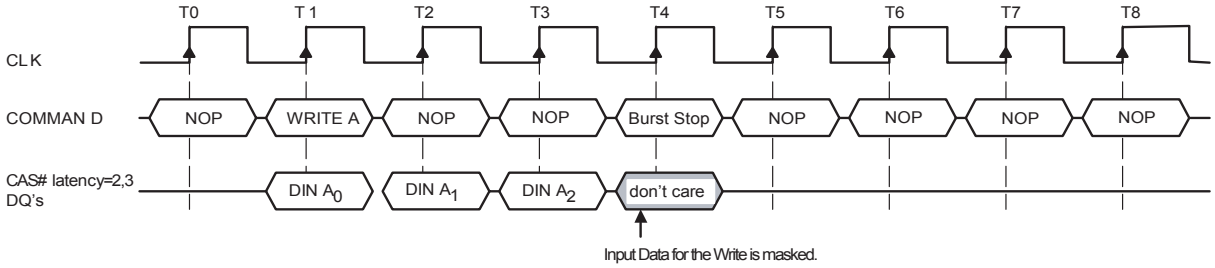
9 Burst Stop command

(RAS#=”H”,CAS#=”H”,WE#=”L”)

The Burst Stop command is used to terminate either fixed-length or full-page bursts.This command is only effective in a read/write burst without the auto precharge function.The terminated read burst ends after a delay equal to the CAS#latency (refer to the following figure).The termination of a write burst is shown in the following figure.



Termination of a Burst Read Operation (Burst Length **> 4**,CAS#Latency =2,3)



Termination of a Burst Write Operation (Burst Length =X)

10 Device Deselect command (CS#=”H”)

The Device Deselect command disables the command decoder so that the RAS#,CAS#,WE# and Address inputs are ignored,regardless of whether the CLK is enabled.This command is similar to the No Operation command.

11 AutoRefresh command

(RAS#=”L”,CAS#=”L”,WE#=”H”,CKE =”H”)

The AutoRefresh command is used during normal operation of the SDRAM and is analogous to CAS#-before-RAS#(CBR)Refresh in conventional DRAMs.This command is non-persistent,so it must be issued each time a refresh is required.The addressing is generated by the internal refresh controller.This makes the address bits a “don ’t care”during an AutoRefresh command.The internal refresh counter increments automatically on every auto refresh cycle to all of the rows.The refresh operation must be performed 4096 times within 64ms.The time required to complete the auto refresh operation is specified by tRC(min.).To provide the AutoRefresh command, all banks need to be in the idle state and the device must not be in power down mode (CKE is high in the previous cycle).This command must be followed by NOPs until the auto refresh operation is completed.The precharge time requirement,tRP(min),must be met before successive auto refresh operations are performed.

12 SelfRefresh Entry command

(RAS#=”L”,CAS#=”L”,WE#=”H”,CKE =”L”)

The SelfRefresh is another refresh mode available in the SDRAM.It is the preferred refresh mode for data retention and low power operation.Once the SelfRefresh command is registered,all the inputs to the SDRAM become “don ’t care”with the exception of CKE,which must remain LOW.The refresh addressing and timing is internally generated to reduce power consumption.The SDRAM may remain in SelfRefresh mode for an indefinite period. The SelfRefresh mode is exited by restarting the external clock and then asserting HIGH on CKE (SelfRefresh Exit command).

13 SelfRefresh Exit command

(CKE =”H”,CS#=”H”or CKE =”H”,RAS#=”H”,CAS#=”H”,WE#=”H”)

This command is used to exit from the SelfRefresh mode.Once this command is registered, NOP or Device Deselect commands must be issued for tRC(min.)because time is required for the completion of any bank currently being internally refreshed.If auto refresh cycles in bursts are performed during normal operation,a burst of 4096 auto refresh cycles should be completed just prior to entering and just after exiting the SelfRefresh mode.

14 Clock Suspend Mode Entry /PowerDown Mode Entry command (CKE =”L”)

When the SDRAM is operating the burst cycle,the internal CLK is suspended(masked)from the subsequent cycle by issuing this command (asserting CKE “LOW”).The device operation is held intact while CLK is suspended.On the other hand,when all banks are in the idle state,this command performs entry into the PowerDown mode.All input and output buffers (except the CKE buffer)are turned off in the PowerDown mode.The device may not remain in the Clock Suspend or PowerDown state longer than the refresh period (64ms)since the command does not perform any refresh operations.

15 Clock Suspend Mode Exit /PowerDown Mode Exit command

When the internal CLK has been suspended,the operation of the internal CLK is einitiated from the subsequent cycle by providing this command (asserting CKE “HIGH”).When the device is in the PowerDown mode,the device exits this mode and all disabled buffers are turned on to the active state.tPDE(min.)is required when the device exits from the PowerDown mode.Any subsequent commands can be issued after one clock cycle from the end of this command.

16 Data Write /Output Enable,Data Mask /Output Disable command (DQM =”L”,”H”)

During a write cycle,the DQM signal functions as a Data Mask and can control every word of the input data.During a read cycle,the DQM functions as the controller of output buffers.DQM is also used for device selection,byte selection and bus control in a memory system.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters	Rating	Unit
V_{DD}	Supply Voltage (with respect to V_{SS})	–0.5 to +4.6	V
V_{DDQ}	Supply Voltage for Output (with respect to V_{SSQ})	–0.5 to +4.6	V
V_I	Input Voltage (with respect to V_{SS})	–0.5 to V_{DD}+0.5	V
V_O	Output Voltage (with respect to V_{SSQ})	–1.0 to V_{DDQ}+0.5	V
I_O	Short circuit output current	50	mA
P_D	Power Dissipation (T_A = 25 °C)	1	W
T_{OPT}	Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:
1. Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC RECOMMENDED OPERATING CONDITIONS

(At T_A = 0 to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{DDQ}	Supply Voltage for DQ	3.0	3.3	3.6	V
V_{IH}	High Level Input Voltage (all Inputs)	2.0	—	V_{DD} + 1.2	V
V_{IL}	Low Level Input Voltage (all Inputs)	-1.2	—	+0.8	V

Notes:
1. All voltages are referenced to V_{SS} =0V
2. V_{IH}(max) for pulse width with ≤ 3ns of duration
3. V_{IL}(min) for pulse width with ≤ 3ns of duration

CAPACITANCE CHARACTERISTICS

(At T_A = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.3 ± 0.3V, V_{SS} = V_{SSQ} = 0V , unless otherwise noted)

Symbol	Parameter	Min.	Max.		Unit
			-6	-7/-8	
C_{IN}	Input Capacitance, address & control pin	2.5	3.8	5.0	pF
C_{CLK}	Input Capacitance, CLK pin	2.5	3.5	4.0	pF
$C_{I/O}$	Data Input/Output Capacitance	4.0	6.5	6.5	pF

Recommended D.C.Operating Conditions (VDD =3.3V ± 0.3V,Ta =0~70 C)

Description/Test condition		Symbol	- 6/7/8 Max.	Unit	Note
Operating Current $t_{RC} \geq t_{RC}(min)$, Outputs Open, Input signal one transition per one cycle	1 bank operation	I_{CC1}	140/130/130	mA	3
Precharge Standby Current in power down mode t_{CK} = 15ns, CKE ≤ V_{IL}(max)		I_{CC2P}	2		3
Precharge Standby Current in power down mode t_{CK} = ∞, CKE ≤ V_{IL}(max)		I_{CC2PS}	2		
Precharge Standby Current in non-power down mode t_{CK} = 15ns, CS# ≥ V_{IH}(min), CKE ≥ V_{IH} Input signals are changed once during 30ns.		I_{CC2N}	20		3
Precharge Standby Current in non-power down mode t_{CK} = ∞, CLK ≤ V_{IL}(max), CKE ≥ V_{IH}		I_{CC2NS}	10		
Active Standby Current in power down mode C KE ≤ V_{IL}(max), t_{CK} = 15ns		I_{CC3P}	7		3
Active Standby Current in power down mode CKE& CLK ≤ V_{IL}(max), t_{CK} = ∞		I_{CC3PS}	6		3
Active Standby Current in non-power down mode CKE ≥ V_{IH}(min), CS# ≥ V_{IH}(min), t_{CK} = 15ns		I_{CC3N}	30		
Active Standby Current in non-power down mode CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CK} = ∞		I_{CC3NS}	20		
Operating Current (Burst mode) t_{CK} = t_{CK}(min), Outputs Open, Multi-bank interleave		I_{CC4}	200/180/150		3, 4
Refresh Current $t_{RC} \geq t_{RC}$(min)		I_{CC5}	200/180/160		3
Self Refresh Current C KE ≤ 0.2V		I_{CC6}	0.8 (L-Version) 2		

Parameter	Description	Min.	Max.	Unit	Note
I_{IL}	Input Leakage Current (0V V_{IN} V_{DD}, All other pins not under test = 0V)	- 5	+ 5	µA	
V_{OH}	LVTTL Output "H" Level Voltage (I_{OUT} = -2mA)	2.4		V	
V_{OL}	LVTTL Output "L" Level Voltage (I_{OUT} = 2mA)		0.4	V	

Electrical Characteristics and Recommended A.C.Operating Conditions

(VDD =3.3V ± 0.3V,Ta =0~70 C)(Note:5,6,7,8)

Symbol	A.C. Parameter		- 6/7/8 Min.	- 6/7/8 Max.	Unit	Note
t_{RC}	Row cycle time (same bank)		60/70/80		ns	9
t_{RRD}	Row activate to row activate delay (different banks)		12/14/16			9
t_{RCD}	RAS# to CAS# delay (same bank)		18/21/24			9
t_{RP}	Precharge to refresh/row activate command (same bank)		18/21/24			9
t_{RAS}	Row activate to precharge time (same bank)		42/49/56	100,000		9
t_{CK2}	Clock cycle time	CL* = 2	- / - /10			
t_{CK3}		CL* = 3	6/7/8			
t_{AC2}	Access time from CLK	CL* = 2		- / - /8		9
t_{AC3}	(positive edge)	CL* = 3		5.5/5.5/6		
t_{OH}	Data output hold time		2/2.5/2.5			9
t_{CH}	Clock high time		2/3/3			10
t_{CL}	Clock low time		2/3/3			10
t_{IS}	Data/Address/Control Input set-up time		1.5/1.75/2			10
t_{IH}	Data/Address/Control Input hold time		1			10
t_{LZ}	Data output low impedance		1			9
t_{HZ}	Data output high impedance			5.5/5.5/6		8
t_{DAL}	Input data to active/refresh command delay time (During Auto-precharge)		2CLK+t_{RP}			
t_{SRX}	Exit self refresh and active command		70			
t_{RFC}	Auto refresh Period		60/70/80			
t_{REF}	Refresh cycle time(4096)			64	ms	
t_{WR}	Write Recovery Time		2		CLK	
t_{CCD}	CAS# to CAS# Delay time		1			
t_{MRS}	Mode Register Set cycle time		2			
t_{PDE}	CKE to clock enable or power down exit setup mode		1			

* CL is CAS# Latency.

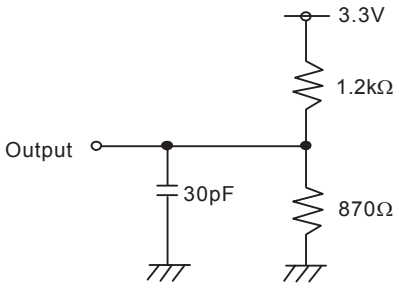
Note:

1. Stress greater than those listed under “Absolute Maximum Ratings”may cause permanent damage to the device.
2. All voltages are referenced to VSS.
3. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of tCK and tRC.Input signals are changed one time during tCK.
4. These parameters depend on the output loading.Specified values are obtained with the output open.
5. Power-up sequence is described in Note 11.

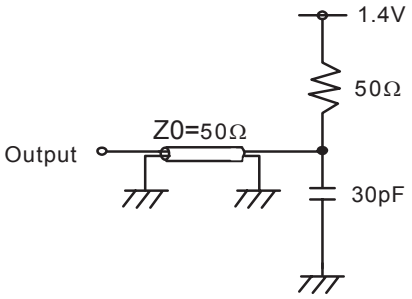
6.A.C.Test Conditions

LVTTL Interface

Reference Level of Output Signals	1.4V /1.4V
Output Load	Reference to the Under Output Load (B)
Input Signal Levels	2.4V /0.4V
Transition Time (Rise and Fall)of Input Signals	1ns
Reference Level of Input Signals	1.4V



LVTTL D.C. Test Load (A)



LVTTL A.C. Test Load (B)

7. Transition times are measured between VIH and VIL.Transition(rise and fall)of input signals are in a fixed slope (1 ns).
8. t_{HZ} defines the time in which the outputs achieve the open circuit condition and are not at reference levels.
9. If clock rising time is longer than 1 ns,(t_R /2 -0.5)ns should be added to the parameter.
10. Assumed input rise and fall time t_T (t_R &t_F)=1 ns
    If t_R or t_F is longer than 1 ns,transient time compensation should be considered,i.e.,[(tr +tf)/2 -1]ns should be added to the parameter.
11. Power up Sequence
    Power up must be performed in the following sequence.
    1) Power must be applied to V_{DD} and V_{DDQ}(simultaneously)when all input signals are held “NOP”state and both CKE =”H”and DQM =”H.”The CLK signals must be started at the same time.
    2) After power-up,a pause of 200μ seconds minimum is required.Then,it is recommended that DQM is held “HIGH”(V_{DD} levels)to ensure DQ output is in high impedance.
    3) All banks must be precharged.
    4) Mode Register Set command must be asserted to initialize the Mode register.
    5) A minimum of 2 Auto-Refresh dummy cycles must be required to stabilize the internal circuitry of the device.

Timing Waveforms

Figure 1.AC Parameters for Write Timing (Burst Length=4,CAS#Latency=2)

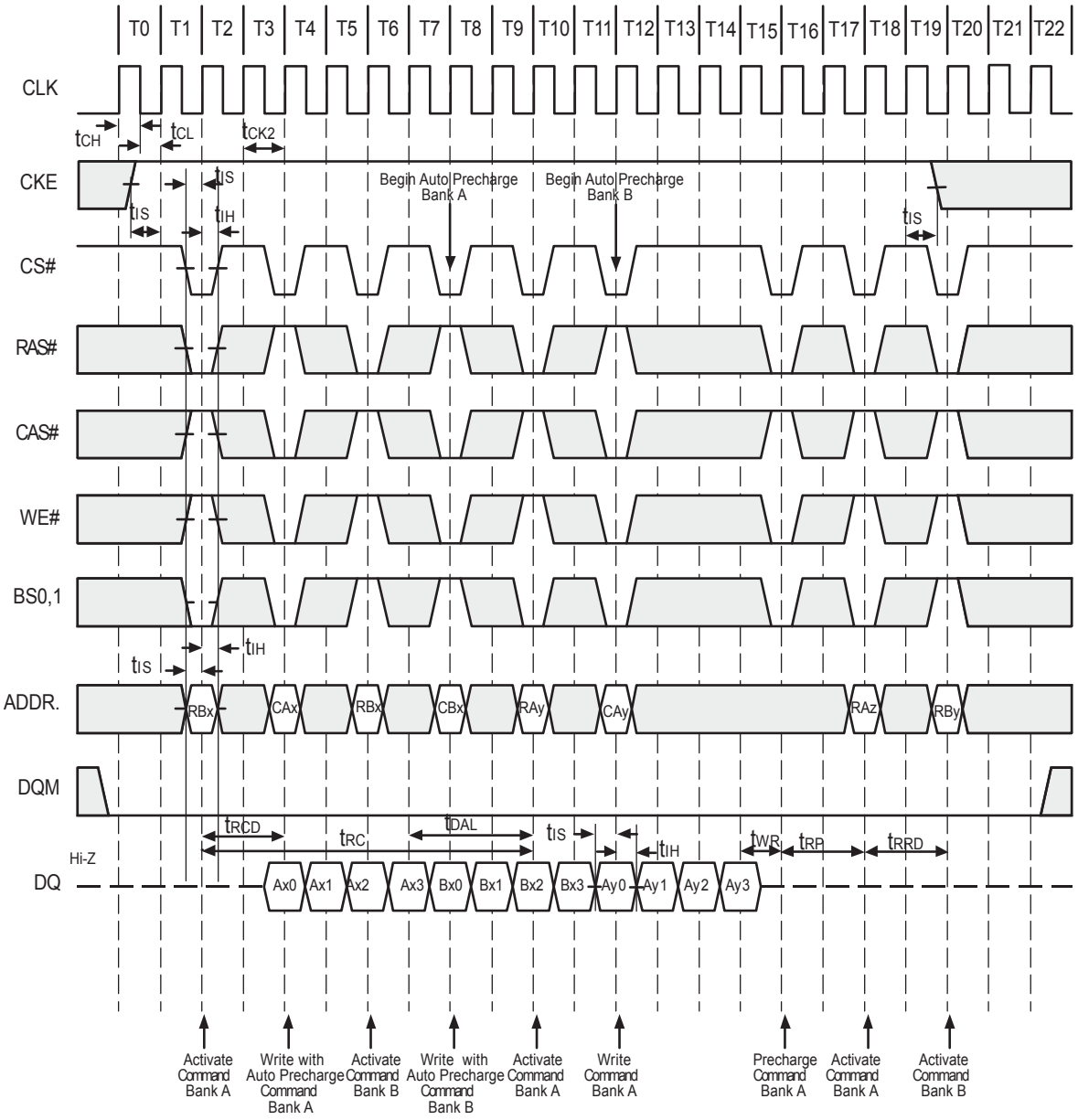


Figure 2.AC Parameters for Read Timing (Burst Length=2,CAS#Latency=2)

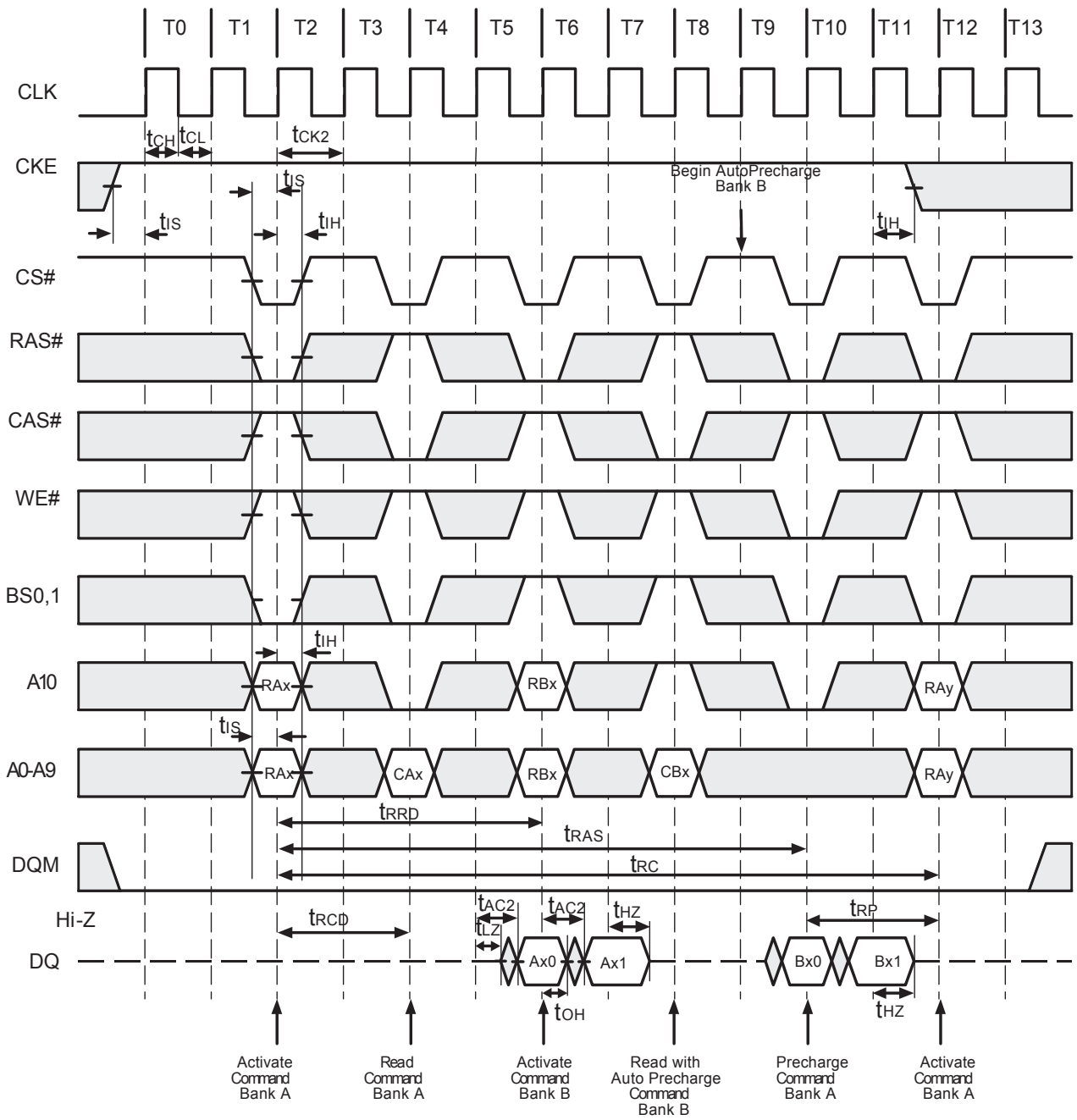


Figure 3.Auto Refresh (CBR)(Burst Length=4,CAS#Latency=2)

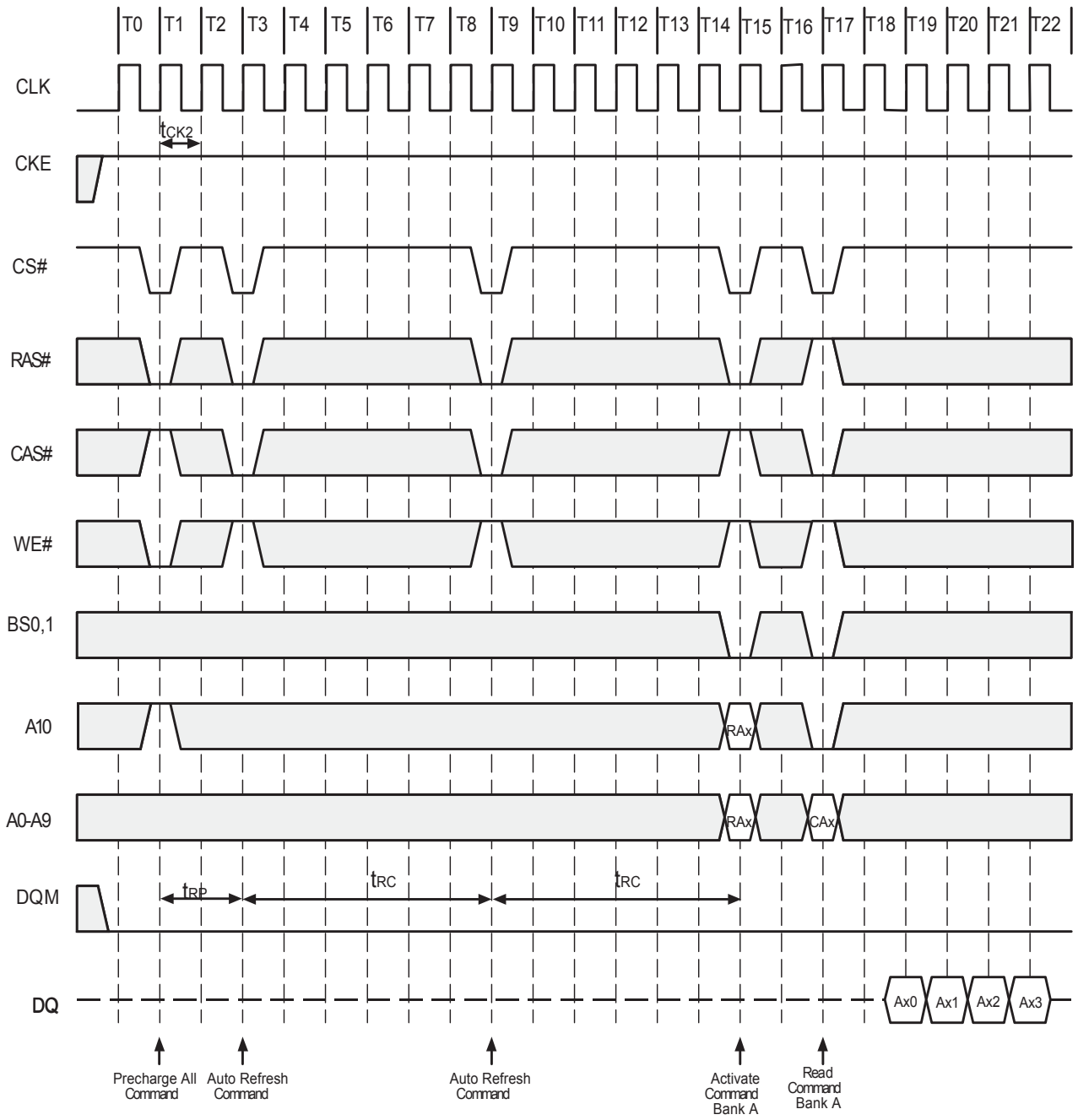


Figure 4.Power on Sequene and Auto Refresh (CBR)

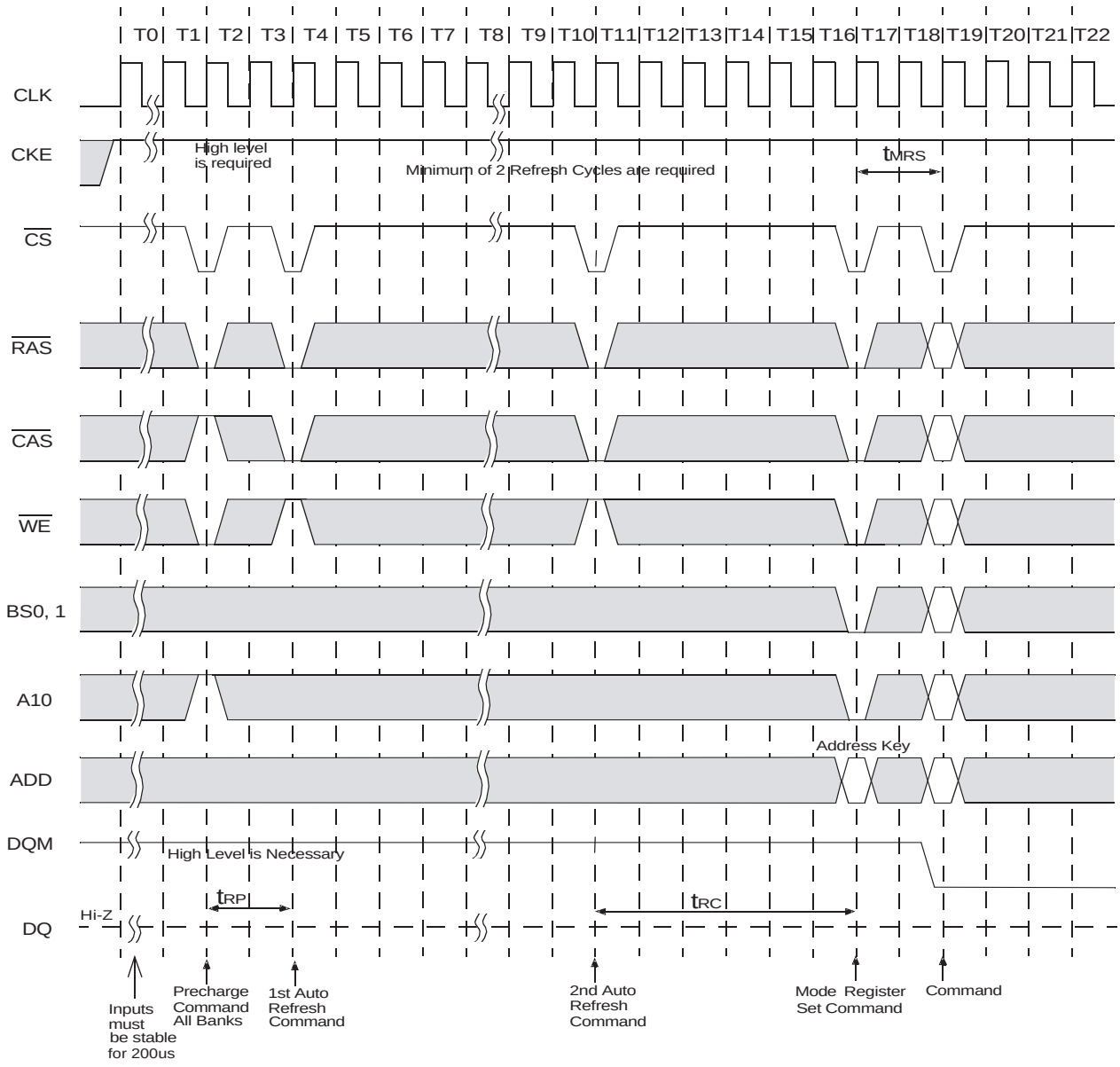
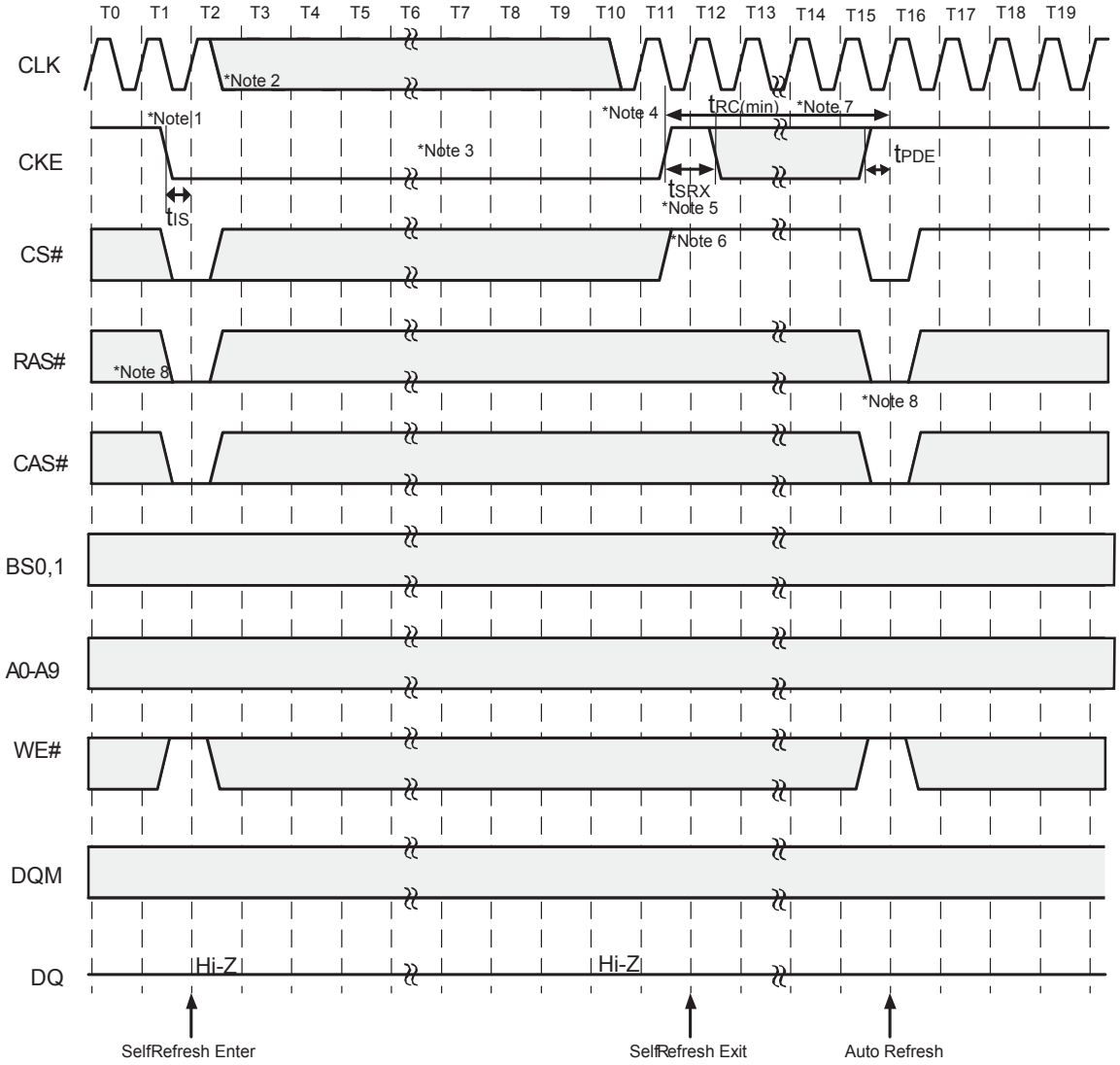


Figure 5.Self Refresh Entry &Exit Cycle



Note:To Enter SelfRefresh Mode

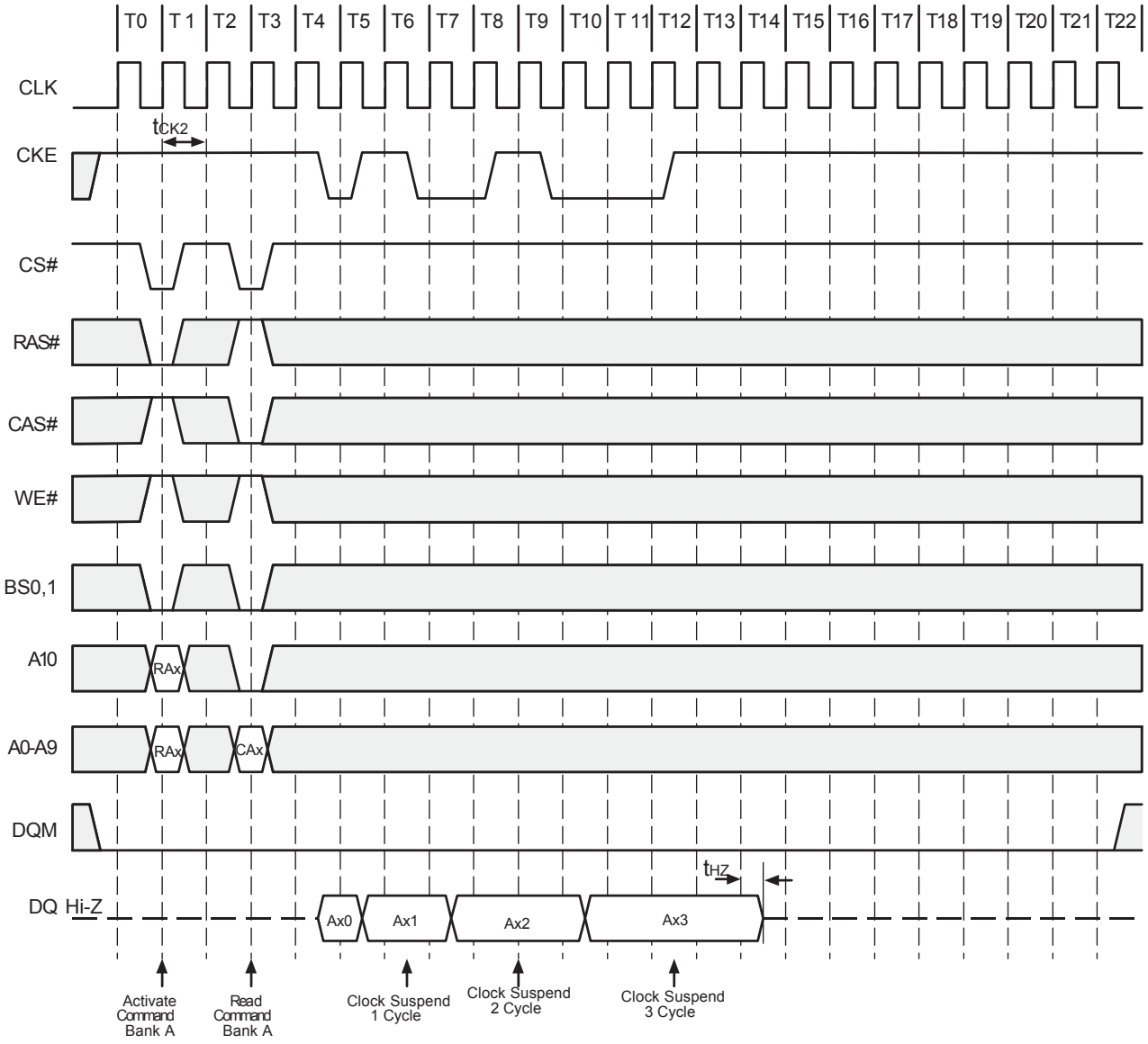
1. CS#,RAS#&CAS#with CKE should be low at the same clock cycle.
2. After 1 clock cycle,all the inputs including the system clock can be don ’t care except for CKE.
3. The device remains in SelfRefresh mode as long as CKE stays “low”.
   Once the device enters SelfRefresh mode,minimum tRAS is required before exit from SelfRefresh.

To Exit SelfRefresh Mode

4. System clock restart and be stable before returning CKE high.
5. Enable CKE and CKE should be set high for minimum time of tSRX.
6. CS#starts from high.
7. Minimum tRC is required after CKE going high to complete SelfRefresh exit.
8. 4096 cycles of burst AutoRefresh is required before SelfRefresh entry and after SelfRefresh exit if the system uses burst refresh.

Figure 6.2.Clock Suspension During Burst Read (Using CKE)

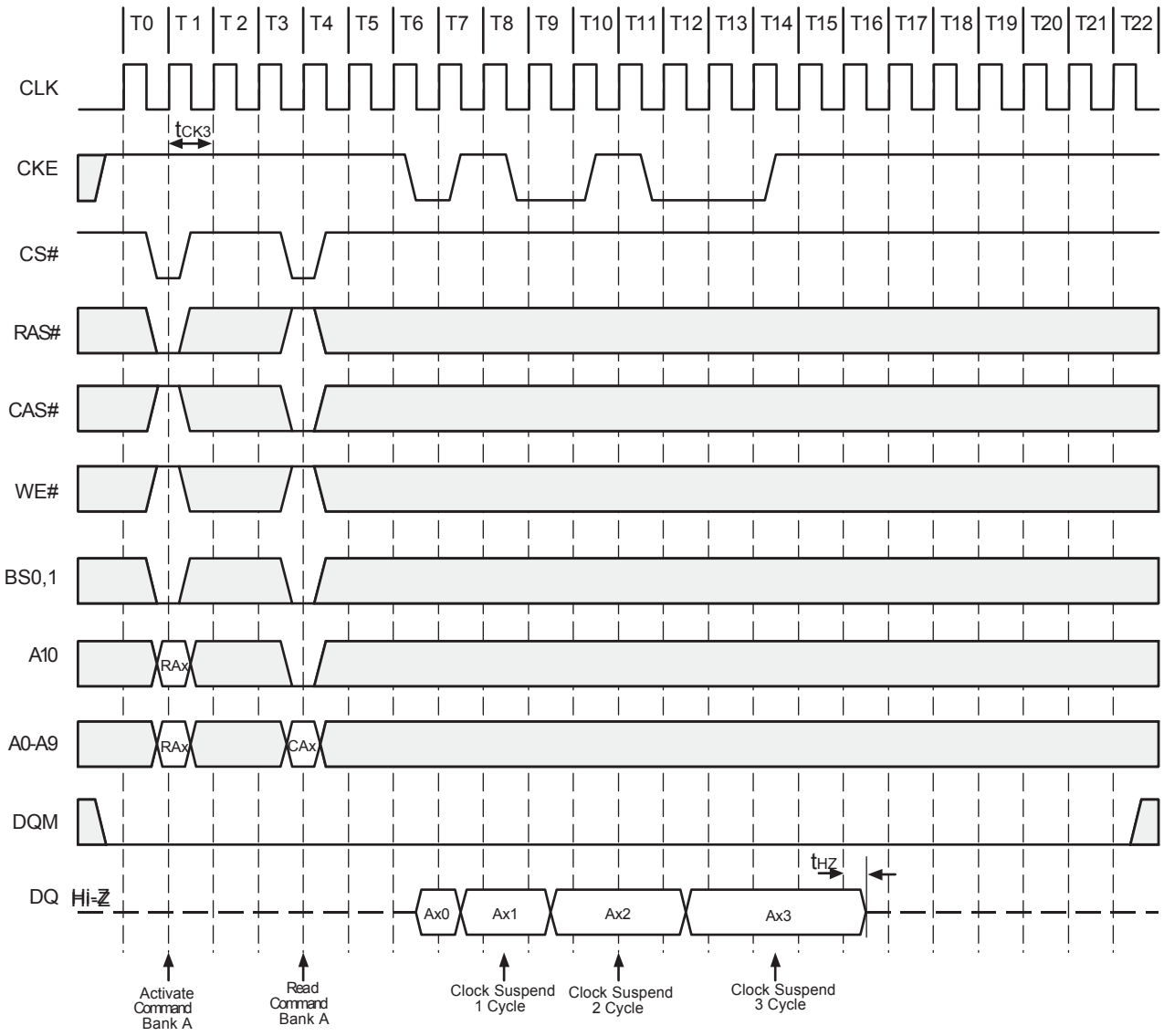
(Burst Length=4,CAS#Latency=2)



Note:CKE to CLK disable/enable =1 clock

Figure 6.3.Clock Suspension During Burst Read (Using CKE)

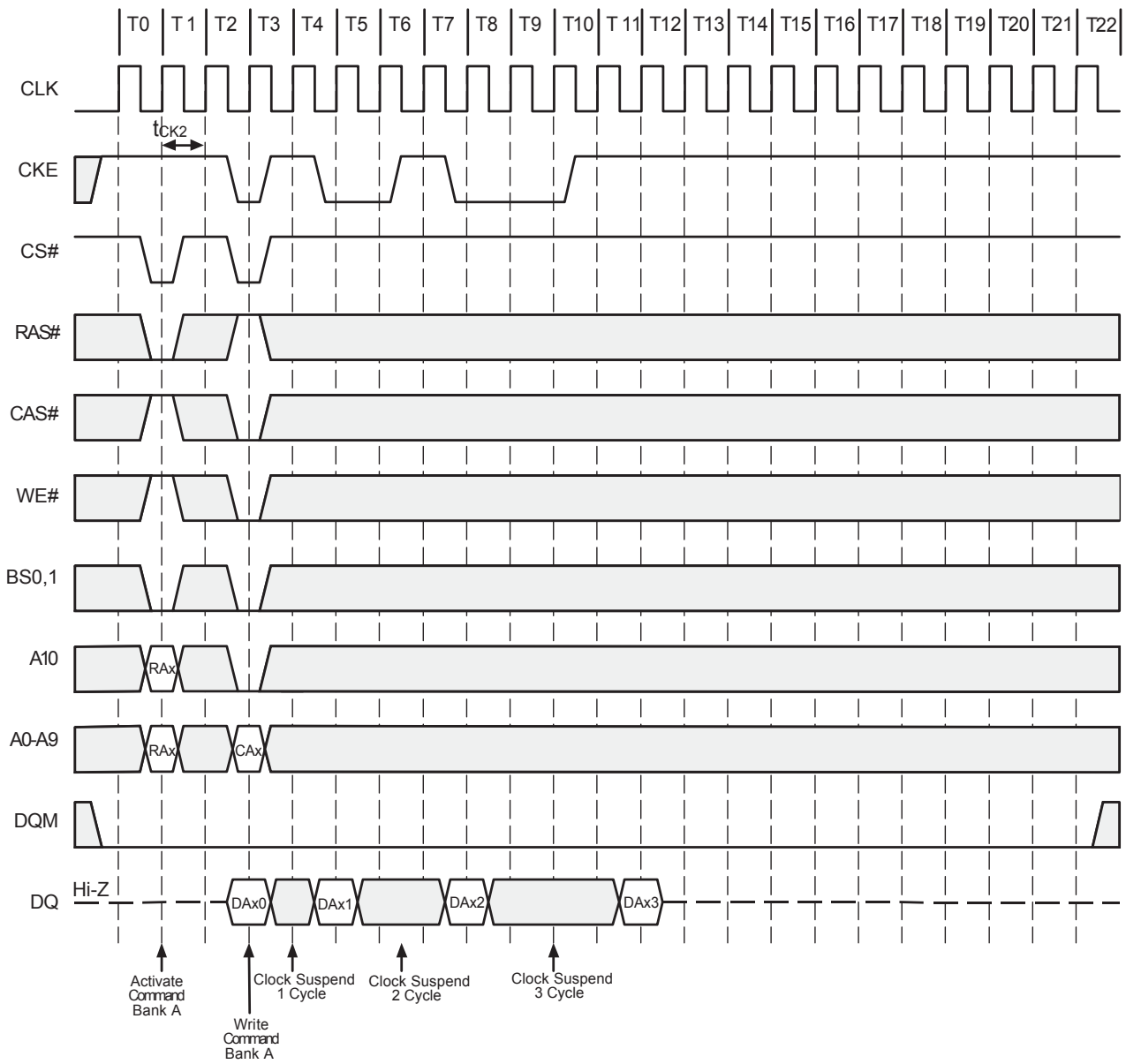
(Burst Length=4,CAS#Latency=3)



Note:CKE to CLK disable/enable =1 clock

Figure 7.2.Clock Suspension During Burst Write (Using CKE)

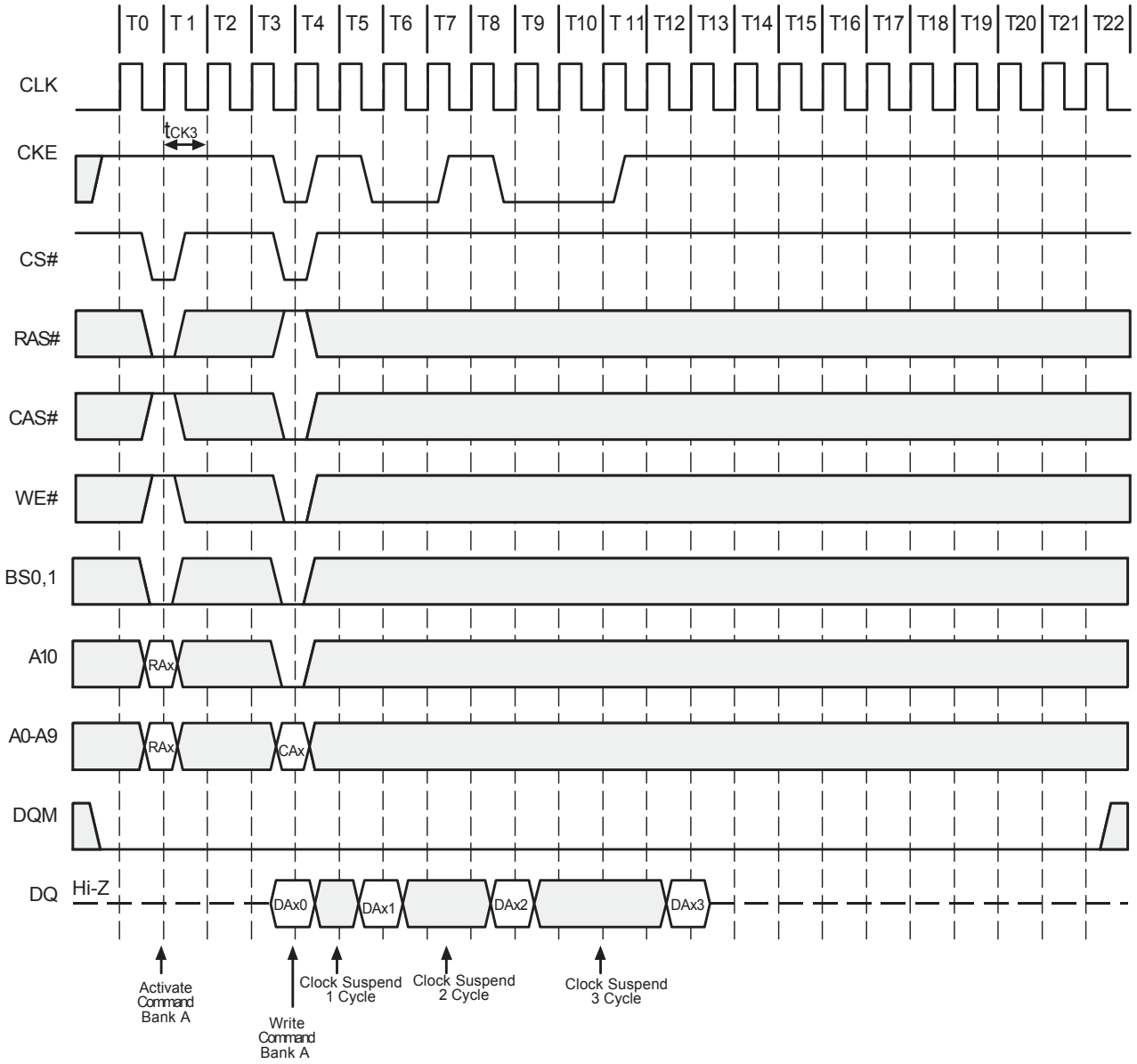
(Burst Length=4,CAS#Latency=2)



Note:CKE to CLK disable/enable =1 clock

Figure 7.3.Clock Suspension During Burst Write (Using CKE)

(Burst Length=4,CAS#Latency=3)



Note:CKE to CLK disable/enable =1 clock

Figure 8.Power Down Mode and Clock Mask (Burst Lenght=4, CAS#Latency=2)

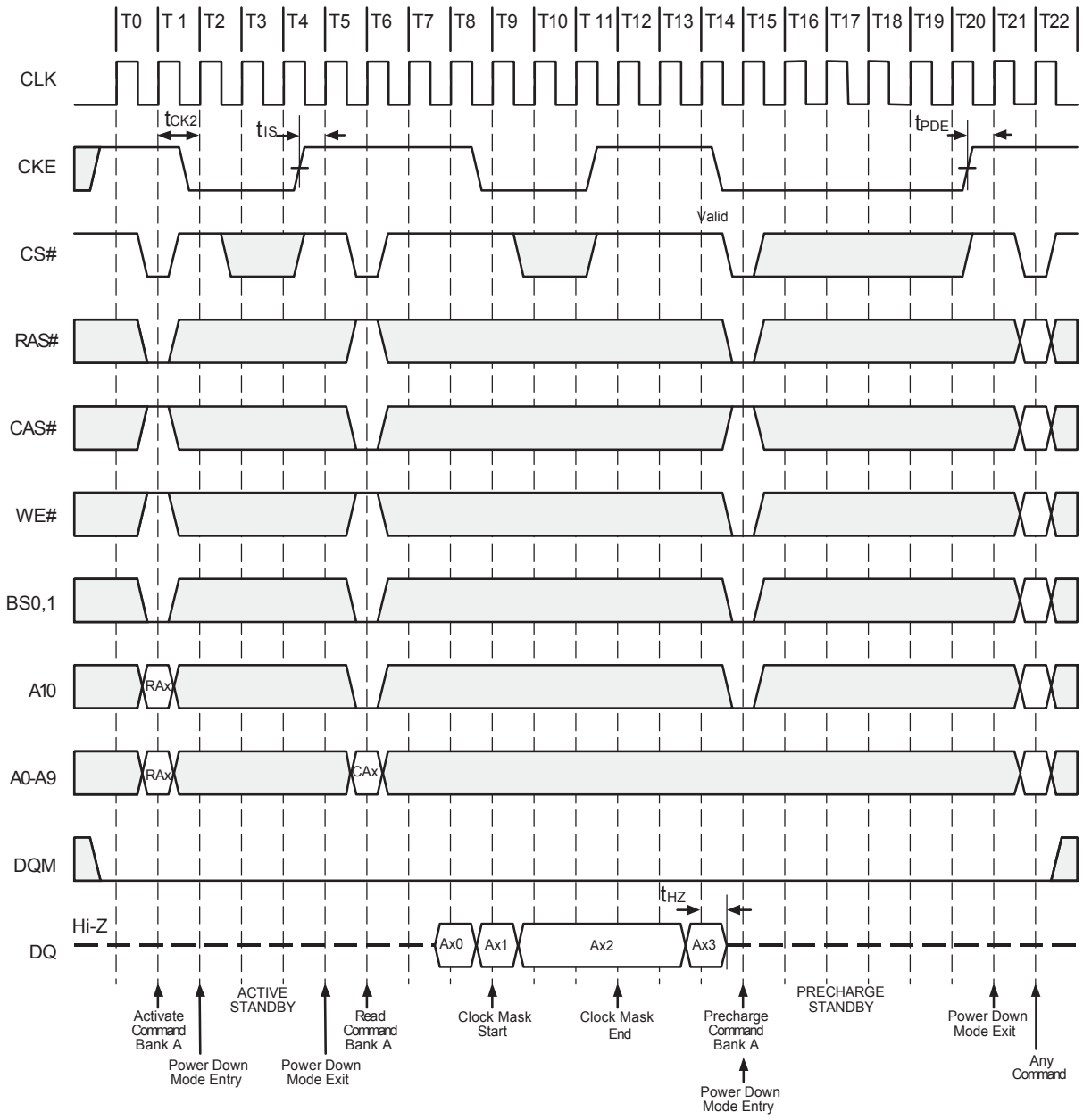


Figure 9.2.Random Column Read (Page within same Bank)

(Burst Length=4,CAS#Latency=2)

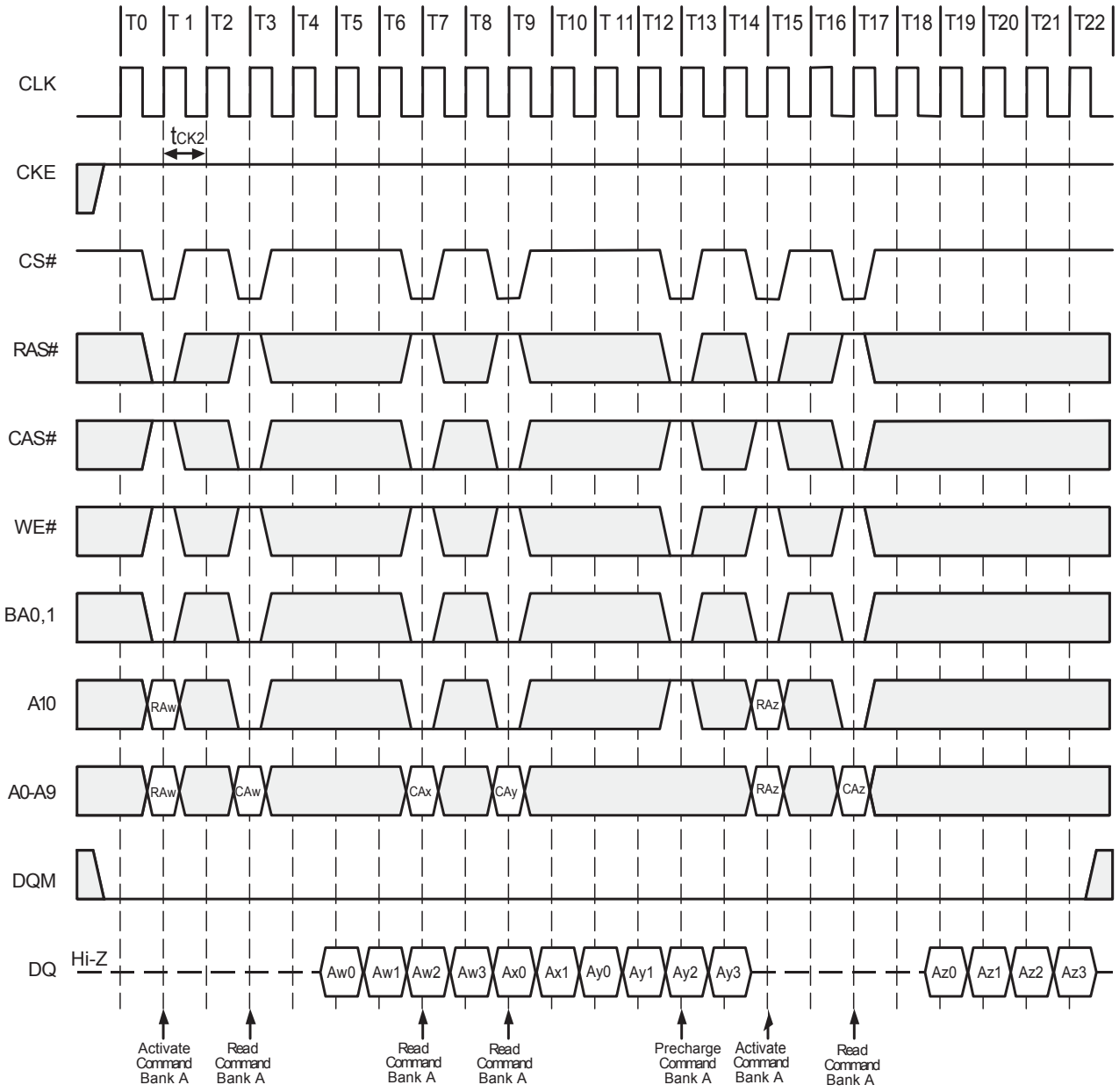


Figure 9.3.Random Column Read (Page within same Bank)

(Burst Length=4,CAS#Latency=3)

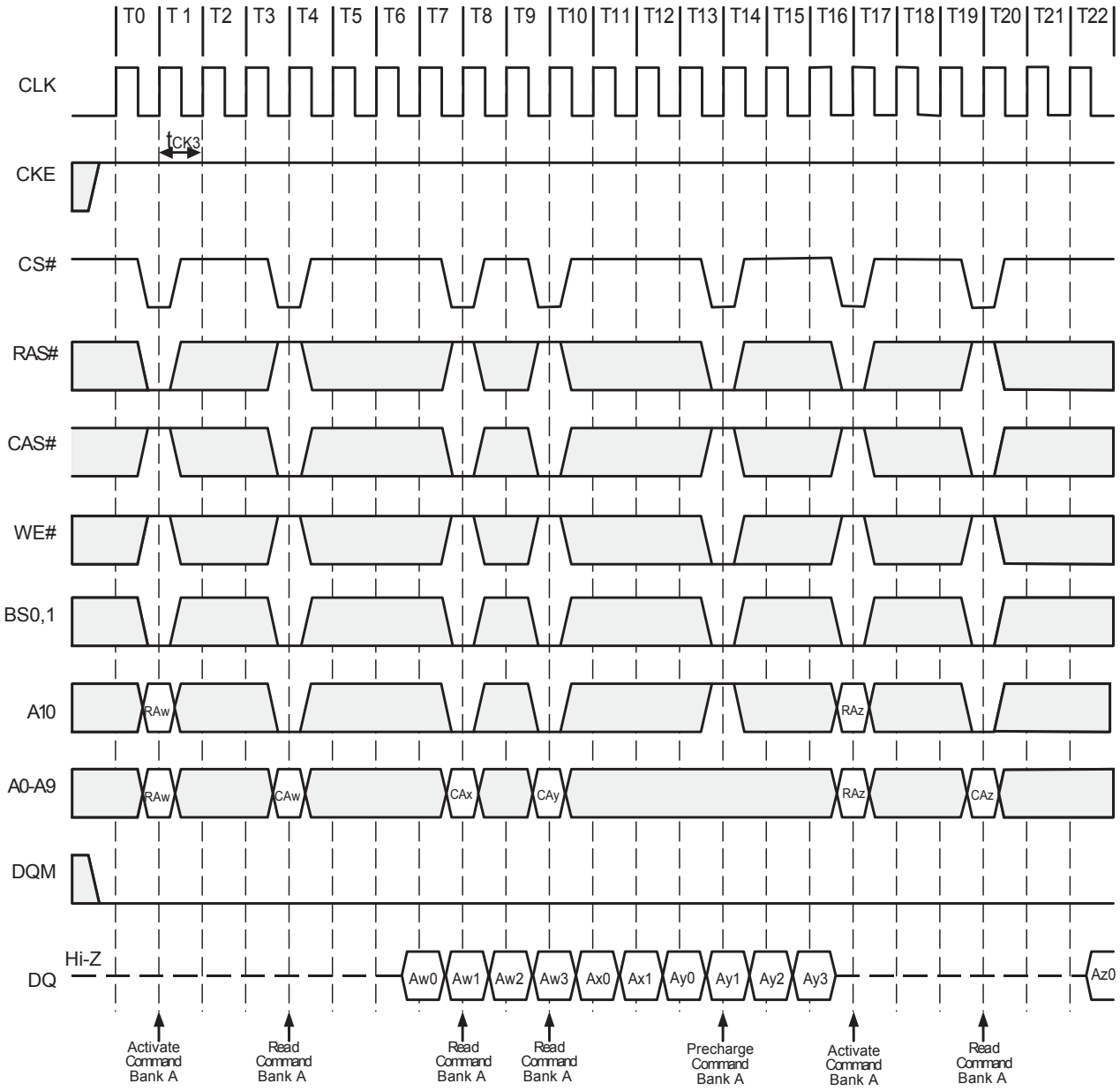


Figure 10.2.Random Column Write (Page within same Bank)

(Burst Length=4,CAS#Latency=2)

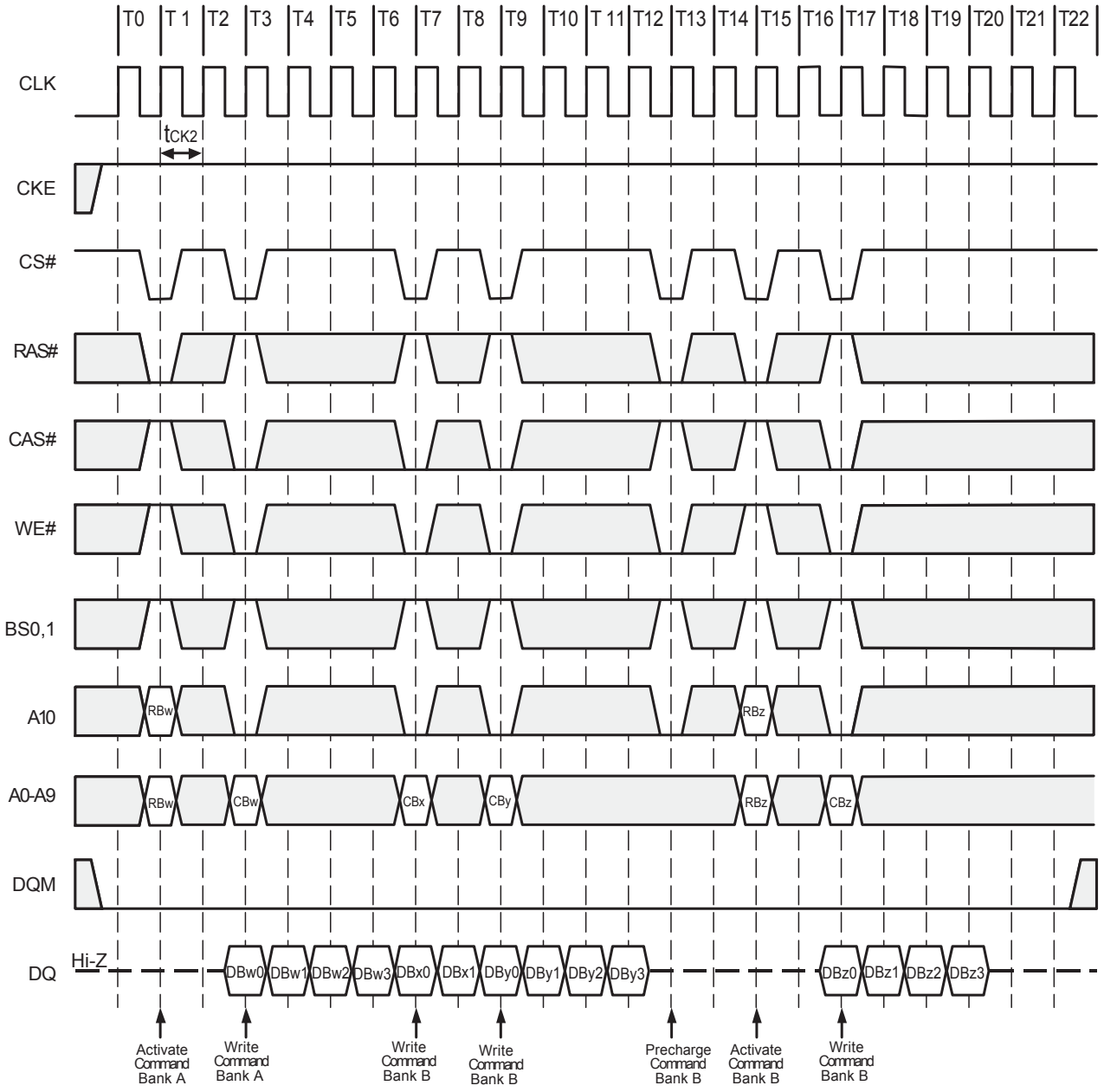


Figure 10.3.Random Column Write (Page within same Bank)

(Burst Length=4,CAS#Latency=3)

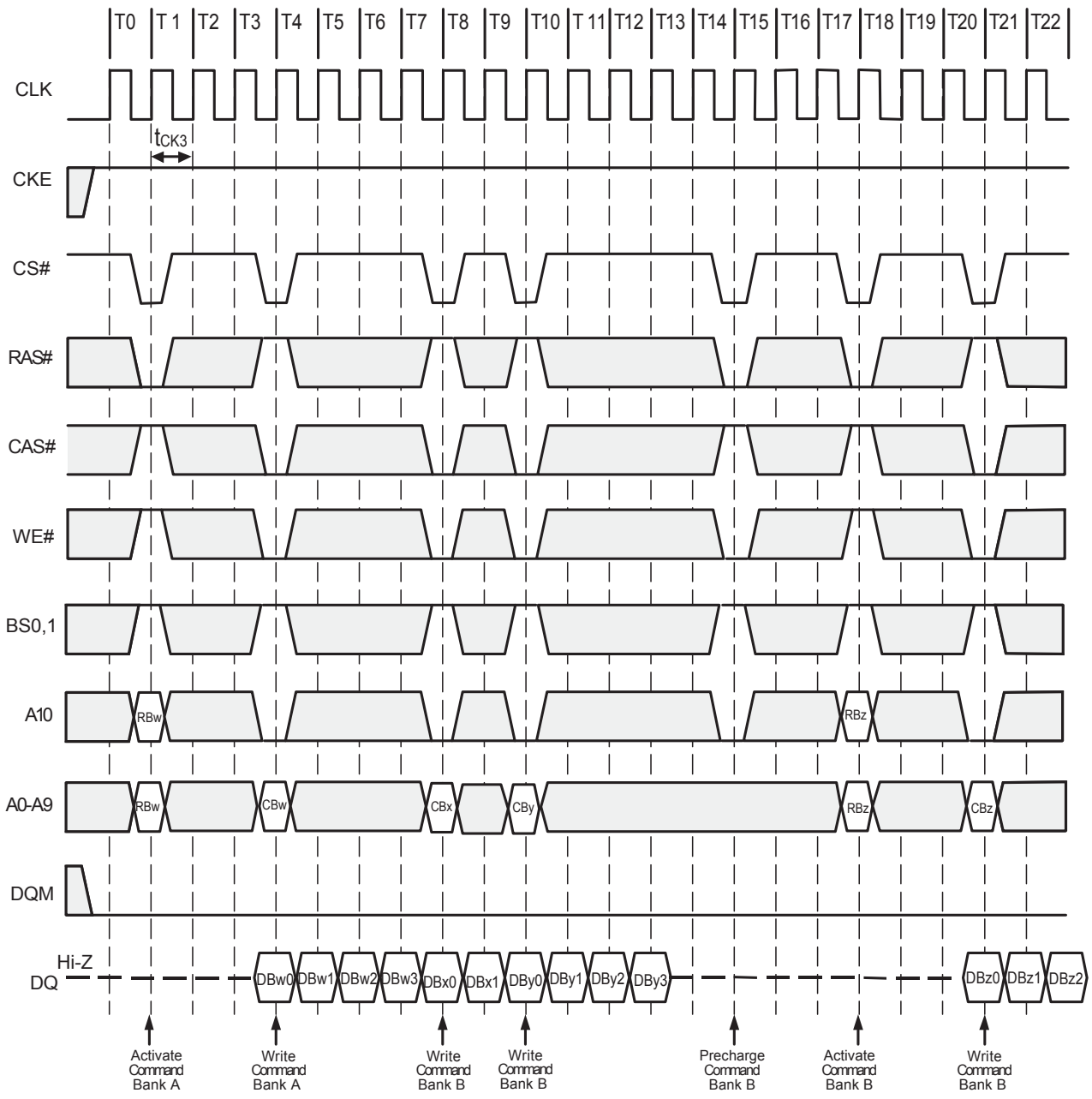


Figure 11.3.Random Row Read (Interleaving Banks)

(Burst Length=8,CAS#Latency=3)

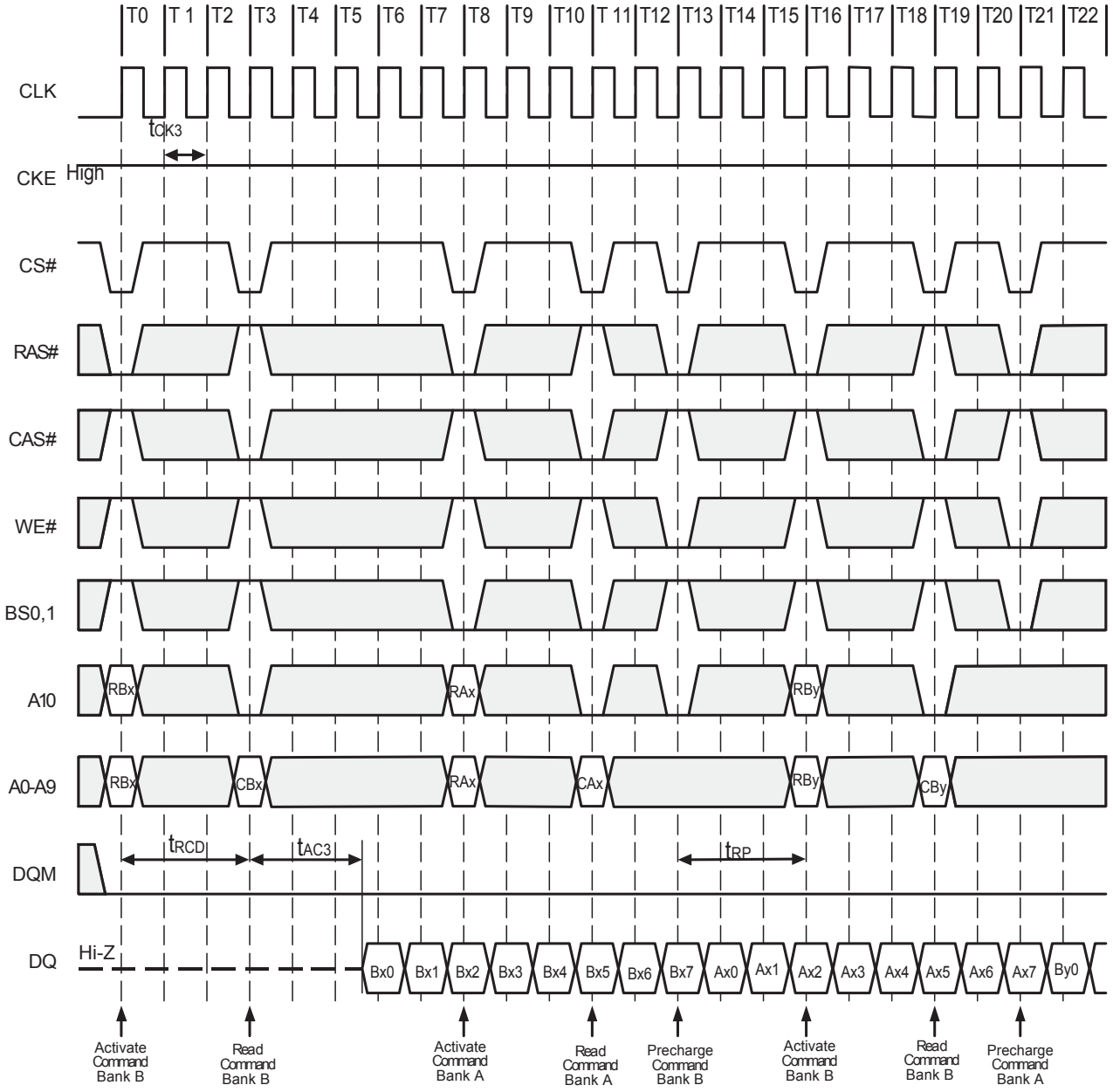


Figure 12.1.Random Row Write (Interleaving Banks)

(Burst Length=8,CAS#Latency=1)

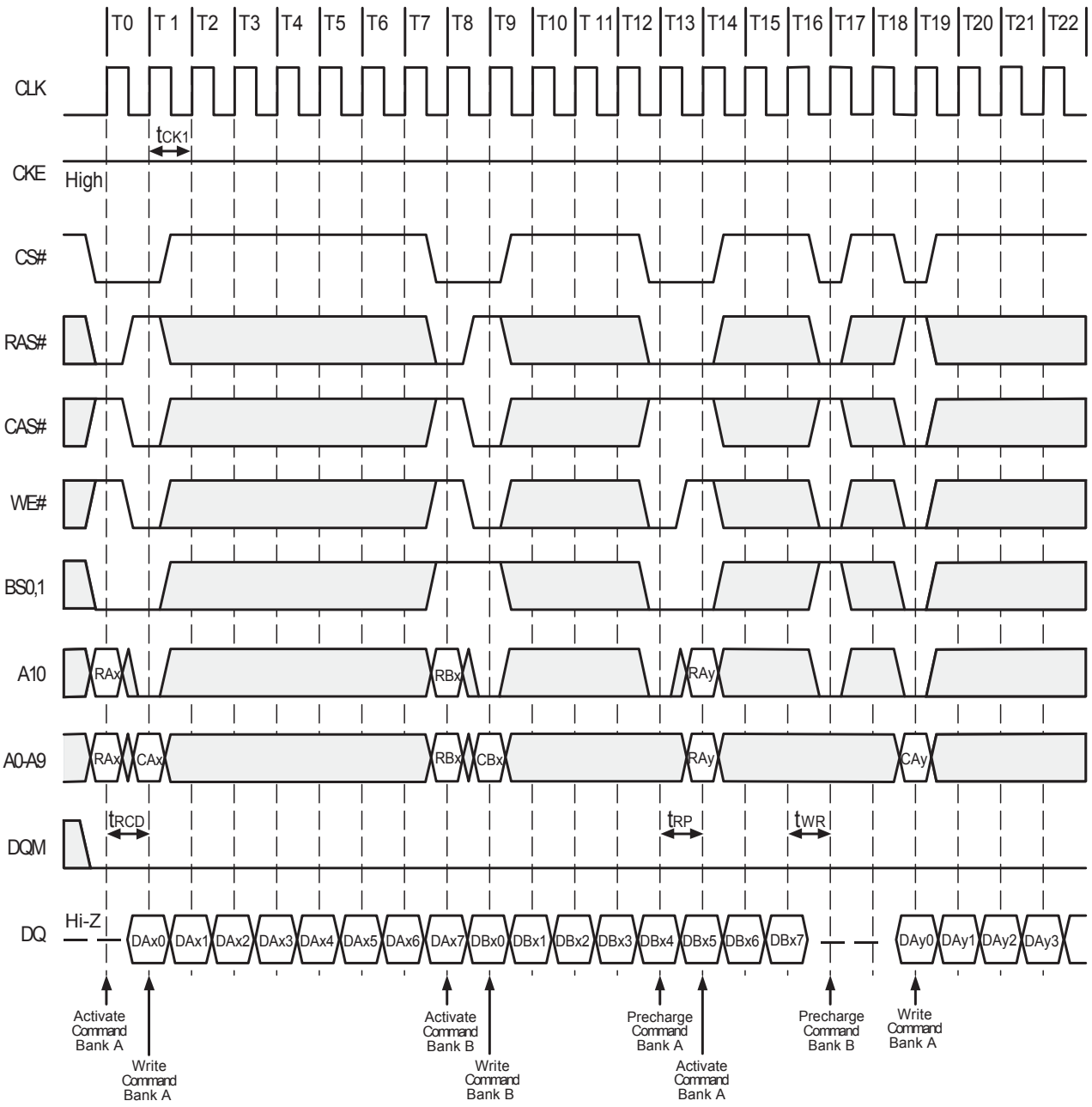
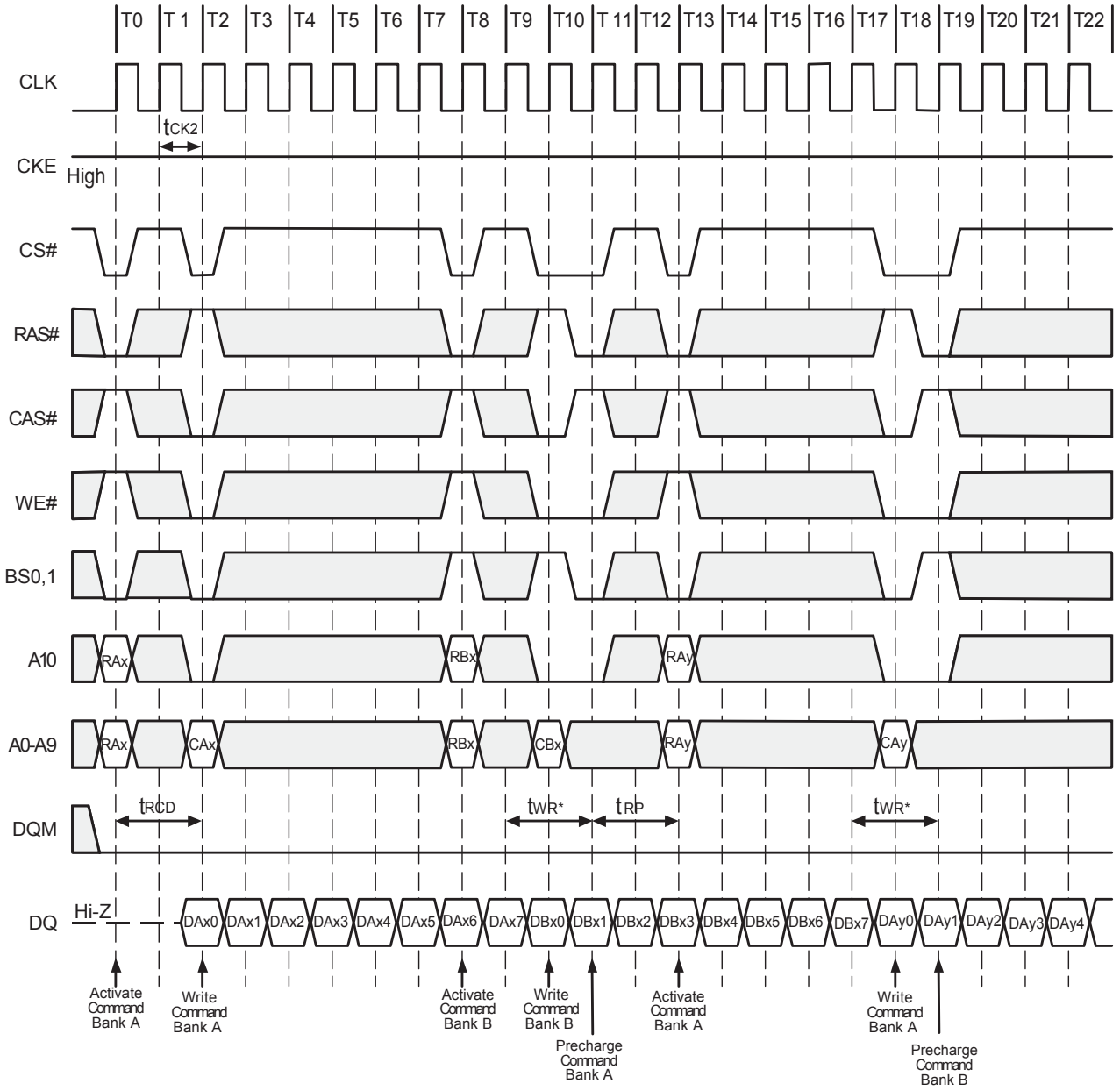


Figure 12.2.Random Row Write (Interleaving Banks)

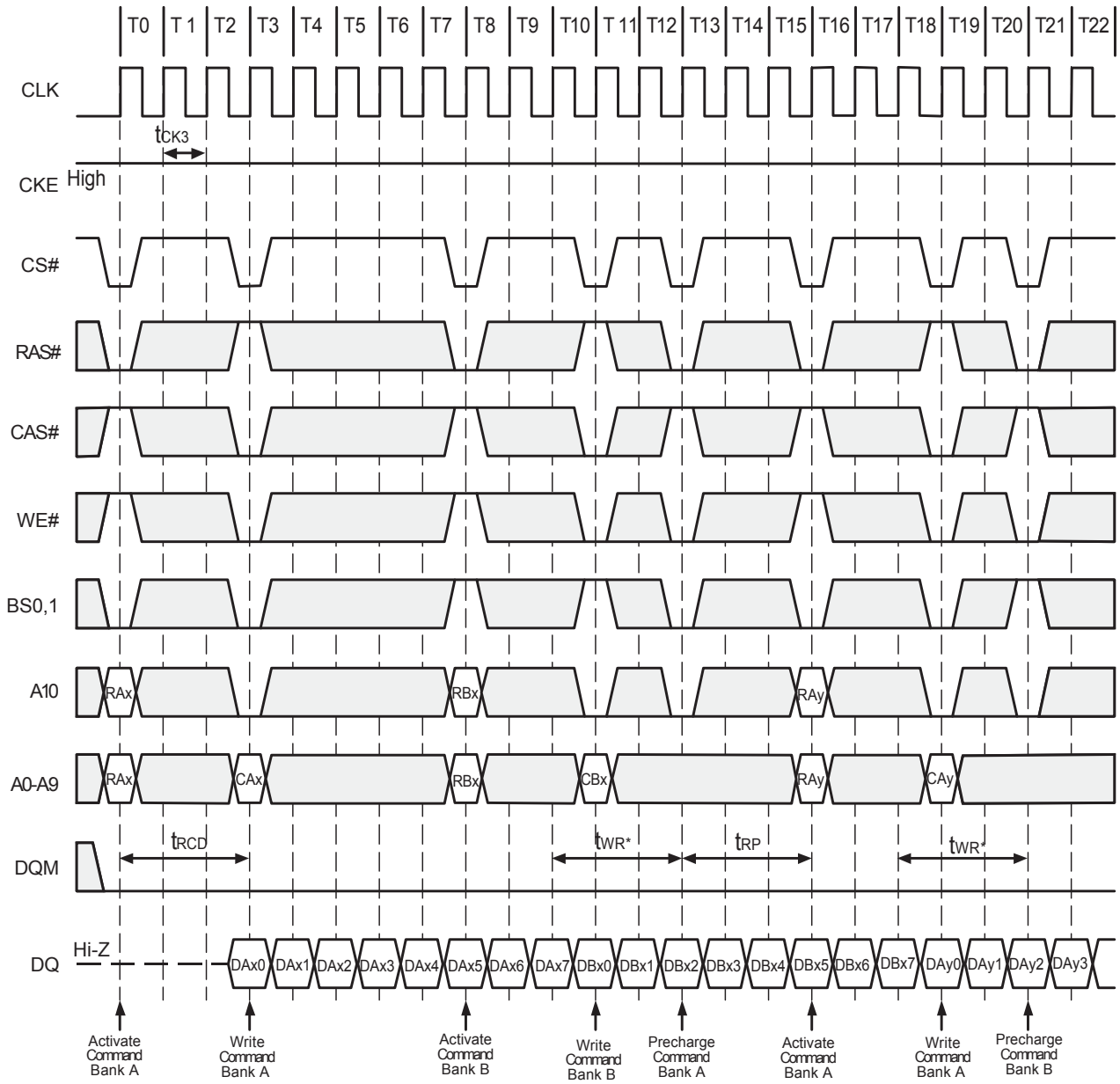
(Burst Length=8,CAS#Latency=2)



* tWR > tWR(min.)

Figure 12.3.Random Row Write (Interleaving Banks)

(Burst Length=8,CAS#Latency=3)



* $t_{WR} > t_{WR}(min.)$

Figure 13.2.Read and Write Cycle (Burst Length=4,CAS#Latency=2)

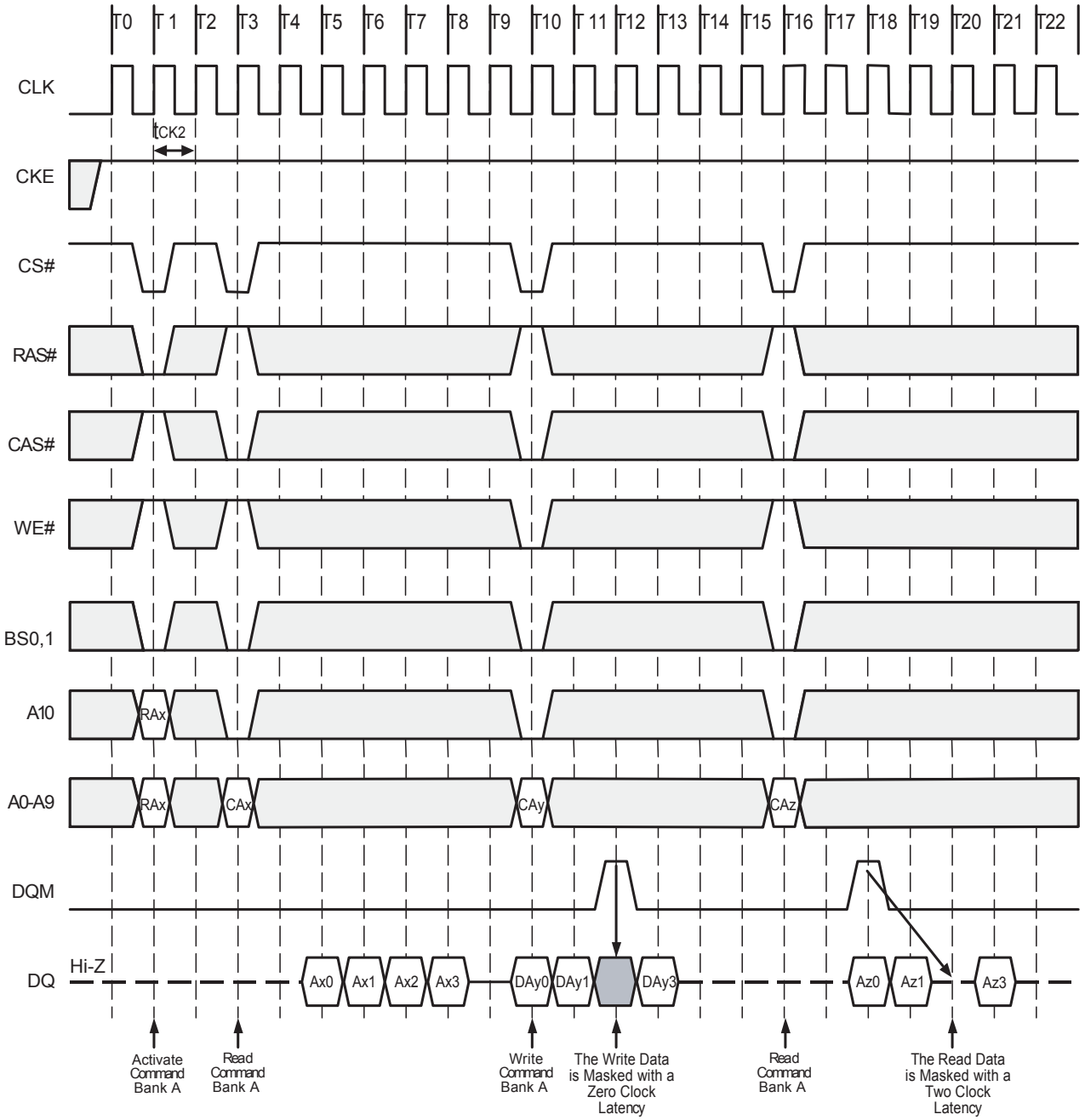


Figure 13.3.Read and Write Cycle (Burst Length=4,CAS#Latency=3)

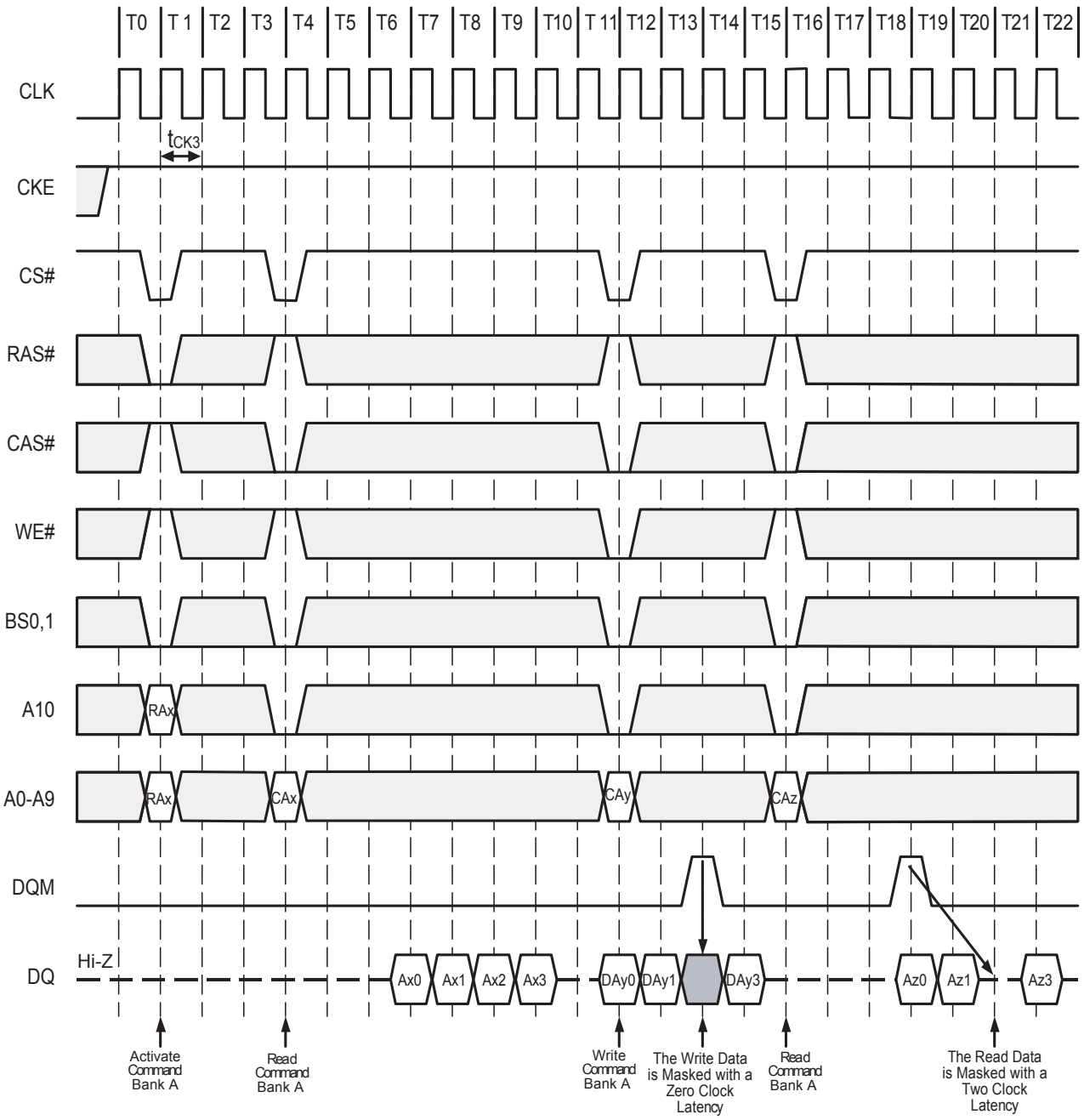


Figure 14.2.Interleaving Column Read Cycle (Burst Length=4,CAS#Latency=2)

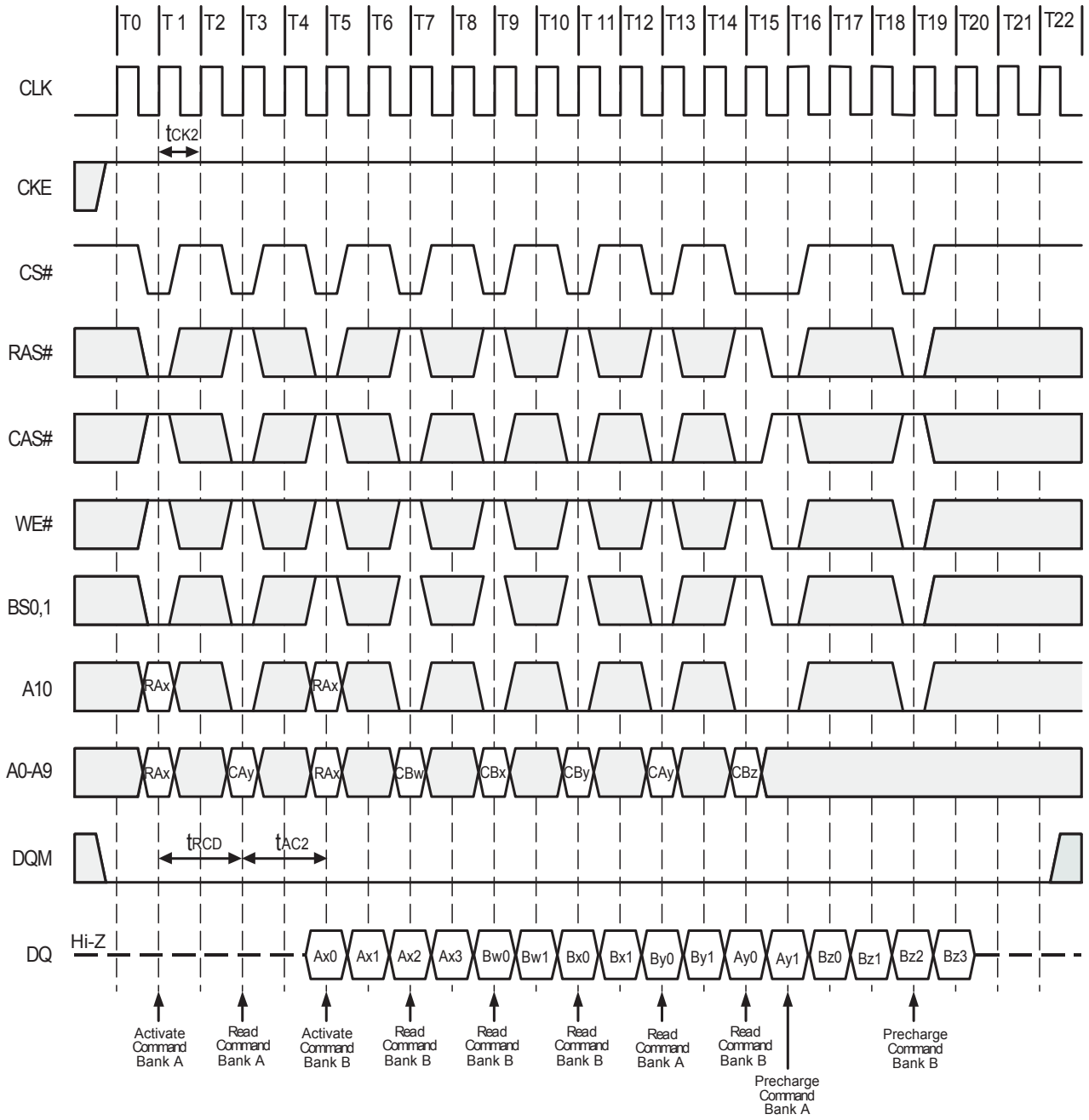


Figure 14.3.Interleaved Column Read Cycle (Burst Length=4,CAS#Latency=3)

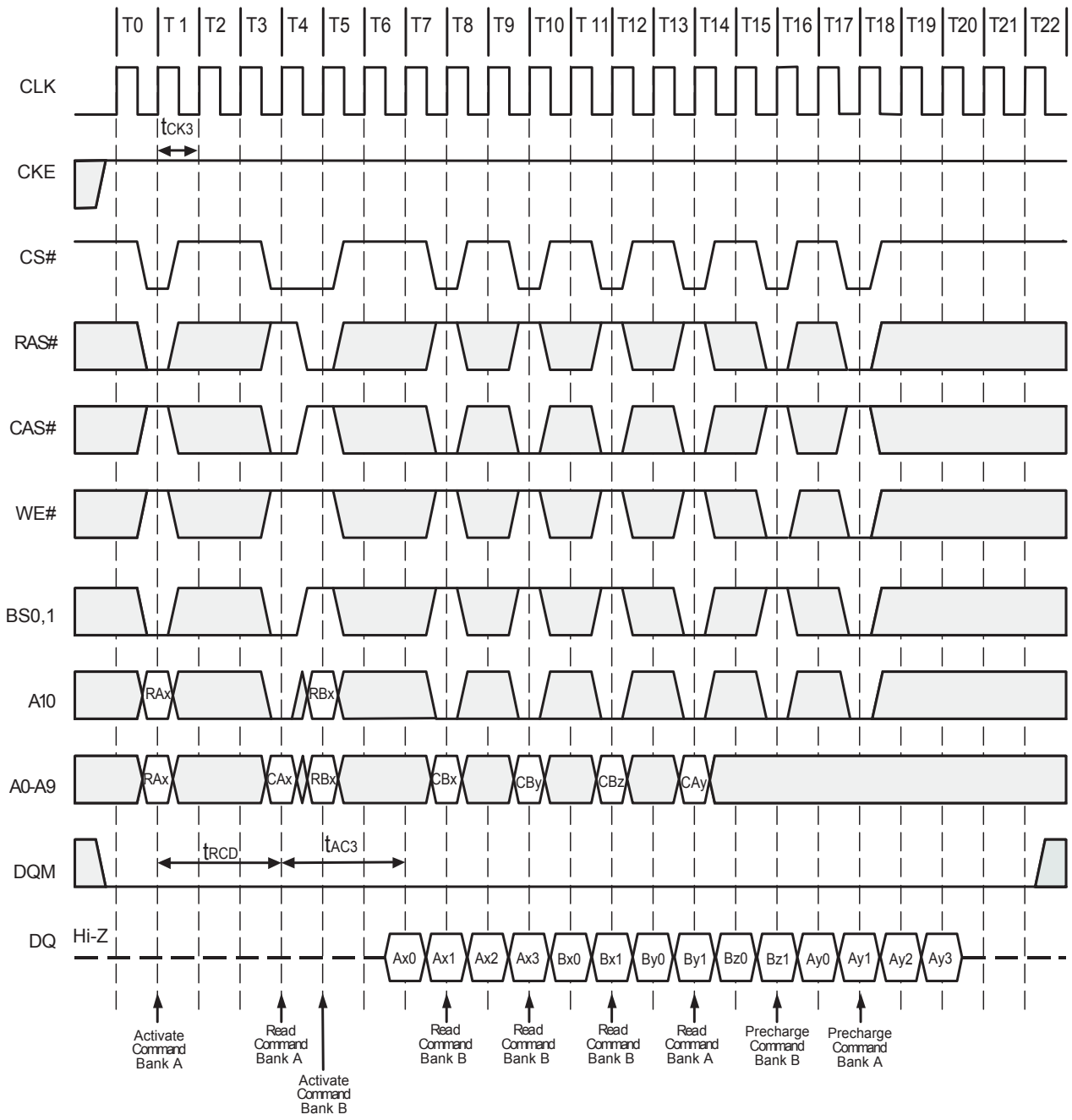


Figure 15.2.Interleaved Column Write Cycle (Burst Length=4,CAS#Latency=2)

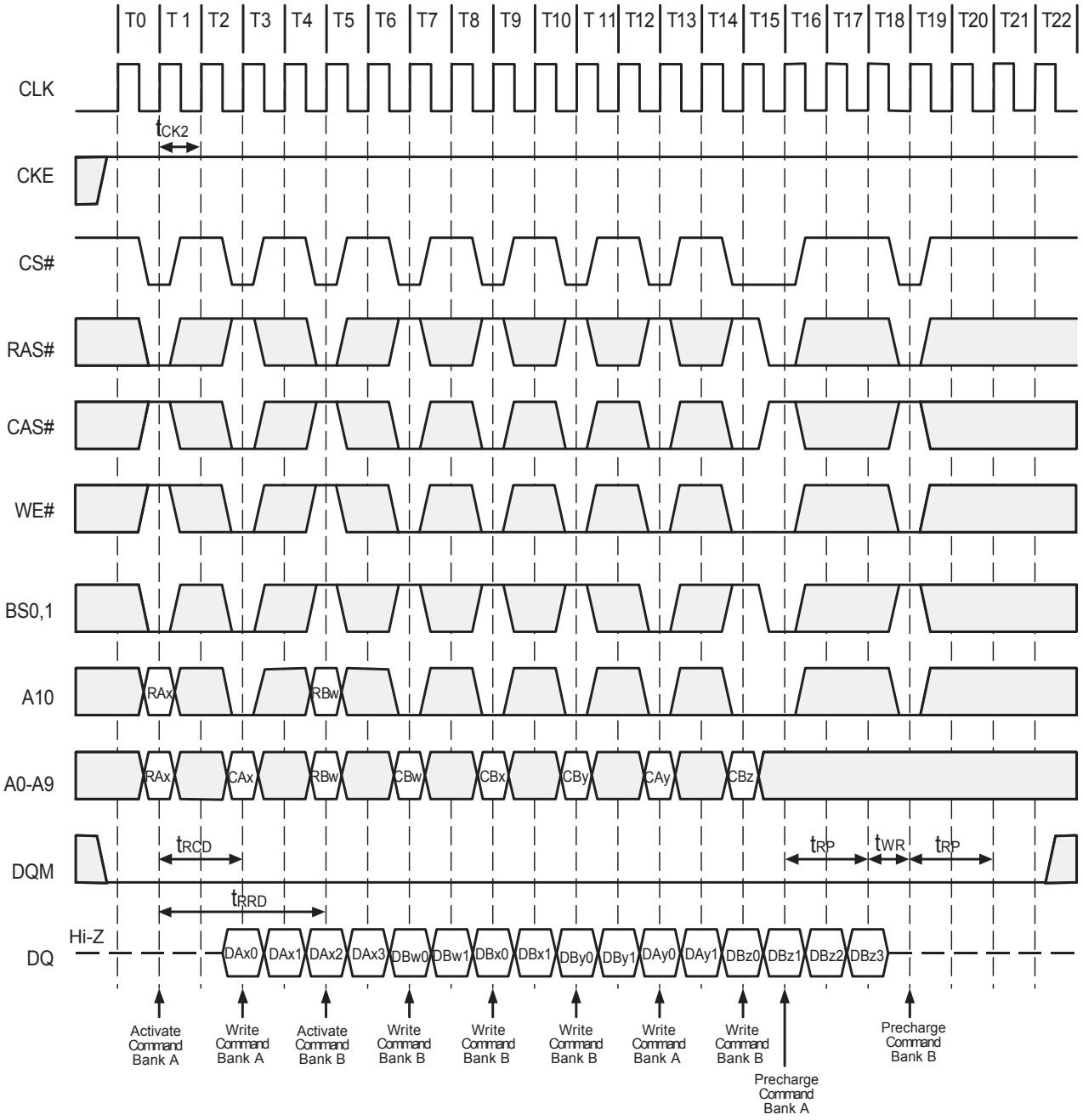


Figure 15.3.Interleaved Column Write Cycle (Burst Length=4,CAS#Latency=3)

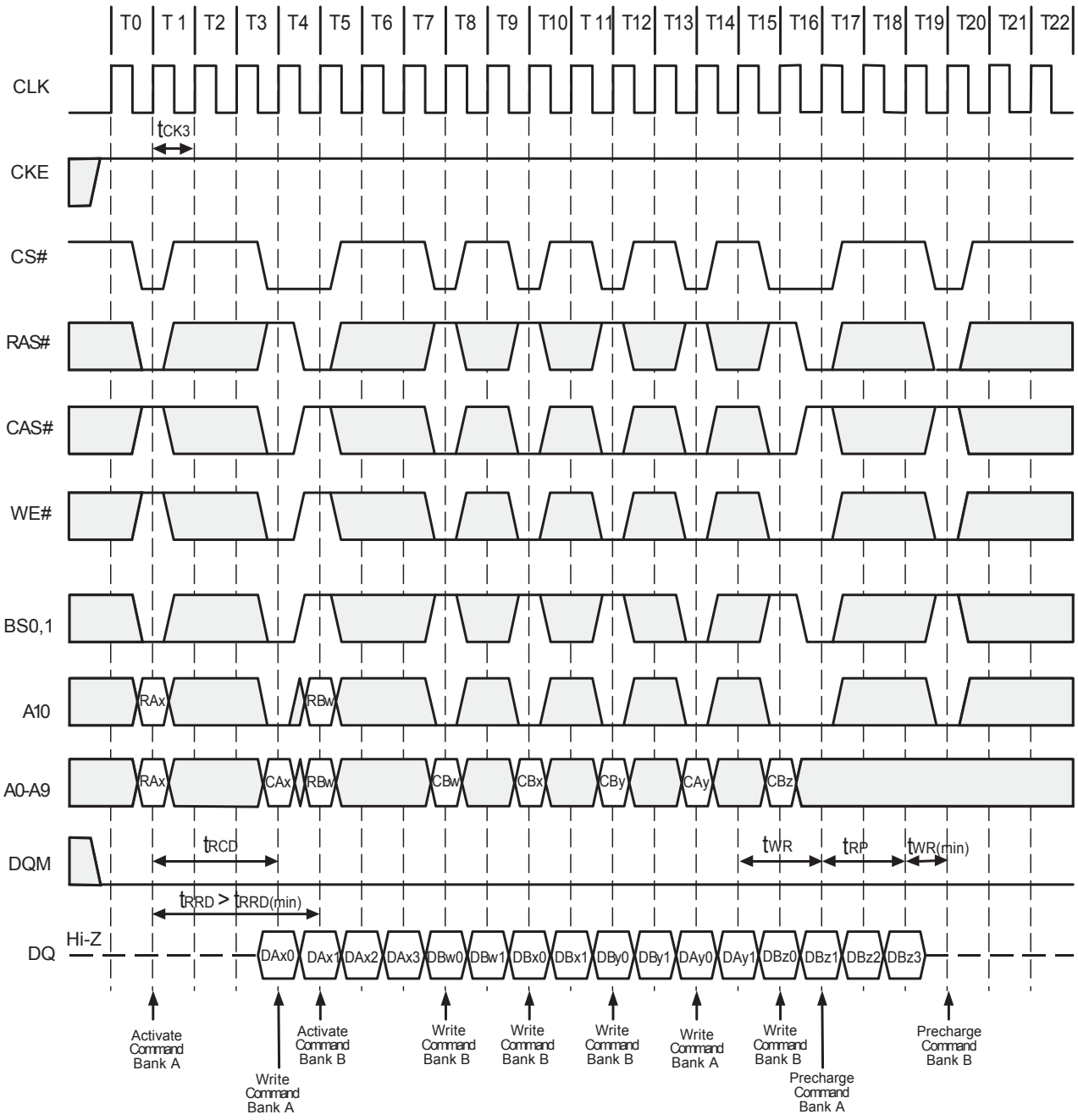


Figure 16.2.Auto Precharge after Read Burst (Burst Length=4,CAS#Latency=2)

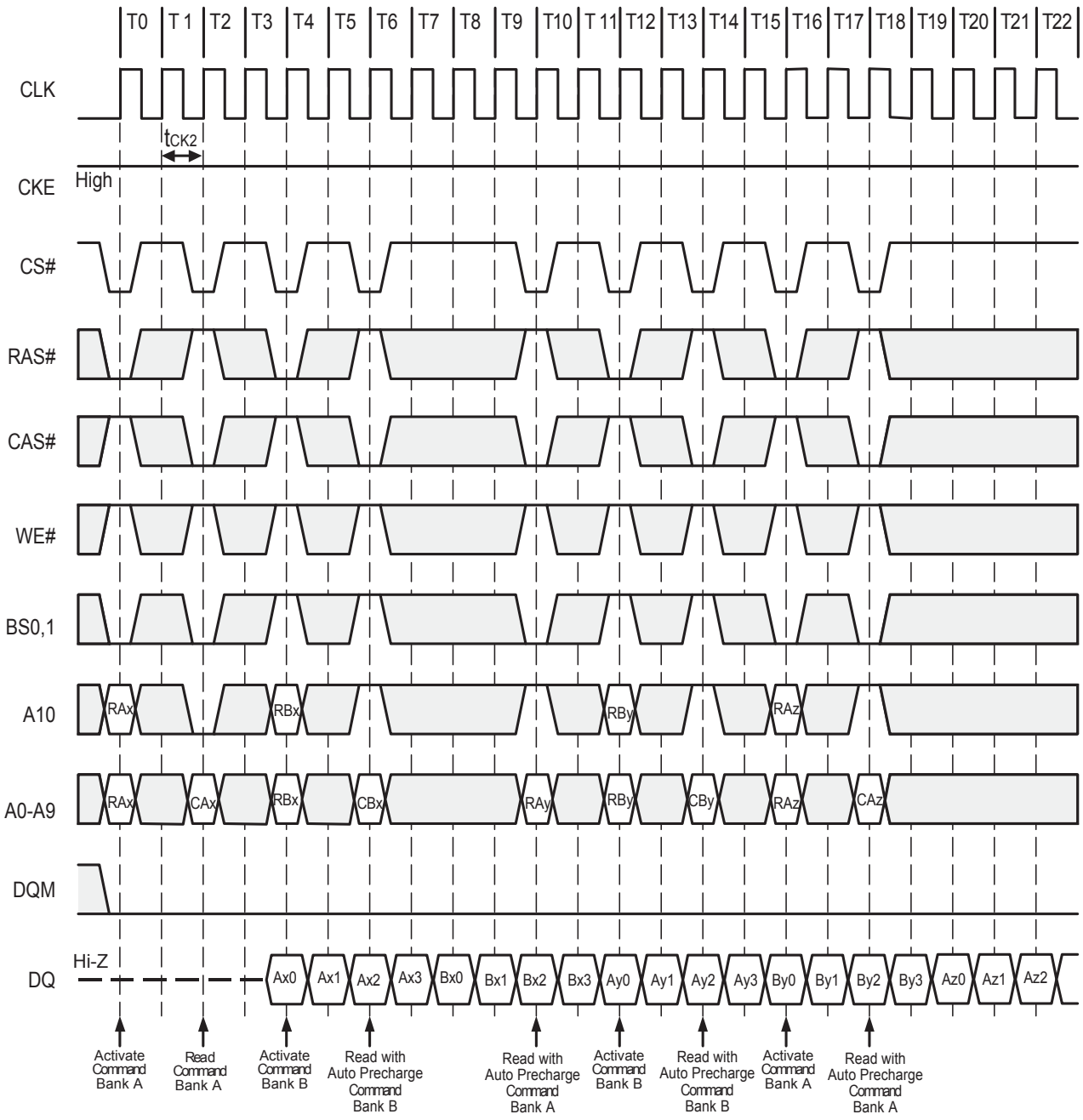


Figure 16.3.Auto Precharge after Read Burst (Burst Length=4,CAS#Latency=3)

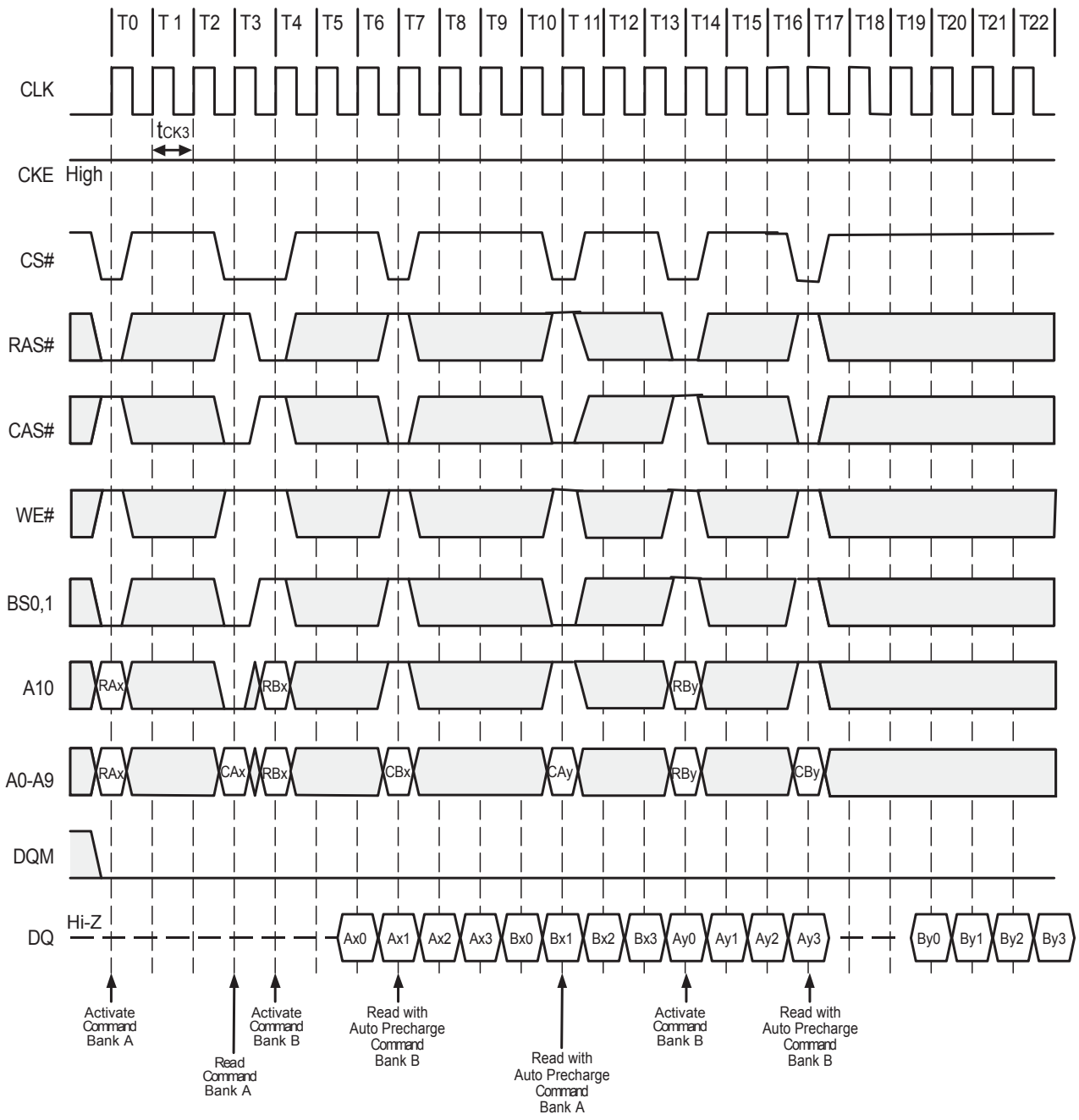


Figure 17.2.Auto Precharge after Write Burst (Burst Length=4,CAS#Latency=2)

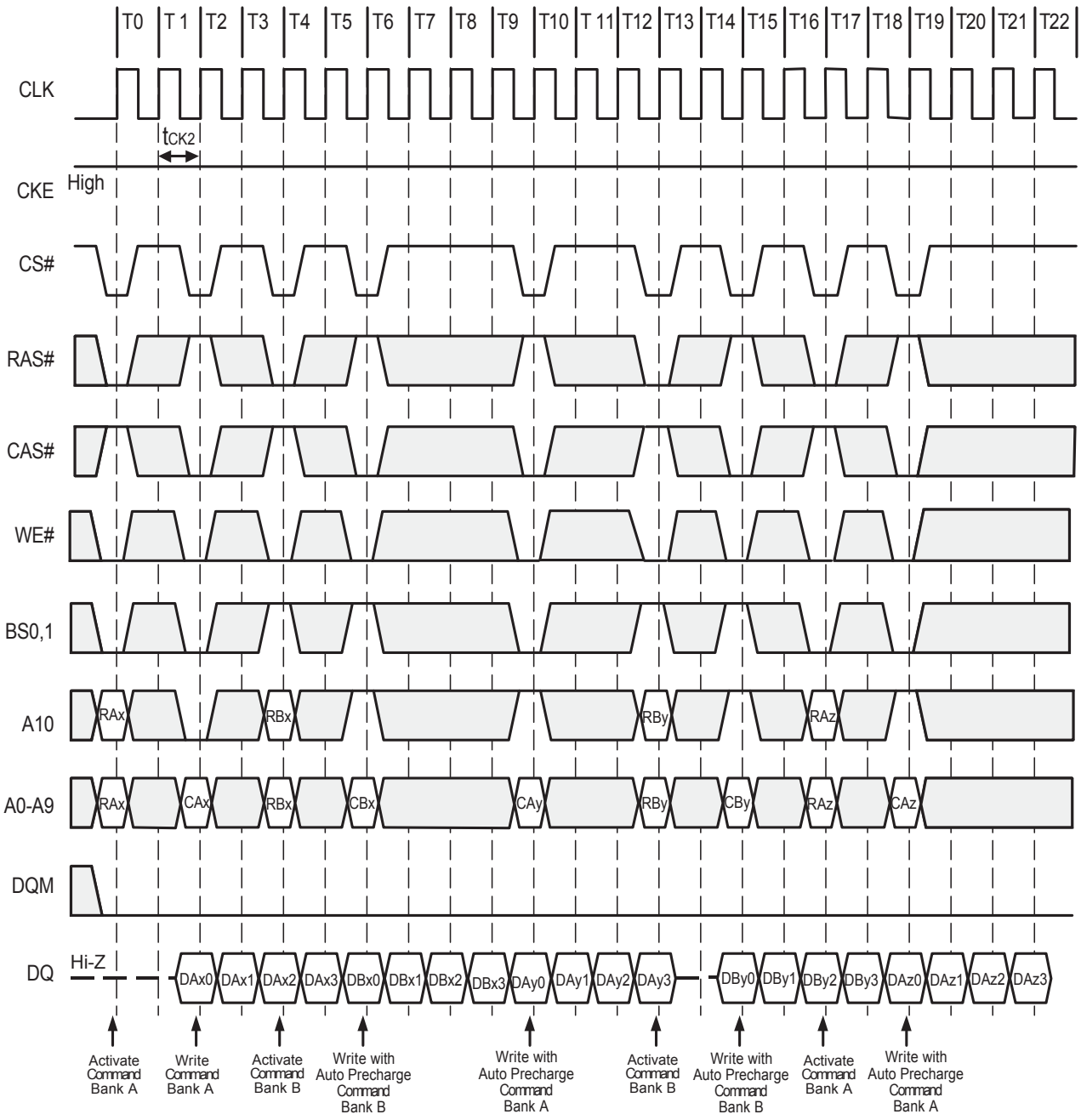


Figure 17.3.Auto Precharge after Write Burst (Burst Length=4,CAS#Latency=3)

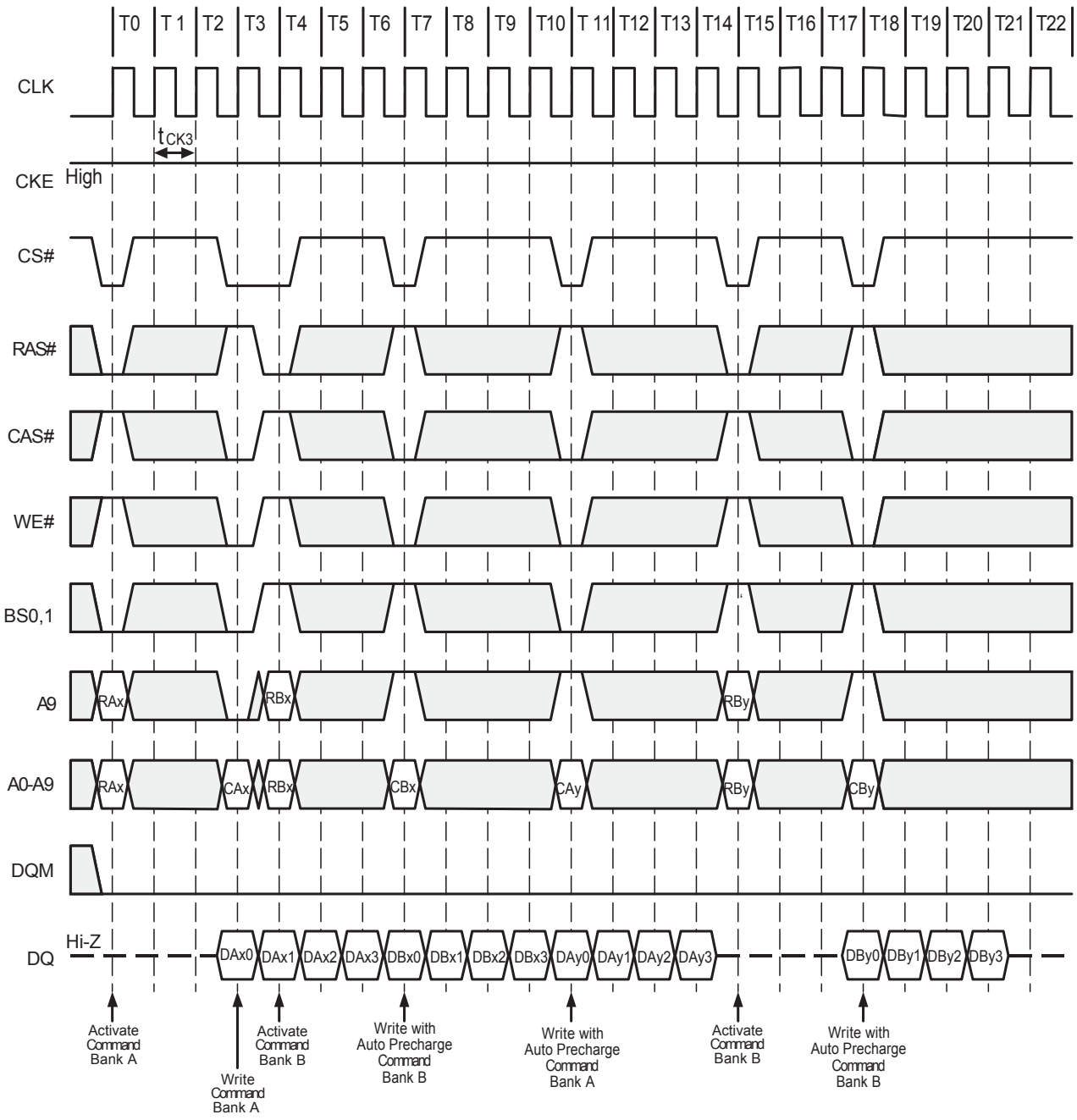


Figure 18.2.Full Page Read Cycle (Burst Length=Full Page,CAS#Latency=2)

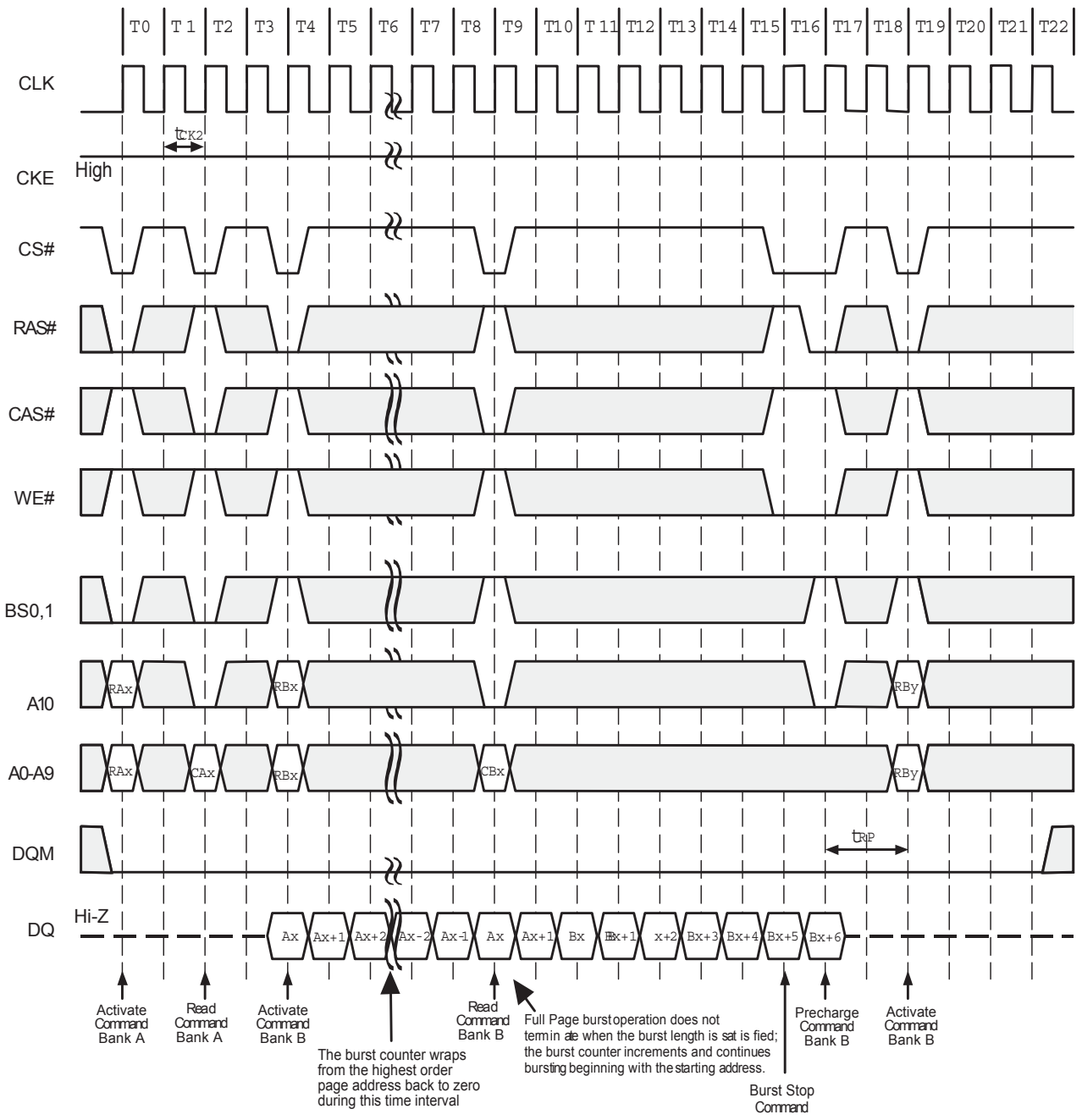


Figure 18.3.Full Page Read Cycle (Burst Length=Full Page,CAS#Latency=3)

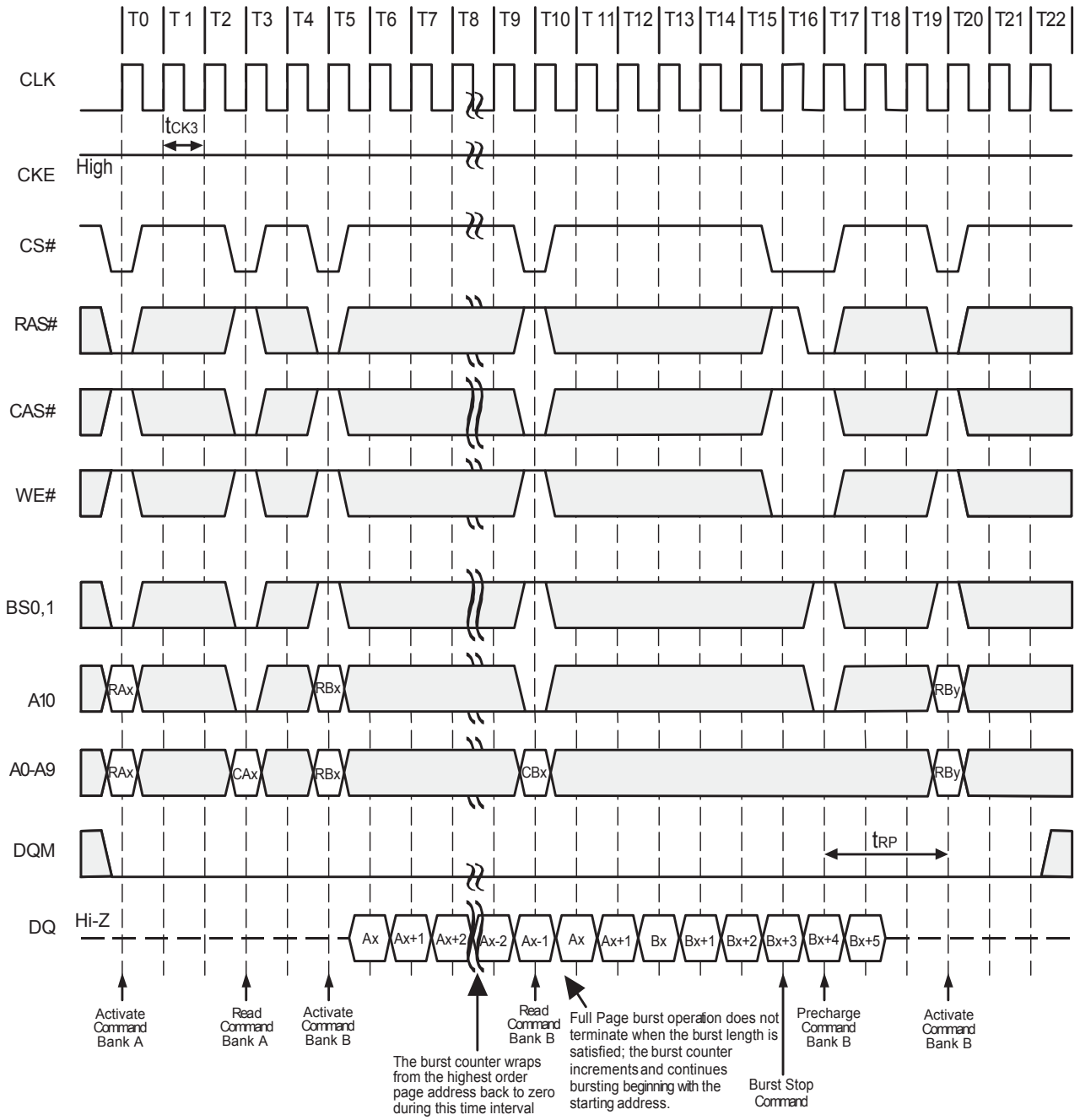


Figure 19.2.Full Page Write Cycle (Burst Length=Full Page,CAS#Latency=2)

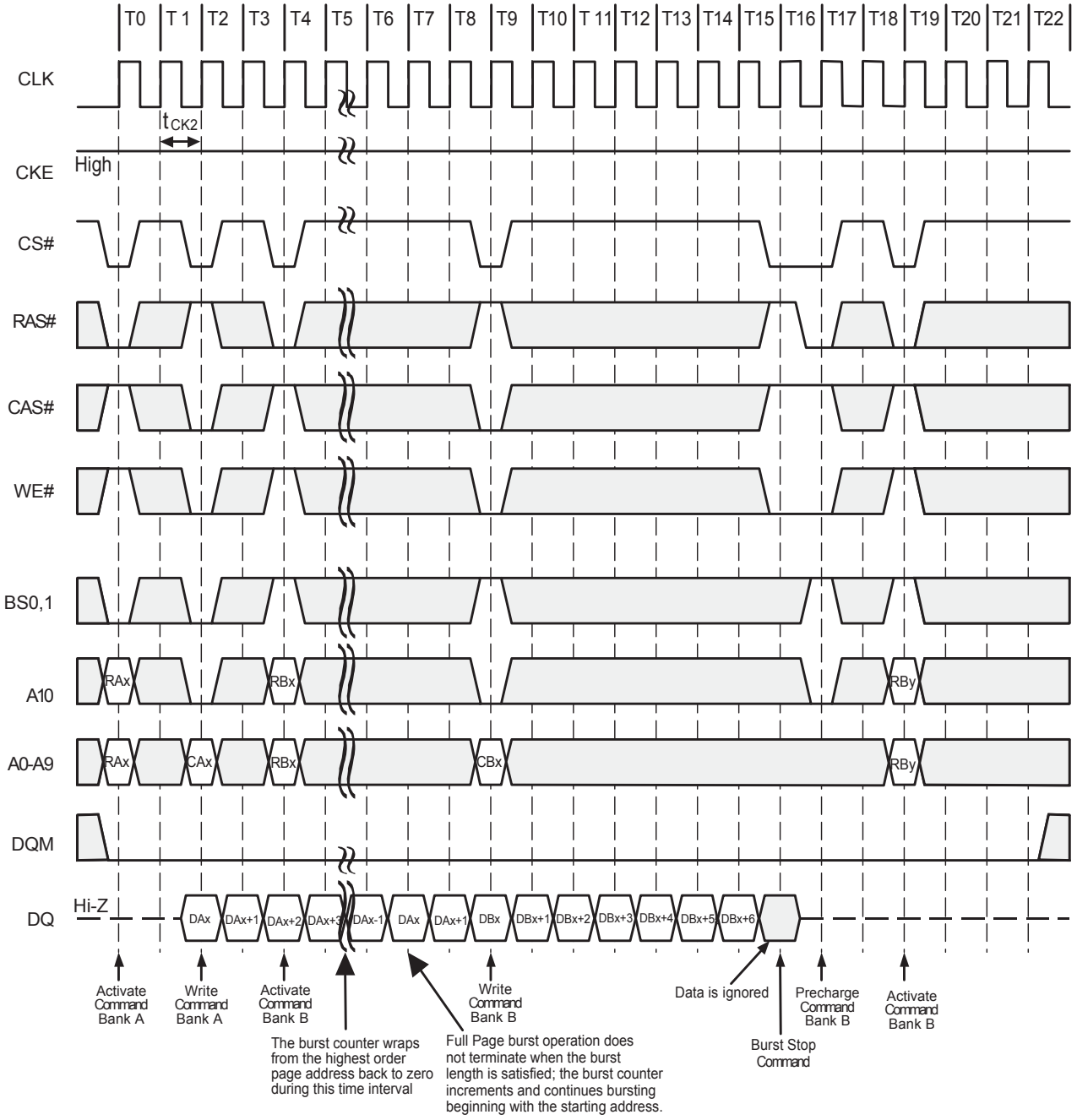


Figure 19.3.Full Page Write Cycle (Burst Length=Full Page,CAS#Latency=3)

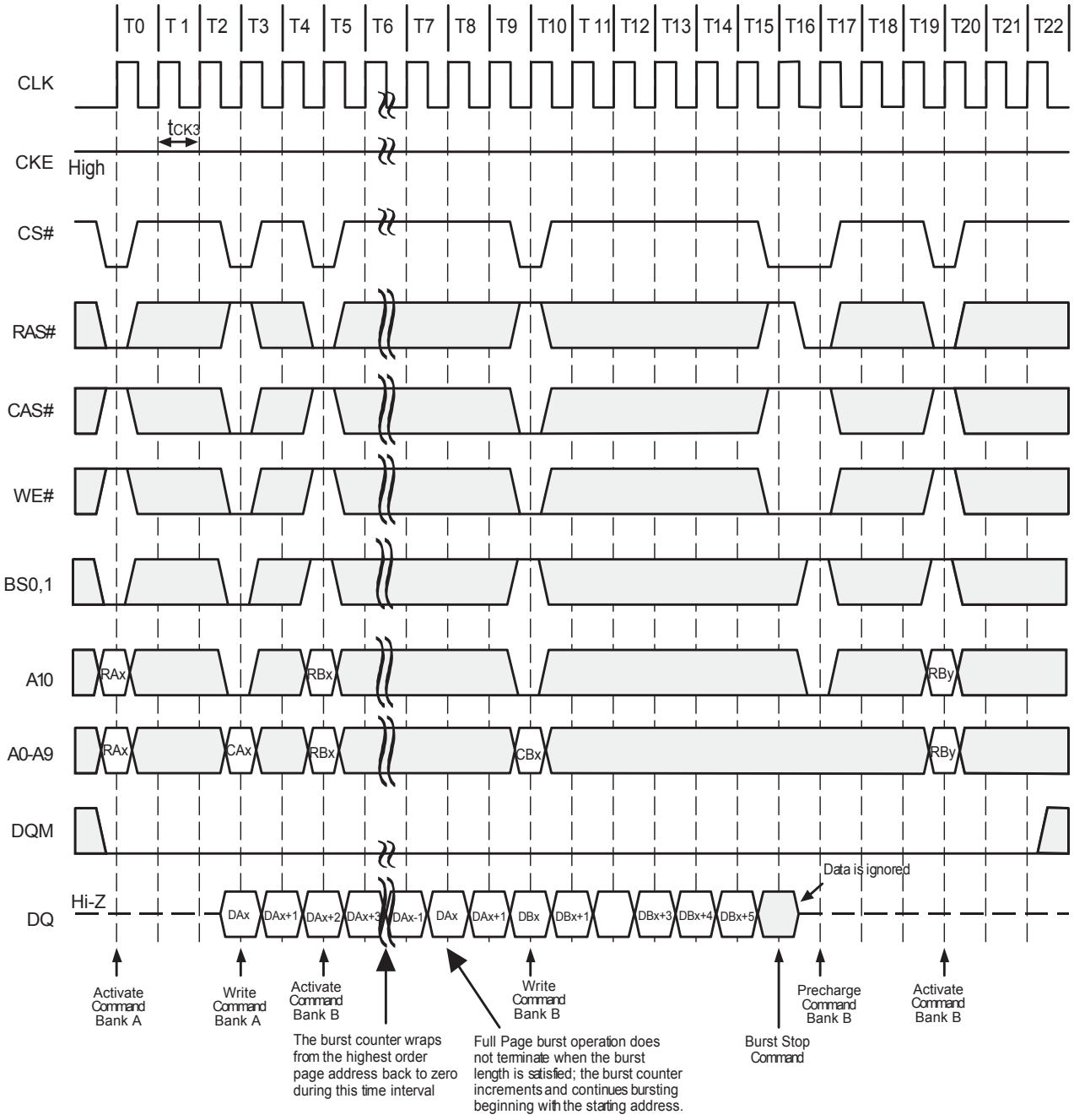


Figure 20.Byte Write Operation (Burst Length=4,CAS#Latency=2)

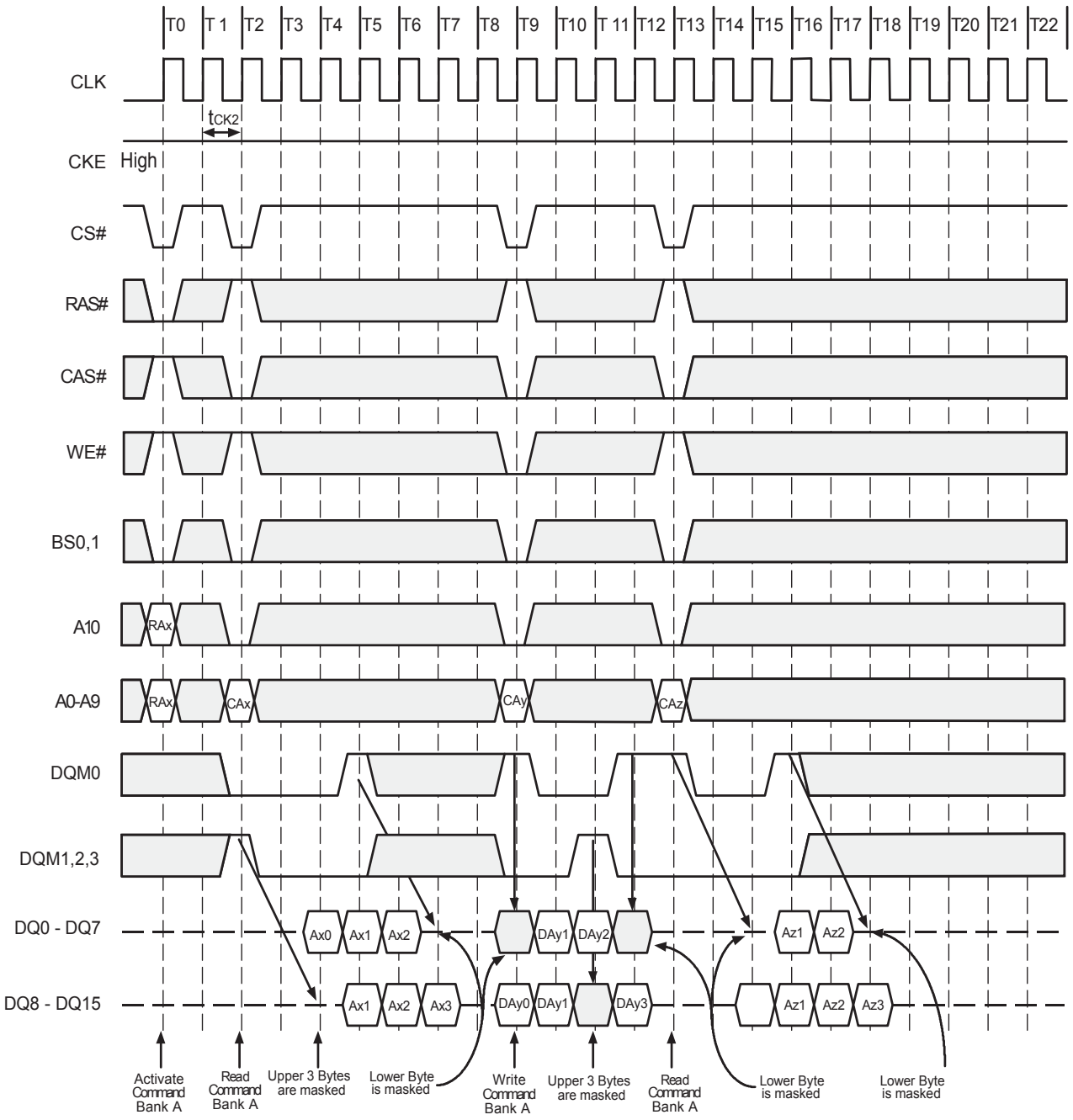


Figure 22.Full Page Random Column Read (Burst Length=Full Page,CAS#Latency=2)

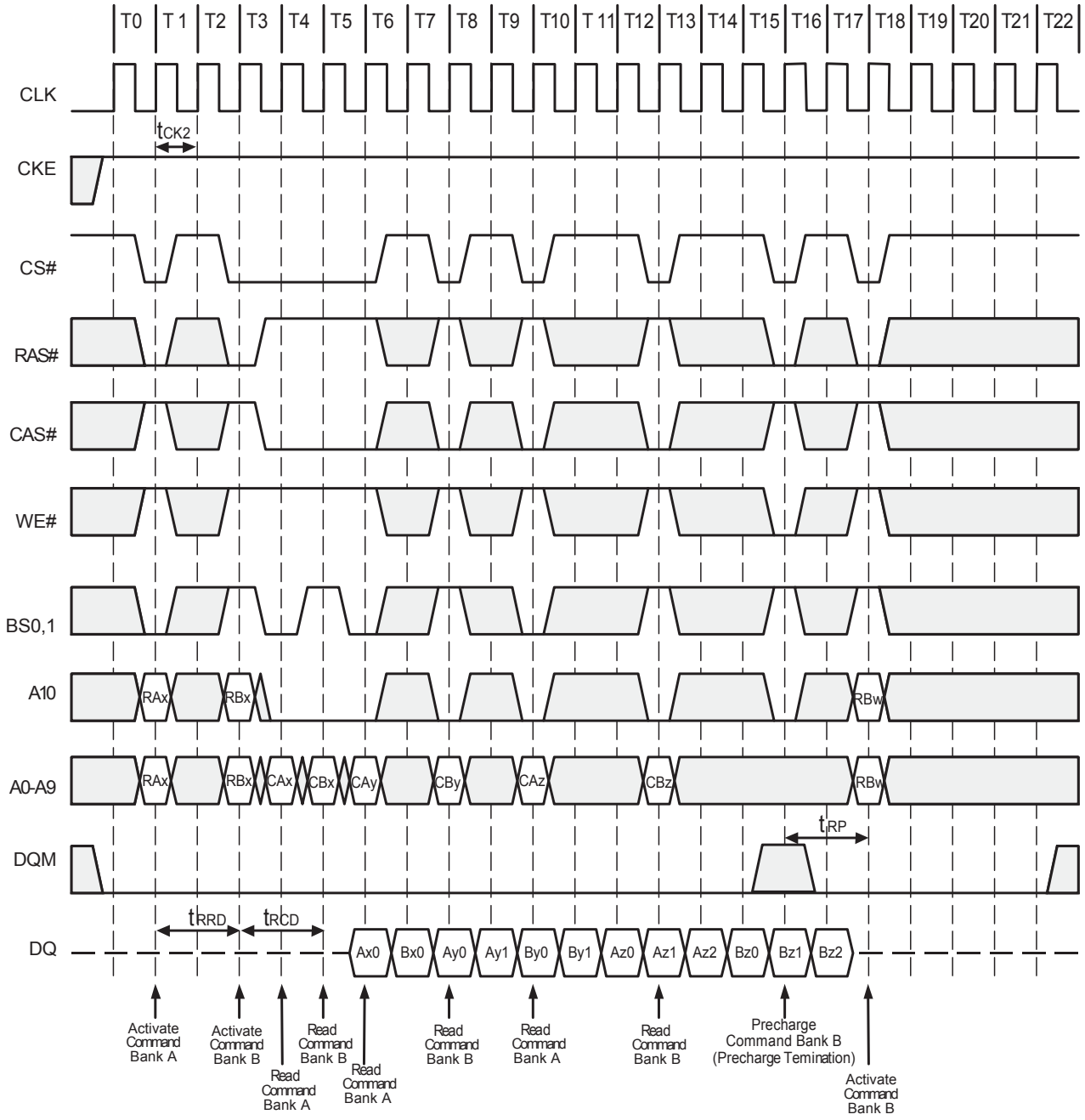


Figure 23.Full Page Random Column Write (Burst Length=Full Page,CAS#Latency=2)

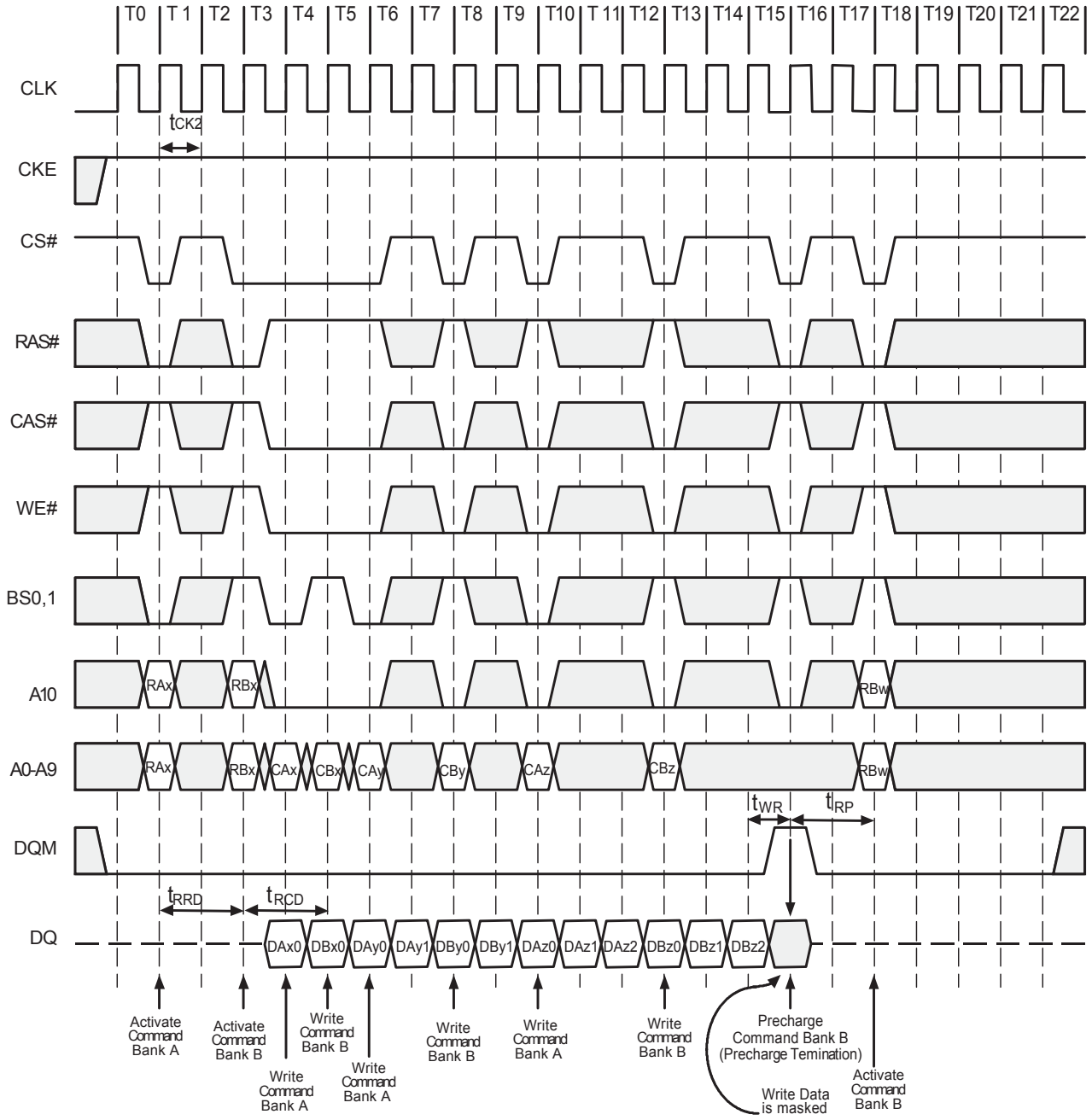


Figure 24.2.Precharge Termination of a Burst

(Burst Length=8 or Full Page,CAS#Latency=2)

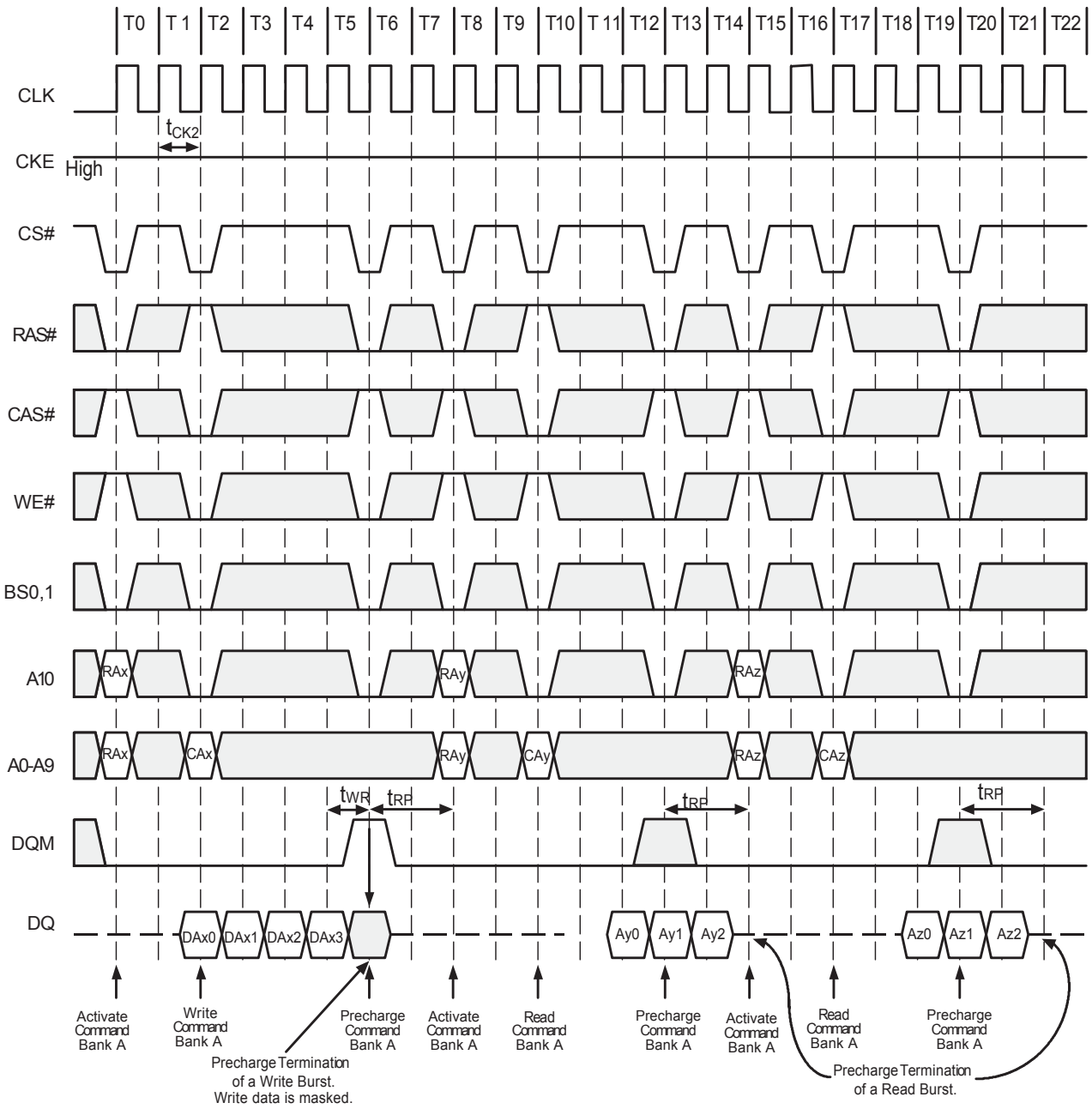
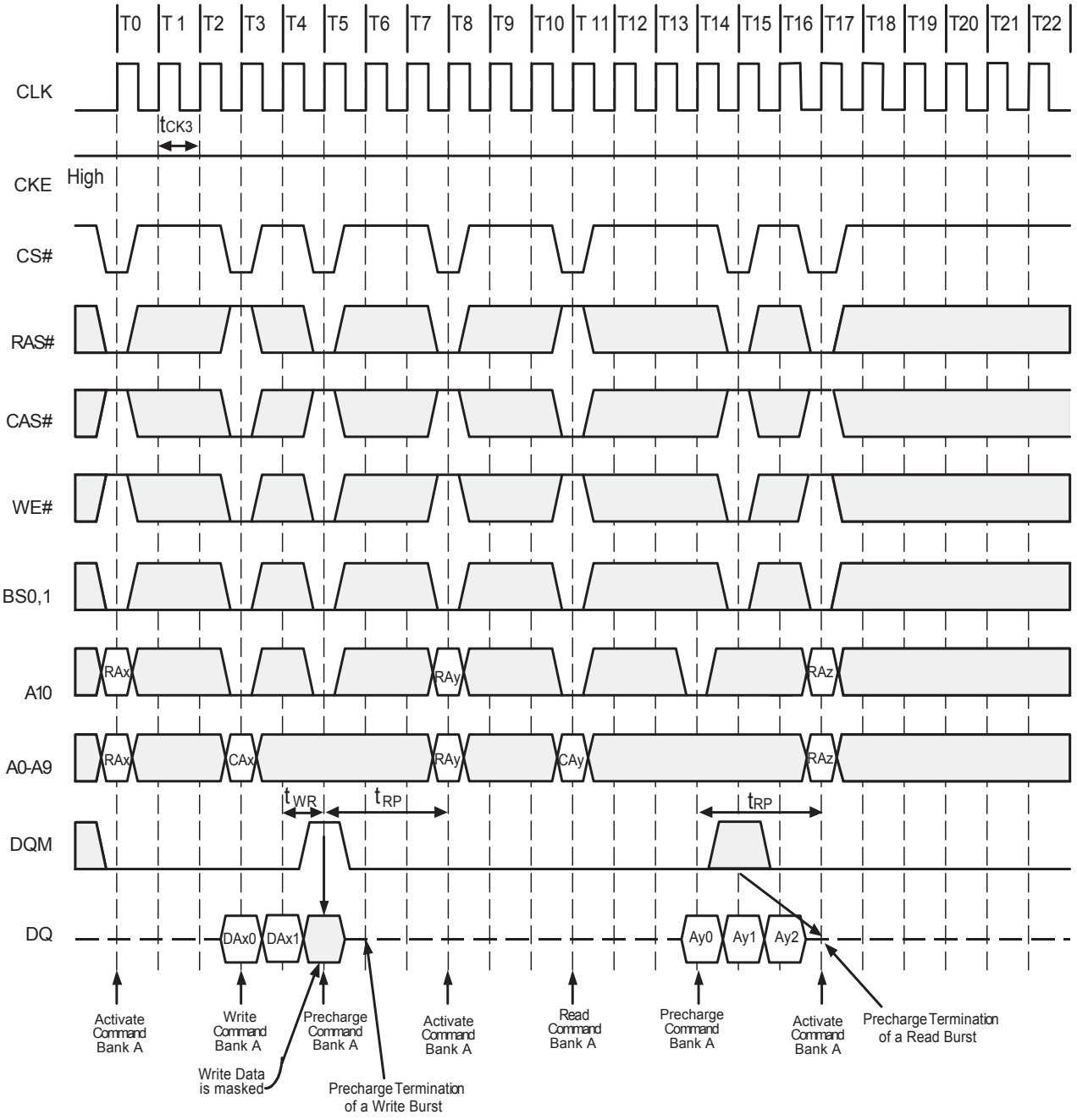


Figure 24.3.Precharge Termination of a Burst

(Burst Length=4,8 or Full Page,CAS#Latency=3)



ORDERING INFORMATION

Commercial Range: 0°C to 70°C

Frequency	Speed (ns)	Order Part No.	Package
166MHz	6	IC42S32400/L-6T	400mil TSOP-2
166MHz	6	IC42S32400/L-6B	11*13mm BGA
143MHz	7	IC42S32400/L-7T	400mil TSOP-2
143MHz	7	IC42S32400/L-7B	11*13mm BGA
125MHz	8	IC42S32400/L-8T	400mil TSOP-2
125MHz	8	IC42S32400/L-8B	11*13mm BGA

ORDERING INFORMATION

Industrial Temperature Range: -40°C to 85°C

Frequency	Speed (ns)	Order Part No.	Package
166MHz	6	IC42S32400/L-6TI	400mil TSOP-2
166MHz	6	IC42S32400/L-6BI	11*13mm BGA
143MHz	7	IC42S32400/L-7TI	400mil TSOP-2
143MHz	7	IC42S32400/L-7BI	11*13mm BGA
125MHz	8	IC42S32400/L-8TI	400mil TSOP-2
125MHz	8	IC42S32400/L-8BI	11*13mm BGA

ORDERING INFORMATION (Pb-free Package)
Commercial Range: 0°C to 70°C

Frequency	Speed (ns)	Order Part No.	Package
166MHz	6	IC42S32400/L-6TG	400mil TSOP-2
166MHz	6	IC42S32400/L-6BG	11*13mm BGA
143MHz	7	IC42S32400/L-7TG	400mil TSOP-2
143MHz	7	IC42S32400/L-7BG	11*13mm BGA
125MHz	8	IC42S32400/L-8TG	400mil TSOP-2
125MHz	8	IC42S32400/L-8BG	11*13mm BGA

ORDERING INFORMATION (Pb-free Package)
Industrial Temperature Range: -40°C to 85°C

Frequency	Speed (ns)	Order Part No.	Package
166MHz	6	IC42S32400/L-6TIG	400mil TSOP-2
166MHz	6	IC42S32400/L-6BIG	11*13mm BGA
143MHz	7	IC42S32400/L-7TIG	400mil TSOP-2
143MHz	7	IC42S32400/L-7BIG	11*13mm BGA
125MHz	8	IC42S32400/L-8TIG	400mil TSOP-2
125MHz	8	IC42S32400/L-8BIG	11*13mm BGA

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