

IC61C6416

64K x 16 HIGH-SPEED CMOS STATIC RAM

FEATURES

- High-speed access time: 10, 12, 15, and 20 ns
- CMOS low power operation
 - 1650 mW (max) @ -10ns Cycle
 - 55 mW (max) CMOS Standby
- TTL compatible interface levels
- Single 5V \pm 10% power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial temperature available
- Available in 44-pin SOJ package and 44-pin TSOP-2

DESCRIPTION

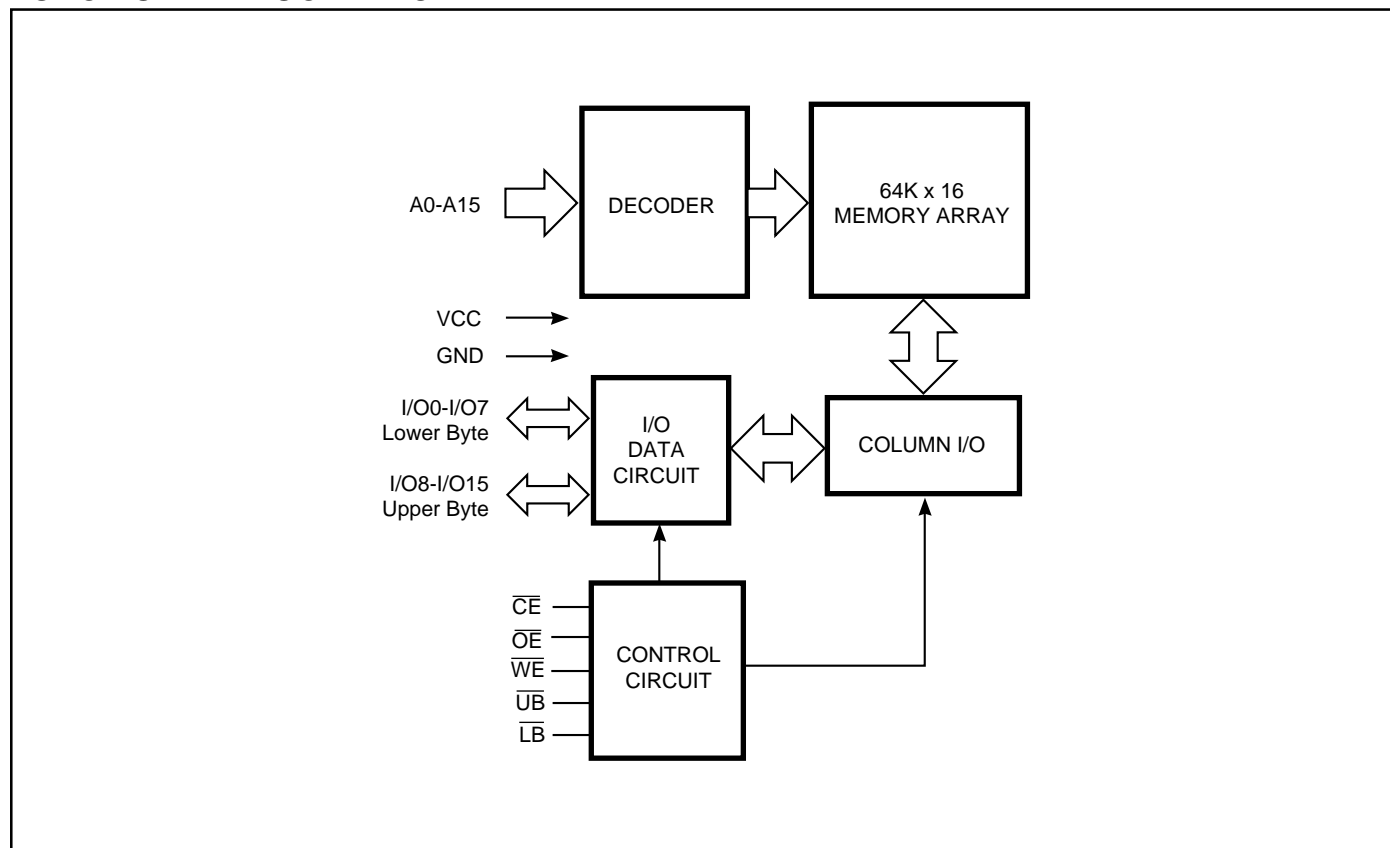
The *ICSI* IC61C6416 is a high-speed, 1,048,576-bit static RAM organized as 65,536 words by 16 bits. It is fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 10 ns with low power consumption.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, \overline{CE} and \overline{OE} . The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory. A data byte allows Upper Byte (\overline{UB}) and Lower Byte (\overline{LB}) access.

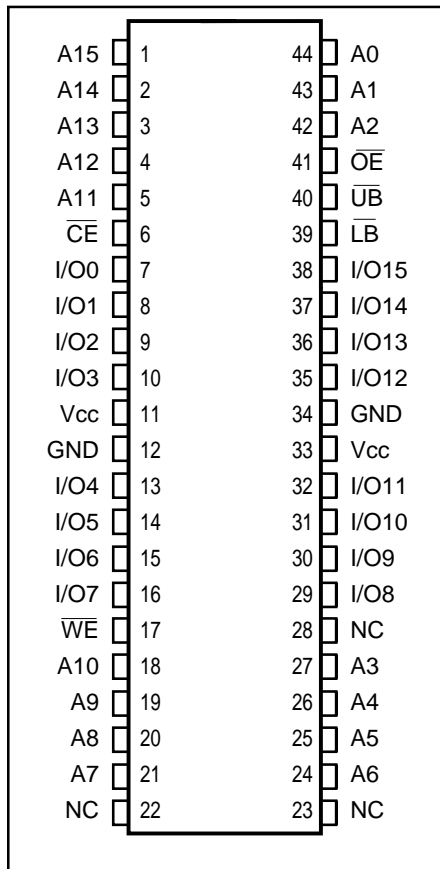
The IC61C6416 is packaged in the JEDEC standard 44-pin 400mil SOJ and 44-pin 400mil TSOP-2.

FUNCTIONAL BLOCK DIAGRAM

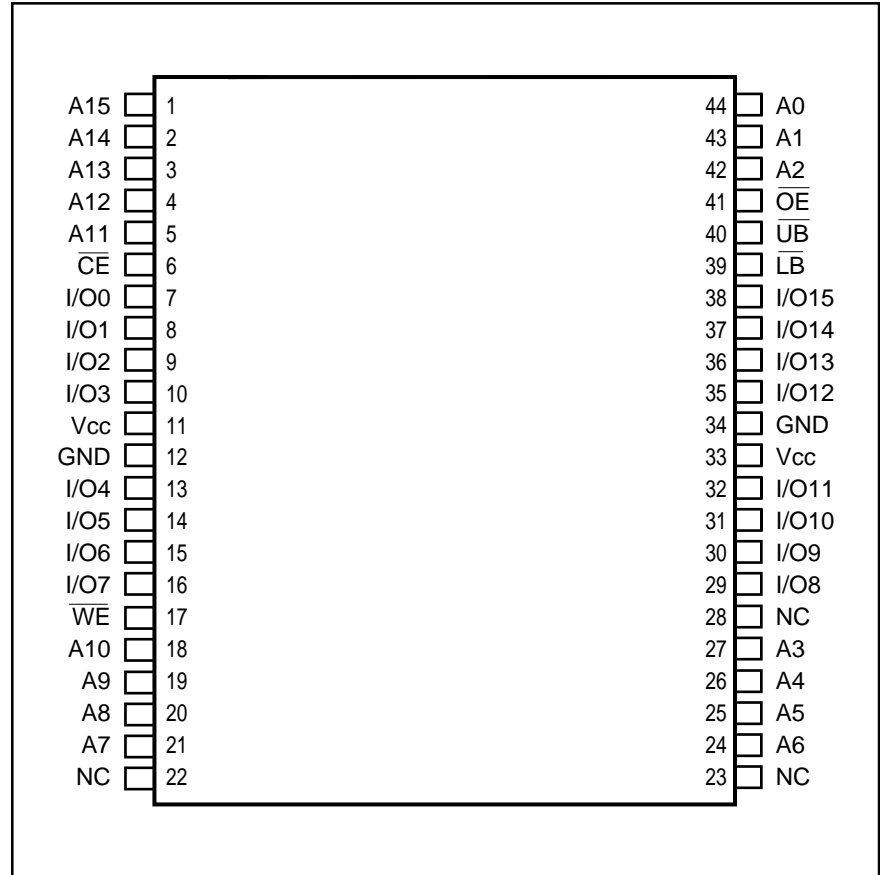


PIN CONFIGURATIONS

44-Pin SOJ



44-Pin TSOP-2



PIN DESCRIPTIONS

| | | | |
|------------|---------------------|-----|---------------------------------|
| A0-A15 | Address Inputs | LB | Lower-byte Control (I/O0-I/O7) |
| I/O0-I/O15 | Data Inputs/Outputs | UB | Upper-byte Control (I/O8-I/O15) |
| CE | Chip Enable Input | NC | No Connection |
| OE | Output Enable Input | Vcc | Power |
| WE | Write Enable Input | GND | Ground |

TRUTH TABLE

| Mode | I/O PIN | | | | | | Vcc Current | |
|-----------------|-----------|-----------|-----------|-----------|-----------|-----------|-------------|------------|
| | WE | CE | OE | LB | UB | I/O0-I/O7 | | I/O8-I/O15 |
| Not Selected | X | H | X | X | X | High-Z | High-Z | Isb1, Isb2 |
| Output Disabled | H | L | H | X | X | High-Z | High-Z | Icc1, Icc2 |
| | X | L | X | H | H | High-Z | High-Z | |
| Read | H | L | L | L | H | DOUT | High-Z | Icc1, Icc2 |
| | H | L | L | H | L | High-Z | DOUT | |
| | H | L | L | L | L | DOUT | DOUT | |
| Write | L | L | X | L | H | DIN | High-Z | Icc1, Icc2 |
| | L | L | X | H | L | High-Z | DIN | |
| | L | L | X | L | L | DIN | DIN | |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|--------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to +7.0 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.5 | W |
| I _{OUT} | DC Output Current (LOW) | 20 | mA |

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

| Range | Ambient Temperature | Speed | V _{CC} |
|------------|---------------------|----------|-----------------|
| Commercial | 0°C to +70°C | -10, -12 | 5V ± 5% |
| | | -15, -20 | 5V ± 10% |
| Industrial | -40°C to +85°C | -12 | 5V ± 5% |
| | | -15, -20 | 5V ± 10% |

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------|-----------------------------------|---|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | — | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 8.0 mA | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage ⁽¹⁾ | | 2.2 | V _{CC} + 0.5 | V |
| V _{IL} | Input LOW Voltage ⁽²⁾ | | -0.5 | 0.8 | V |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{CC} | -2 | 2 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{CC} , Outputs Disabled | -2 | 2 | μA |

Notes:

1. V_{IH} = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL} = -3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -10 | | -12 | | -15 | | -20 | | Unit |
|------------------|--|--|--------------|------|------|------|------------|------|------------|------|------------|------|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| I _{CC} | V _{CC} Dynamic Operating Supply Current | V _{CC} = Max., I _{OUT} = 0 mA, f = MAX | Com. Ind. | — | 300 | — | 280 300 | — | 260 290 | — | 235 255 | mA |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} CE ≥ V _{IH} , f = 0 | Com. Ind. | — | 50 | — | 50 55 | — | 50 55 | — | 50 55 | mA |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{CC} = Max., CE ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. Ind. | — | 10 | — | 10 15 | — | 10 15 | — | 10 15 | mA |

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE⁽¹⁾

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{OUT} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | -10 | | -12 | | -15 | | -20 | | Unit |
|----------------------------------|--|------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{RC} | Read Cycle Time | 10 | — | 12 | — | 15 | — | 20 | — | ns |
| t _{AA} | Address Access Time | — | 10 | — | 12 | — | 15 | — | 20 | ns |
| t _{OH} | Output Hold Time | 3 | — | 3 | — | 3 | — | 4 | — | ns |
| t _{ACE} | \overline{CE} Access Time | — | 10 | — | 12 | — | 15 | — | 20 | ns |
| t _{DOE} | \overline{OE} Access Time | — | 5 | — | 6 | — | 7 | — | 9 | ns |
| t _{HZOE} ⁽²⁾ | \overline{OE} to High-Z Output | — | 5 | — | 6 | 0 | 6 | 0 | 8 | ns |
| t _{LZOE} ⁽²⁾ | \overline{OE} to Low-Z Output | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{HZCE} ⁽²⁾ | \overline{CE} to High-Z Output | 0 | 5 | 0 | 6 | 0 | 6 | 0 | 8 | ns |
| t _{LZCE} ⁽²⁾ | \overline{CE} to Low-Z Output | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| t _{BA} | \overline{LB} , \overline{UB} Access Time | — | 5 | — | 6 | — | 7 | — | 9 | ns |
| t _{HZB} | \overline{LB} , \overline{UB} to High-Z Output | 0 | 5 | 0 | 6 | 0 | 6 | 0 | 8 | ns |
| t _{LZB} | \overline{LB} , \overline{UB} to Low-Z Output | 0 | — | 0 | — | 0 | — | 0 | — | ns |

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 3 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

AC TEST LOADS

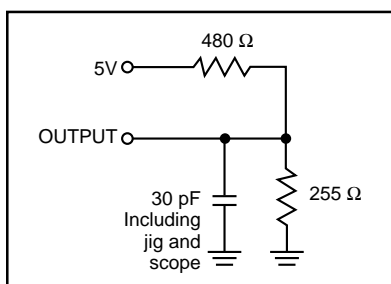


Figure 1

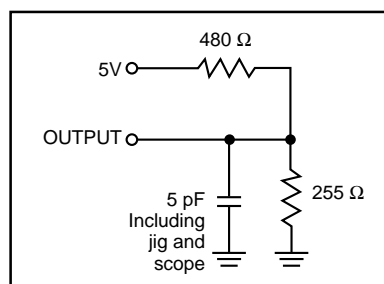
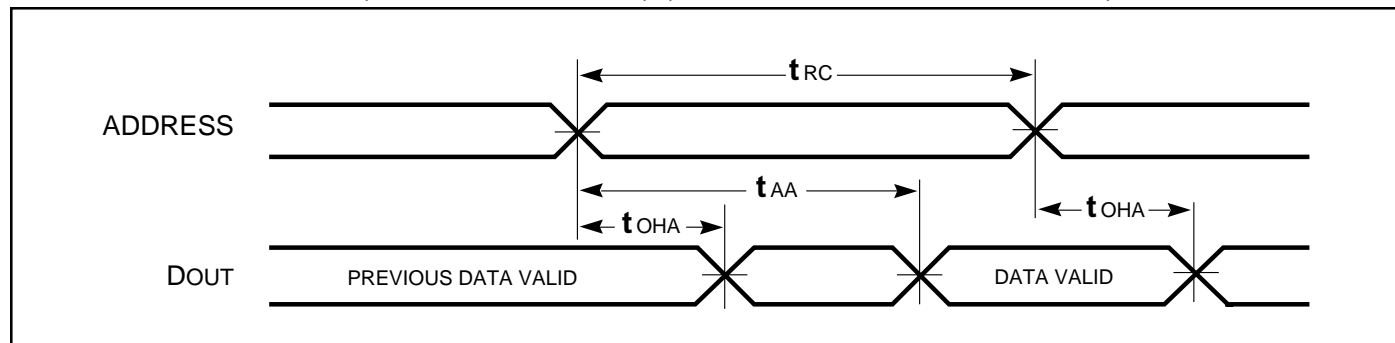


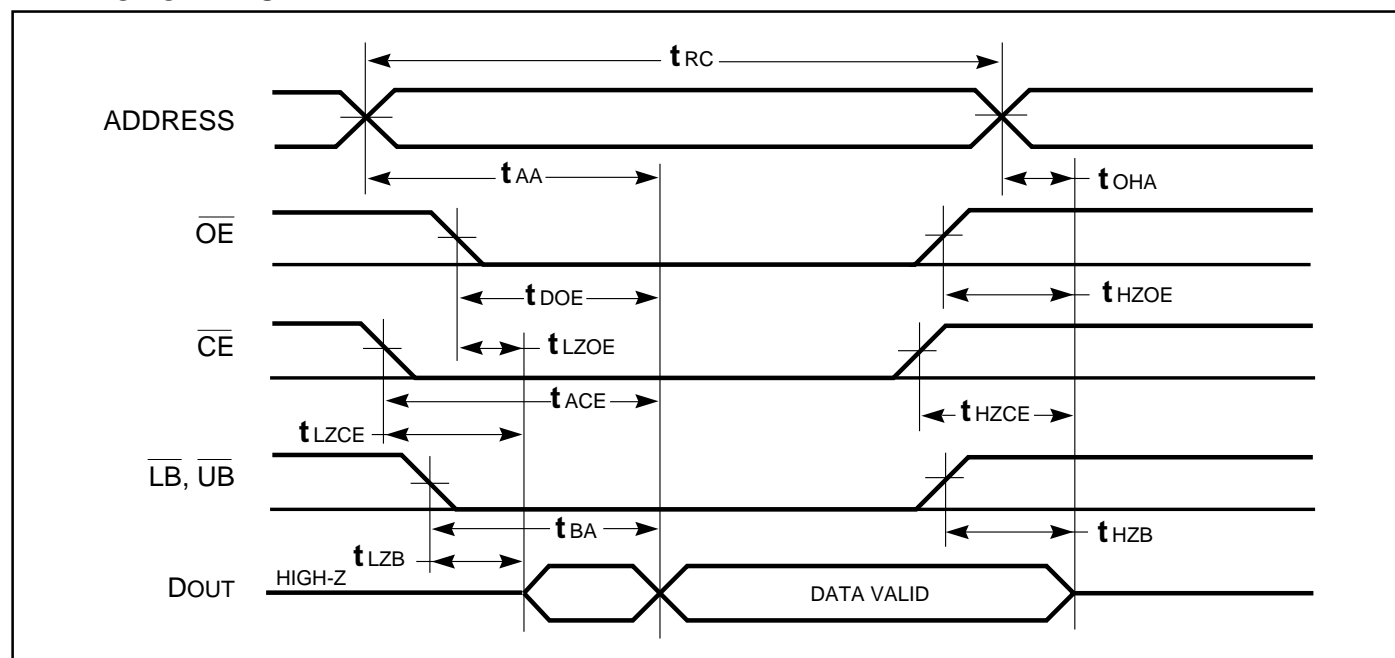
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$, \overline{UB} or $\overline{LB} = V_{IL}$)



READ CYCLE NO. 2^(1,3)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , \overline{CE} , \overline{UB} , or $\overline{LB} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transition.

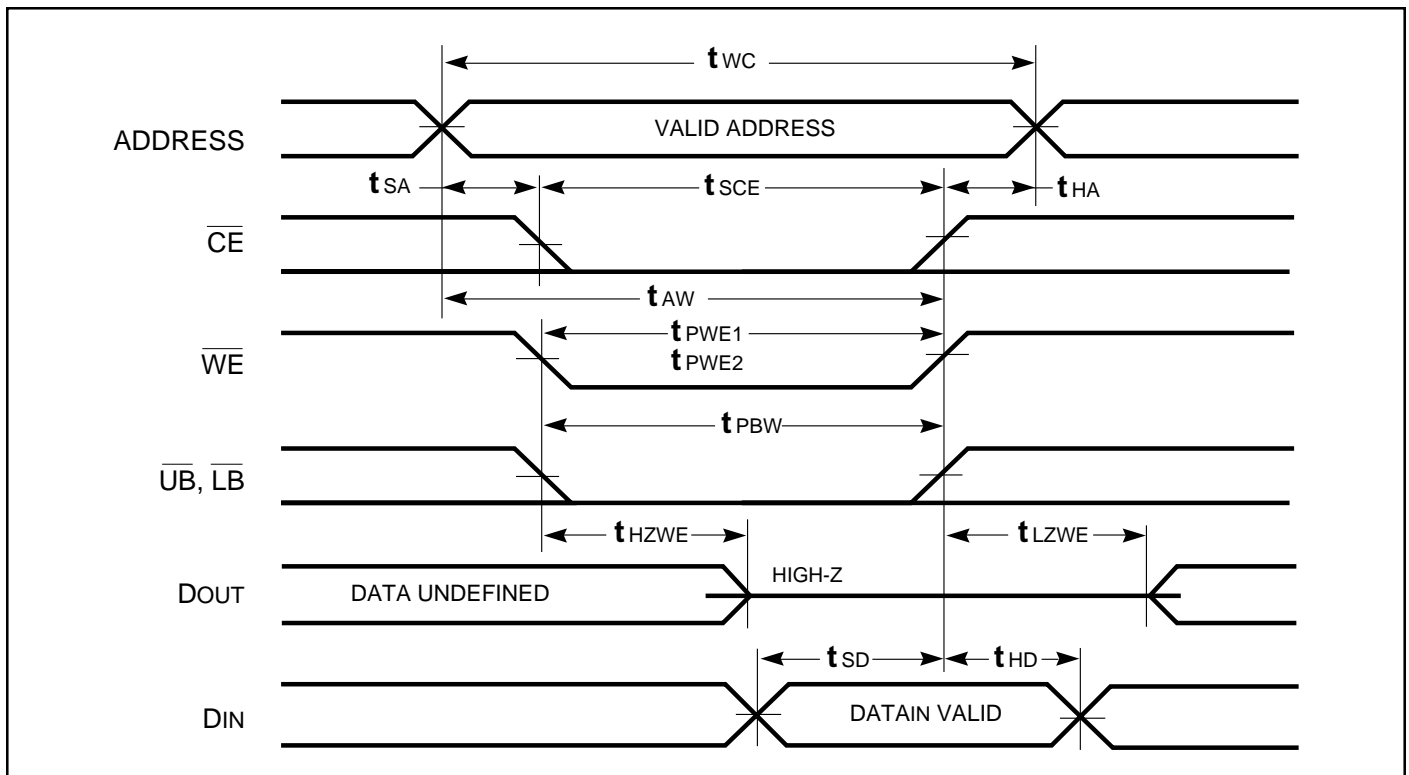
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

| Symbol | Parameter | -10 | | -12 | | -15 | | -20 | | Unit |
|----------------------------------|---|------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{WC} | Write Cycle Time | 10 | — | 12 | — | 15 | — | 20 | — | ns |
| t _{SC} | $\overline{\text{CE}}$ to Write End | 8 | — | 9 | — | 10 | — | 12 | — | ns |
| t _{AW} | Address Setup Time to Write End | 8 | — | 9 | — | 10 | — | 12 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{PWB} | $\overline{\text{LB}}$, $\overline{\text{UB}}$ Valid to End of Write | 8 | — | 9 | — | 10 | — | 12 | — | ns |
| t _{PWE} | $\overline{\text{WE}}$ Pulse Width | 8 | — | 9 | — | 10 | — | 12 | — | ns |
| t _{SD} | Data Setup to Write End | 5 | — | 6 | — | 7 | — | 9 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{HZWE} ⁽²⁾ | $\overline{\text{WE}}$ LOW to High-Z Output | — | 5 | — | 6 | — | 7 | — | 9 | ns |
| t _{LZWE} ⁽²⁾ | $\overline{\text{WE}}$ HIGH to Low-Z Output | 3 | — | 3 | — | 3 | — | 3 | — | ns |

Notes:

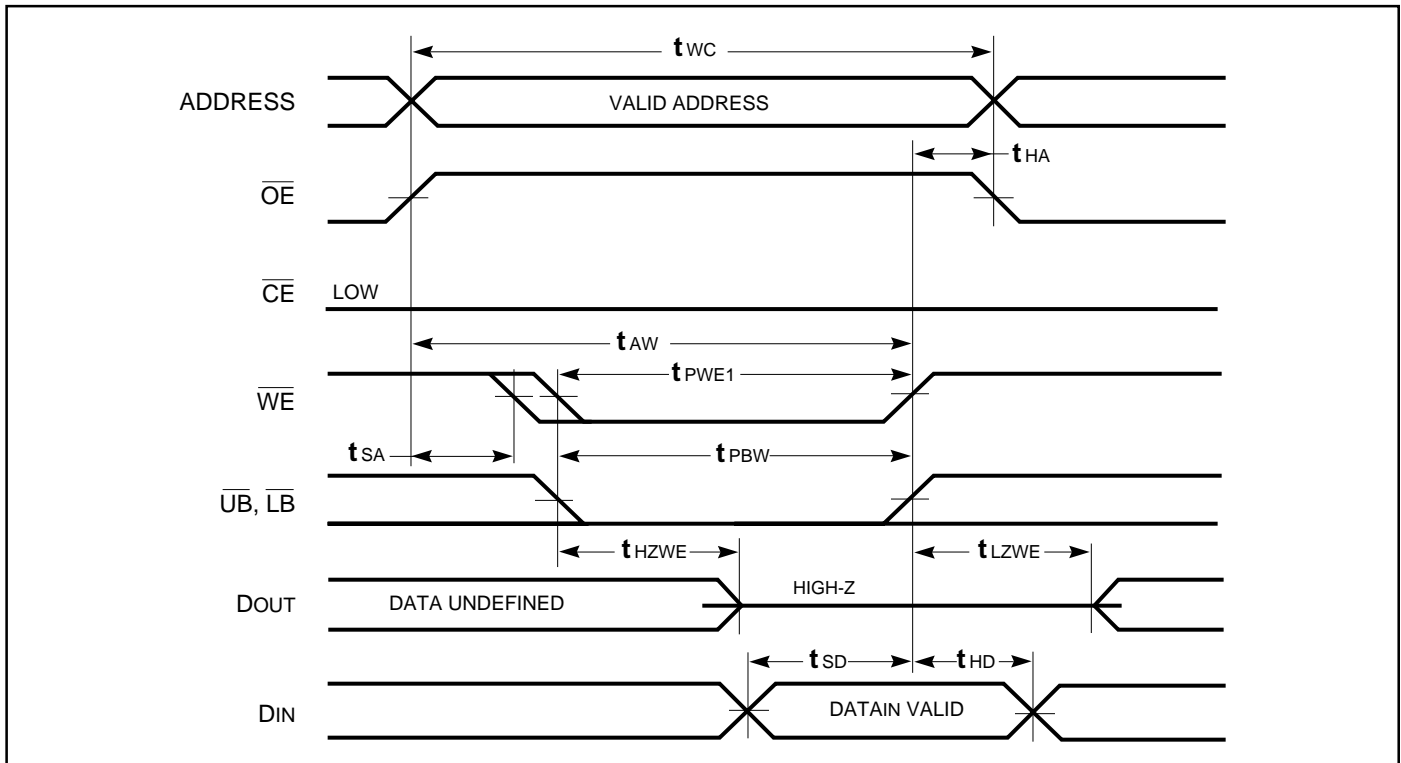
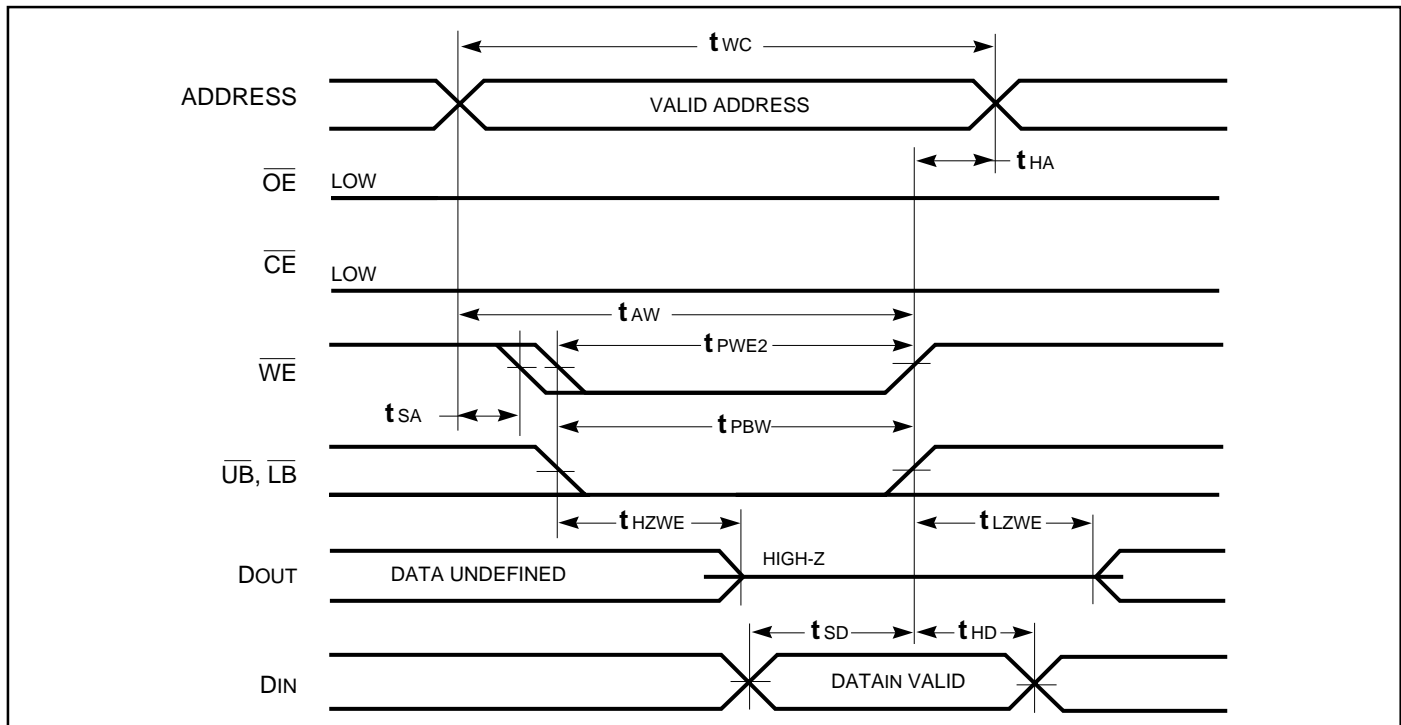
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{UB}}$ or $\overline{\text{LB}}$, and $\overline{\text{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

WRITE CYCLE NO. 1 (\overline{WE} Controlled)^(1,2)

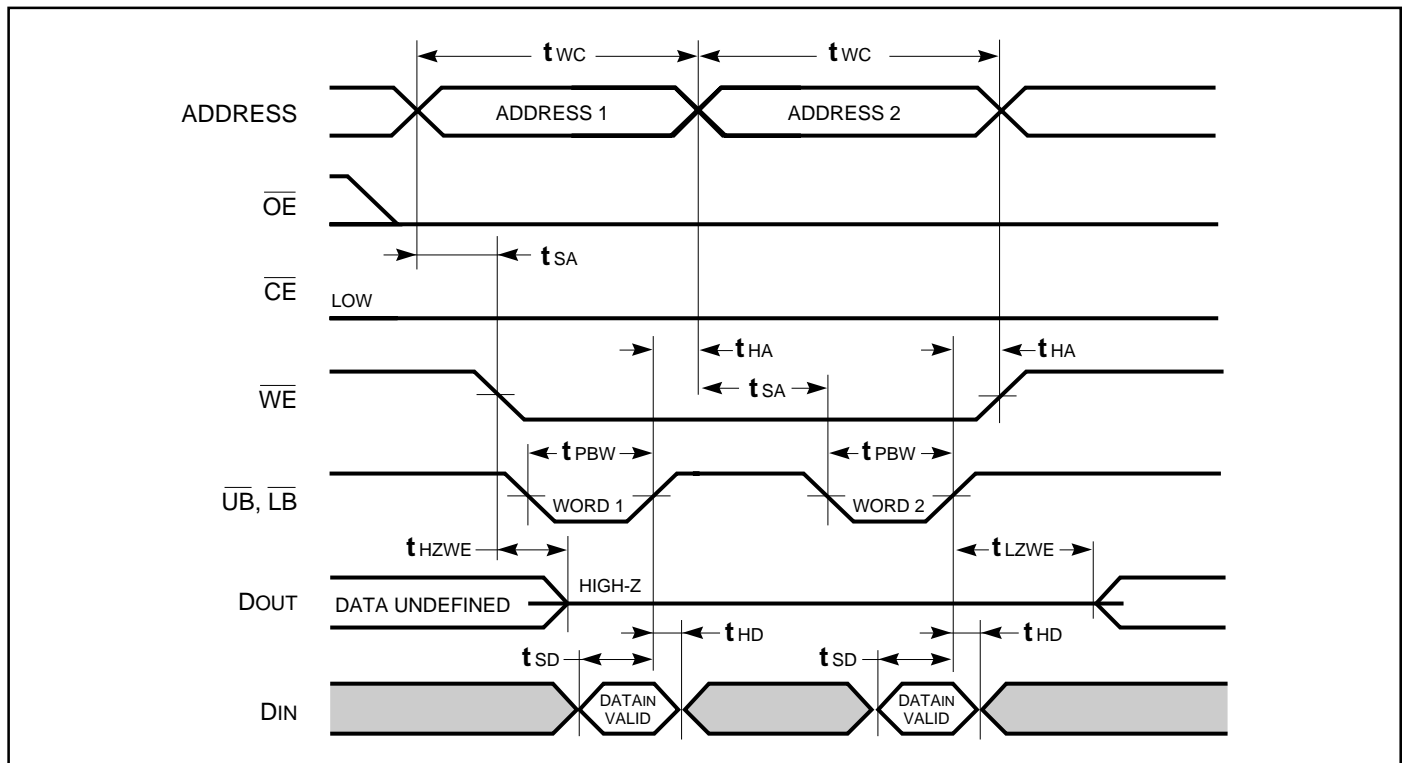
Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the \overline{CE} and \overline{WE} inputs and at least one of the \overline{LB} and \overline{UB} inputs being in the LOW state.
2. $WRITE = (\overline{CE}) [(\overline{LB}) = (\overline{UB})] (\overline{WE})$.

WRITE CYCLE NO. 2 (\overline{OE} is HIGH During Write Cycle) ^(1,2)WRITE CYCLE NO. 3 (\overline{OE} is LOW During Write Cycle) ⁽¹⁾

Notes:

1. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $OE \geq V_{IH}$.

WRITE CYCLE NO. 4 ($\overline{UB}/\overline{LB}$ Back to Back Write)

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

| Speed (ns) | Order Part No. | Package |
|------------|----------------|---------------|
| 10 | IC61C6416-10T | 400mil TSOP-2 |
| 10 | IC61C6416-10K | 400mil SOJ |
| 12 | IC61C6416-12T | 400mil TSOP-2 |
| 12 | IC61C6416-12K | 400mil SOJ |
| 15 | IC61C6416-15T | 400mil TSOP-2 |
| 15 | IC61C6416-15K | 400mil SOJ |
| 20 | IC61C6416-20T | 400mil TSOP-2 |
| 20 | IC61C6416-20K | 400mil SOJ |

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|------------|----------------|---------------|
| 12 | IC61C6416-12TI | 400mil TSOP-2 |
| 12 | IC61C6416-12KI | 400mil SOJ |
| 15 | IC61C6416-15TI | 400mil TSOP-2 |
| 15 | IC61C6416-15KI | 400mil SOJ |
| 20 | IC61C6416-20TI | 400mil TSOP-2 |
| 20 | IC61C6416-20KI | 400mil SOJ |

*Integrated Circuit Solution Inc.*

HEADQUARTER:

NO.2, TECHNOLOGY RD. V, SCIENCE-BASED INDUSTRIAL PARK,
HSIN-CHU, TAIWAN, R.O.C.

TEL: 886-3-5780333

Fax: 886-3-5783000

BRANCH OFFICE:

7F, NO. 106, SEC. 1, HSIN-TAI 5TH ROAD,
HSICHIH TAIPEI COUNTY, TAIWAN, R.O.C.

TEL: 886-2-26962140

FAX: 886-2-26962252

<http://www.icsi.com.tw>