

## Document Title

512 K x 16 bit Low Voltage and Ultra Low Power CMOS Static RAM

## Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0A	Initial Draft	January 3,2002	Preliminary
0B	1. Add CE2 pin for 48 pin TF-BGA 2. Change for I <sub>CC</sub> : 35 mA to 30 mA for 55 ns Industrial product 30 mA to 25 mA for 70 ns Industrial product 25 mA to 20 mA for 100 ns Industrial product  30 mA to 25 mA for 55 ns Commerical product 25 mA to 20 mA for 70 ns Commerical product 20 mA to 15 mA for 100 ns Commerical product 3. Change for I <sub>SB2</sub> : 20 $\mu$ A to 15 $\mu$ A for Commerical product 4. Change for I <sub>DR</sub> : 15 $\mu$ A to 20 $\mu$ A for Commerical/L product 6 $\mu$ A to 13 $\mu$ A for Commerical/LL product 20 $\mu$ A to 30 $\mu$ A for Industrial/L product 9 $\mu$ A to 23 $\mu$ A for Industrial/LL product	September 2,2002	

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# 512K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

## FEATURES

- High-speed access times: 55, 70, 100 ns
- CMOS low power operation  
I<sub>CC</sub>=18mA (typical)\* operating  
I<sub>SB2</sub>=3μA (typical)\* CMOS standby
- TTL compatible interface levels
- Single 2.7V-3.6V V<sub>CC</sub> power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Available in the know good die from 44-pin TSOP-2 and 48-pin 8x10mm TF-BGA
- CE2 pin only for 48-pin TF-BGA.

\* Typical values are measured at V<sub>CC</sub>=3.0V, T<sub>A</sub>=25°C

## DESCRIPTION

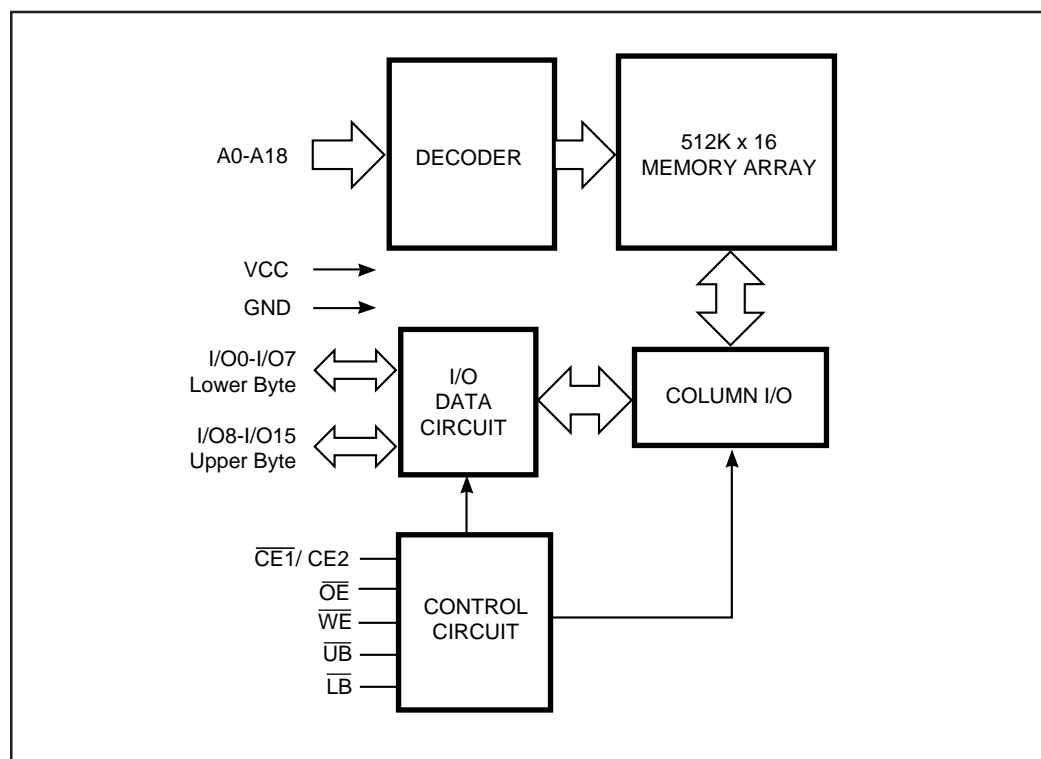
The *ICSI* IC62LV51216L and IC62LV51216LL are low-power, 8.388,608 bit static RAMs organized as 524,288 words by 16 bits. They are fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When  $\overline{CE1}$  is HIGH or when CE2 is low (deselected) or both  $\overline{LB}$  and  $\overline{UB}$  are HIGH, the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using Chip Enable Output and Enable inputs,  $\overline{CE1}$ , CE2 and  $\overline{OE}$ . The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory. A data byte allows Upper Byte ( $\overline{UB}$ ) and Lower Byte ( $\overline{LB}$ ) access.

The IC62LV51216L and IC62LV51216LL are packaged in the JEDEC standard 44-pin TSOP-2 and 48-pin 8\*10mm TF-BGA.

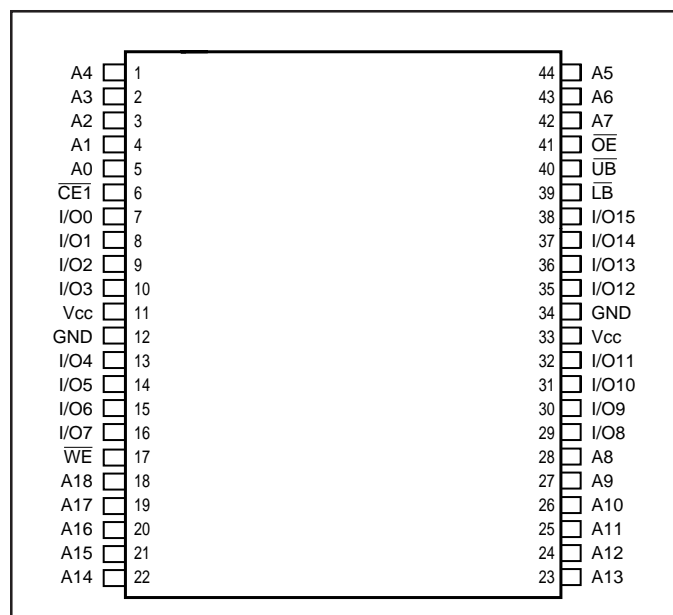
## FUNCTIONAL BLOCK DIAGRAM



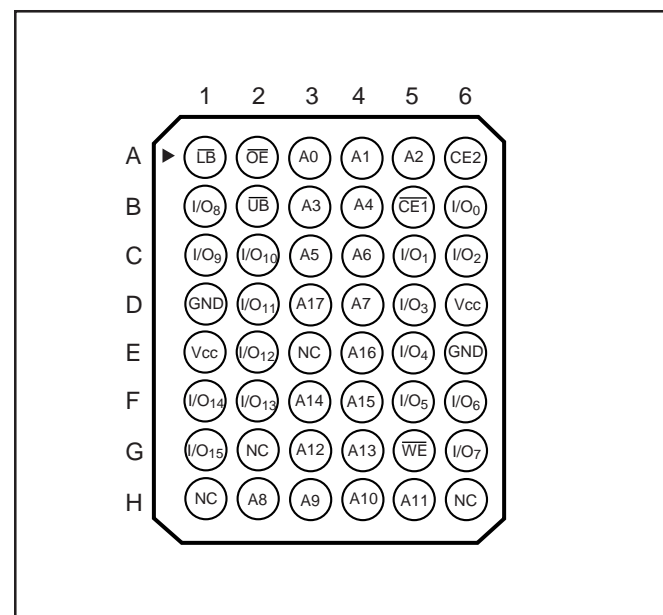
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## PIN CONFIGURATIONS

### 44-Pin TSOP-2



### 48-Pin TF-BGA (TOP View)



## PIN DESCRIPTIONS

A0-A18	Address Inputs
I/O0-I/O15	Data Input/Output
$\overline{CE1}$	Chip Enable1 Input
$\overline{CE2}$	Chip Enable2 Input, BGA only
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input

$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

## TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0-I/O7	I/O8-I/O15	Vcc Current
Not Selected	X	H	X	X	X	X	High-Z	High-Z	Standby
	X	X	L	X	X	X	High-Z	High-Z	Standby
	X	L	H	X	H	H	High-Z	High-Z	Standby
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	Active
	H	L	H	H	X	L	High-Z	High-Z	Active
Read	H	L	H	L	L	H	DOUT	High-Z	Active
	H	L	H	L	H	L	High-Z	DOUT	Active
	H	L	H	L	L	L	DOUT	DOUT	Active
Write	L	L	H	X	L	H	DIN	High-Z	Active
	L	L	H	X	H	L	High-Z	DIN	Active
	L	L	H	X	L	L	DIN	DIN	Active

## OPERATING RANGE

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	2.7V- 3.6V
Industrial	−40°C to +85°C	2.7V - 3.6V

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	−0.5 to V <sub>CC</sub> + 0.5	V
T <sub>BIAS</sub>	Temperature Under Bias	−40 to +85	°C
V <sub>CC</sub>	V <sub>CC</sub> related to GND	−0.3 to +4.0	V
T <sub>STG</sub>	Storage Temperature	−65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

### Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = −1 mA	2.0	—	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	—	0.4	V
V <sub>IH</sub> <sup>(1)</sup>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.2	V
V <sub>IL</sub> <sup>(2)</sup>	Input LOW Voltage <sup>(1)</sup>		−0.2	0.4	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	−1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , OUTPUTS DISABLED	−1	1	μA

### Notes:

1. V<sub>IH</sub>(max.) = V<sub>CC</sub> + 0.2V for pulse width less than 10ns.
2. V<sub>IL</sub>(min.) = −2.0V for pulse width less than 10 ns.

## CAPACITANCE<sup>(1)</sup>

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

### Notes:

1. Tested initially and after any design or process changes that may affect these parameters.

## AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Times	5 ns
Input Reference Level	1.3V
Output Reference Level	1.5V
Output Load	See Figures 1 and 2

## AC TEST LOADS

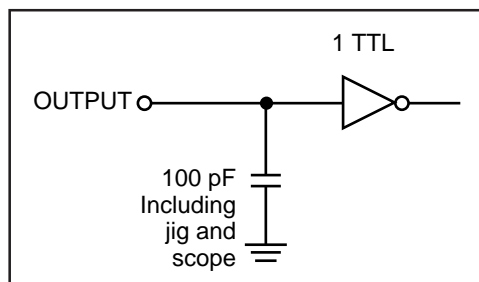


Figure 1

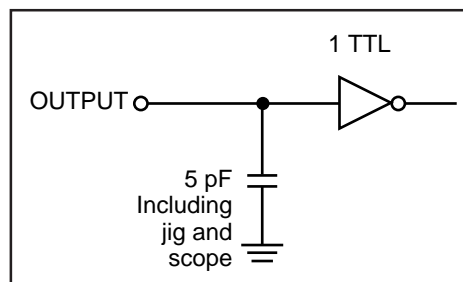


Figure 2

## IS62LV51216L POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions		-55		-70		-100		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>CC</sub>	V <sub>CC</sub> Dynamic Operating Supply Current	V <sub>CC</sub> = 3.0V., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com. Ind.	— —	30 35	— —	25 30	— —	20 25	mA
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , f = 0 $\overline{CE1}$ = V <sub>IH</sub> , CE2 = V <sub>IL</sub>	Com. Ind.	— —	0.2 0.3	— —	0.2 0.3	— —	0.2 0.3	mA
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>CC</sub> = Max., $\overline{CE1} \geq V_{CC} - 0.2V$ , or CE2 $\leq 0.2V$ other input = 0-V <sub>CC</sub> , f = 0	Com. Ind.	— —	35 50	— —	35 50	— —	35 50	$\mu A$
<b>OR</b>										
	ULB Control	V <sub>CC</sub> = Max., $\overline{CE1}$ = V <sub>IL</sub> , CE2 = V <sub>IH</sub> V <sub>IN</sub> $\leq 0.2V$ , f = 0, $\overline{UB} / \overline{LB} \geq V_{CC} - 0.2V$								

### Note:

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

## IC62LV51216LL POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions		-55		-70		-100		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>CC</sub>	V <sub>CC</sub> Dynamic Operating Supply Current	V <sub>CC</sub> = 3.0V I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com. Ind.	— —	25 30	— —	20 25	— —	15 20	mA
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , CE1 = V <sub>IH</sub> , CE2 = V <sub>IL</sub>	Com. Ind.	— —	0.2 0.3	— —	0.2 0.3	— —	0.2 0.3	mA
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>CC</sub> = Max., f = 0 CE1 ≥ V <sub>CC</sub> - 0.2V, or CE2 ≤ 0.2V other input = 0-V <sub>CC</sub> , f = 0	Com. Ind.	— —	15 25	— —	15 25	— —	15 25	μA
<b>OR</b>										
	ULB Control	V <sub>CC</sub> = Max., CE1 = V <sub>IL</sub> , CE2 = V <sub>IH</sub> V <sub>IN</sub> ≤ 0.2V, f = 0, UB / LB ≥ V <sub>CC</sub> - 0.2V								

### Note:

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

## READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

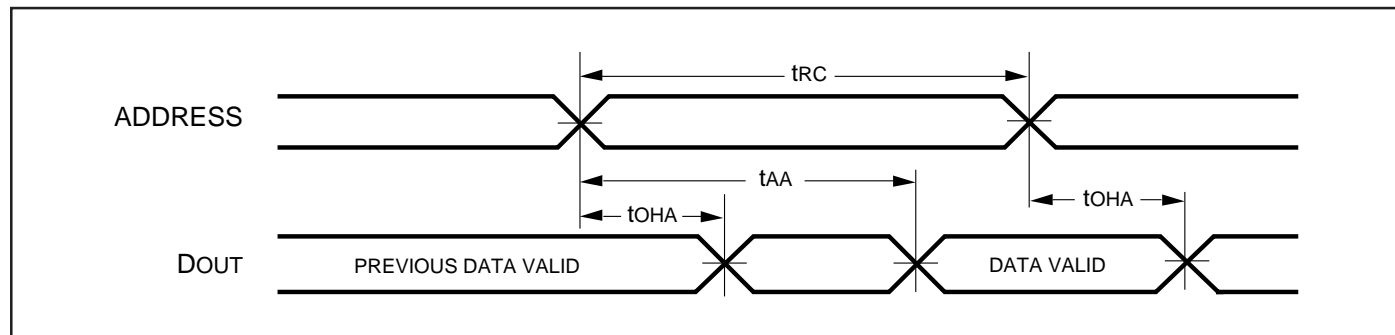
Symbol	Parameter	-55		-70		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	55	—	70	—	100	—	ns
t <sub>AA</sub>	Address Access Time	—	55	—	70	—	100	ns
t <sub>OHA</sub>	Output Hold Time	10	—	10	—	15	—	ns
t <sub>ACE</sub>	CE Access Time	—	55	—	70	—	100	ns
t <sub>DOE</sub>	OE Access Time	—	30	—	38	—	50	ns
t <sub>HZOE</sub> <sup>(2)</sup>	OE to High-Z Output	—	20	—	25	—	30	ns
t <sub>LZOE</sub> <sup>(2)</sup>	OE to Low-Z Output	5	—	5	—	5	—	ns
t <sub>HZCE</sub> <sup>(2)</sup>	CE1 or CE2 to High-Z Output	0	20	0	25	0	30	ns
t <sub>LZCE</sub> <sup>(2)</sup>	CE1 and CE2 to Low-Z Output	10	—	10	—	10	—	ns
t <sub>BA</sub>	LB, UB Access Time	—	55	—	70	—	100	ns
t <sub>HZB</sub>	LB, UB to High-Z Output	0	25	0	25	0	35	ns
t <sub>LZB</sub>	LB, UB to Low-Z Output	0	—	0	—	0	—	ns

### Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
- Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

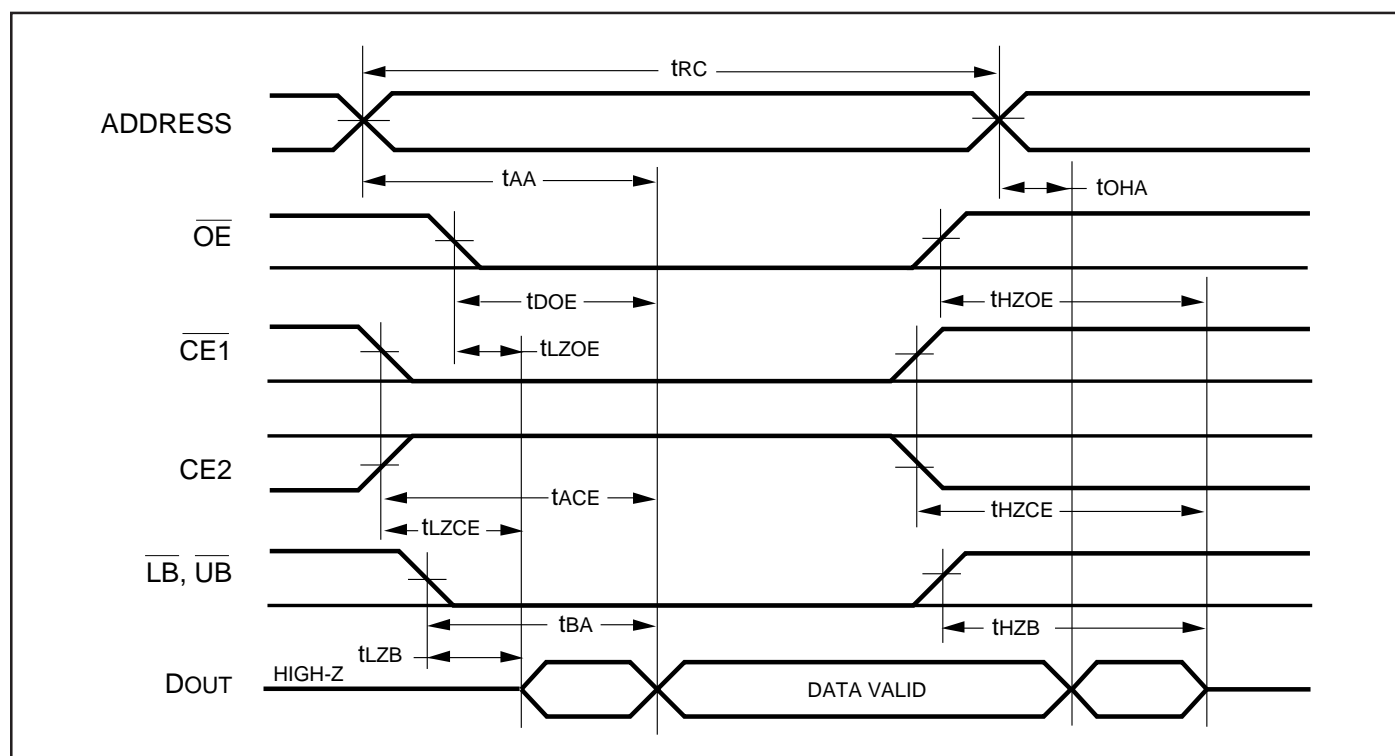
## AC TEST LOADS

### READ CYCLE NO.1<sup>(1,2)</sup> (Address Controlled) ( $\overline{CE1} = \overline{OE} = V_{IL}$ , $CE2 = V_{IH}$ , $\overline{UB}$ or $\overline{LB} = V_{IL}$ )



## AC WAVEFORMS

### READ CYCLE NO. 2<sup>(1,3)</sup> ( $\overline{OE}$ , Controlled)



#### Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE1}$ ,  $\overline{UB}$ , or  $\overline{LB} = V_{IL}$ ,  $CE2 = V_{IH}$
3. Address is valid prior to or coincident with  $\overline{CE1}$  LOW and  $CE2$  HIGH transitions.

## WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup> (Over Operating Range)

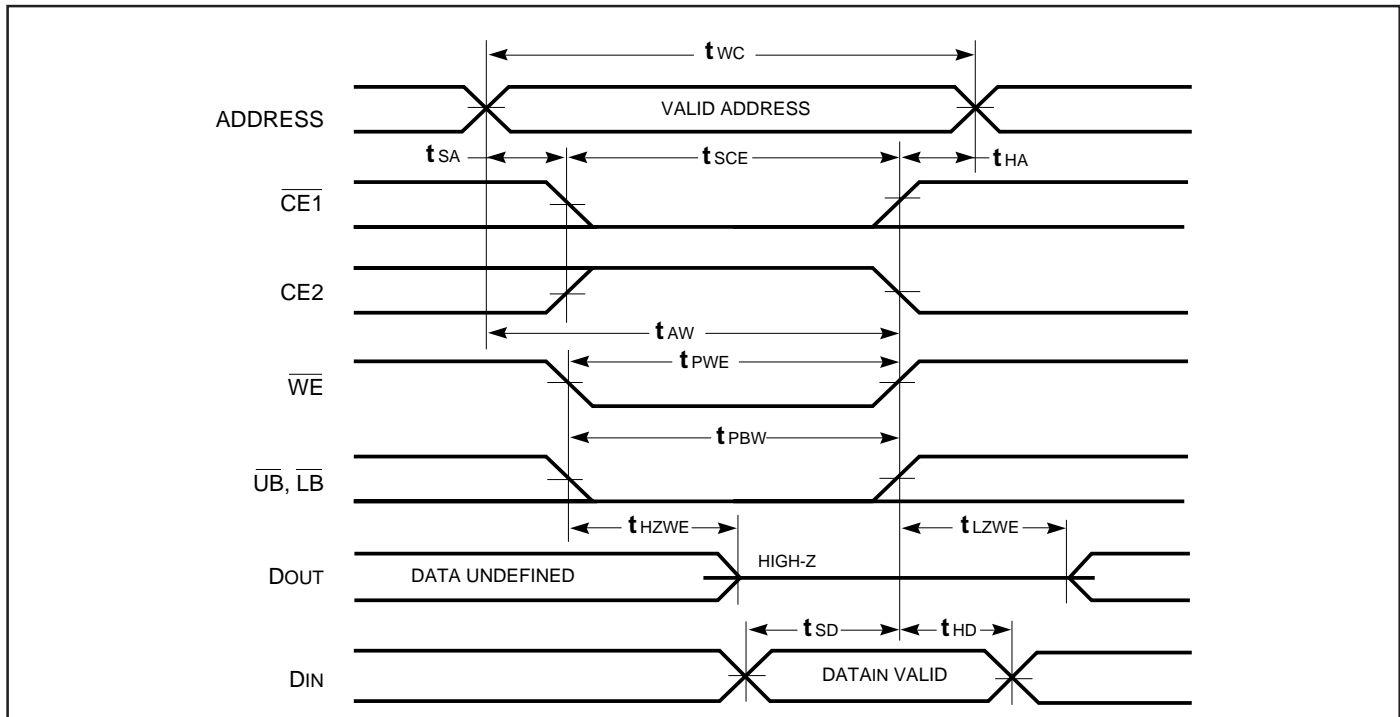
Symbol	Parameter	-55		-70		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{WC}$	Write Cycle Time	55	—	70	—	100	—	ns
$t_{SCE}$	$\overline{CE1}$ Low and CE2 HIGH to Write End	50	—	65	—	80	—	ns
$t_{AW}$	Address Setup Time to Write End	50	—	65	—	80	—	ns
$t_{HA}$	Address Hold from Write End	0	—	0	—	0	—	ns
$t_{SA}$	Address Setup Time	0	—	0	—	0	—	ns
$t_{PWB}$	$\overline{LB}$ , $\overline{UB}$ Valid to End of Write	45	—	60	—	80	—	ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	45	—	55	—	80	—	ns
$t_{SD}$	Data Setup to Write End	25	—	30	—	40	—	ns
$t_{HD}$	Data Hold from Write End	0	—	0	—	0	—	ns
$t_{HZWE}^{(3)}$	$\overline{WE}$ LOW to High-Z Output	—	30	—	30	—	40	ns
$t_{LZWE}^{(3)}$	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

### Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
- The internal write time is defined by the overlap of  $\overline{CE1}$  LOW, and  $\overline{UB}$  or  $\overline{LB}$ ,  $\overline{WE}$  LOW, and CE2 HIGH. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
- Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

## AC WAVEFORMS

### WRITE CYCLE NO. 1<sup>(1,2)</sup> ( $\overline{CE1}$ or CE2, Controlled, $\overline{OE}$ = HIGH or LOW)

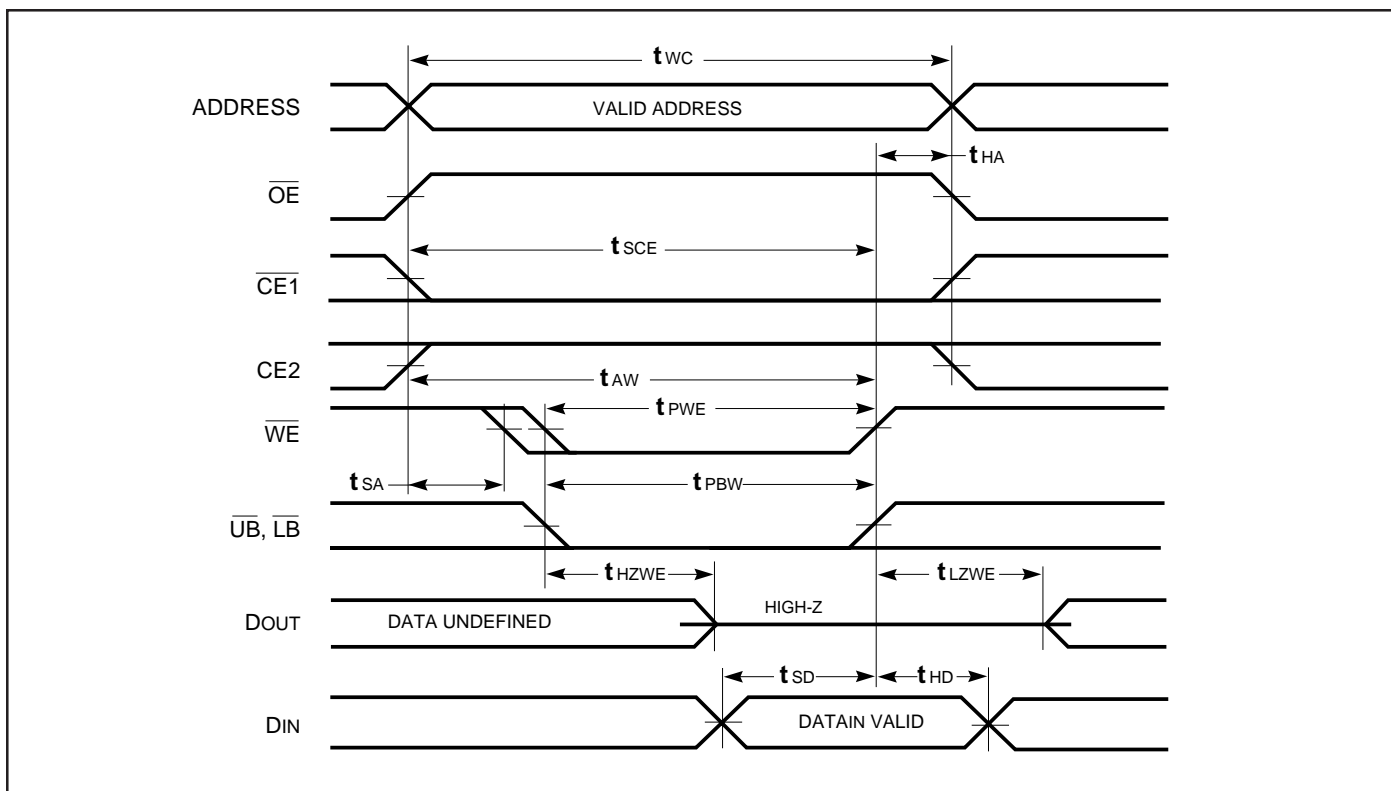


### Notes:

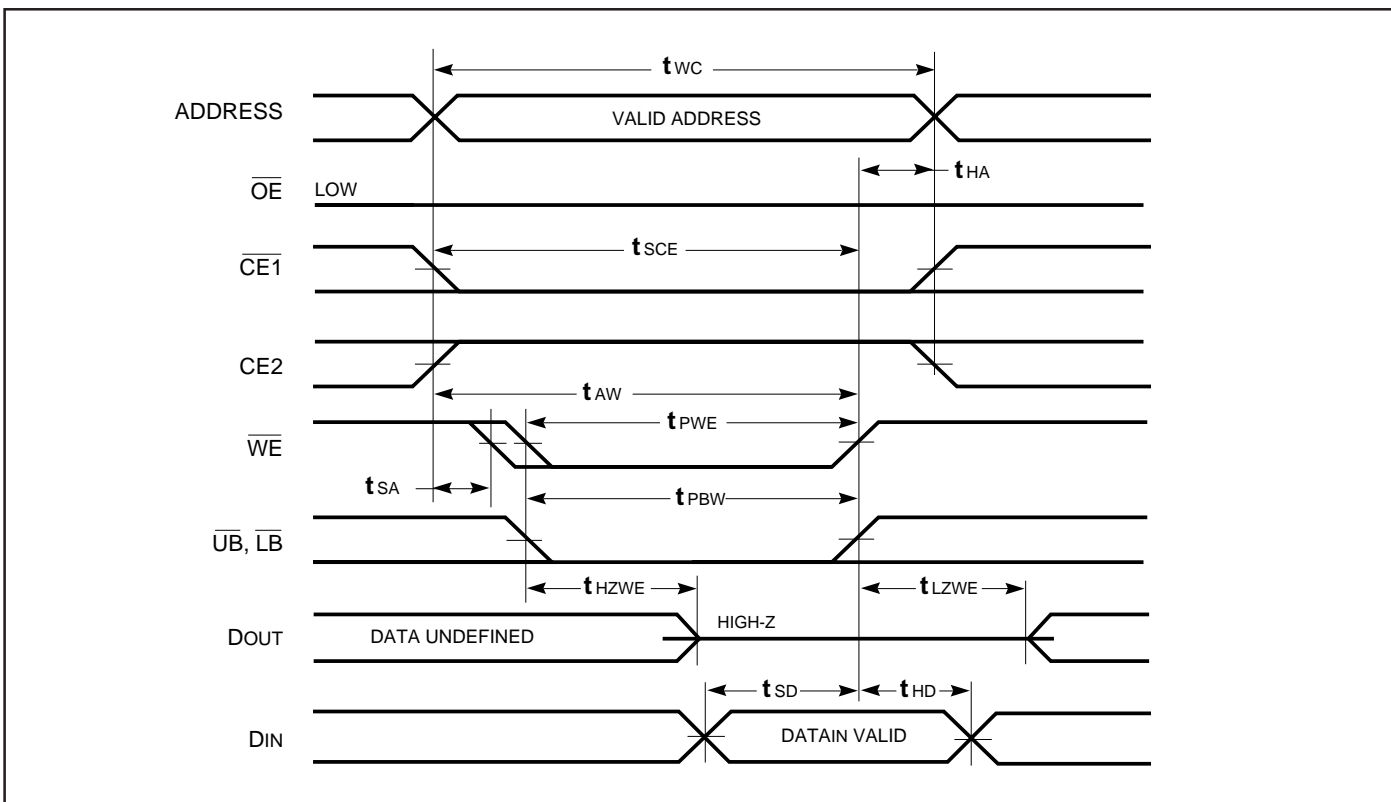
- WRITE is an internally generated signal asserted during an overlap of the  $\overline{WE}$ ,  $\overline{CE1} = V_{IL}$ ,  $CE2 = V_{IH}$  and at least one of the  $\overline{LB}$  and  $\overline{UB}$  inputs being in the LOW state.



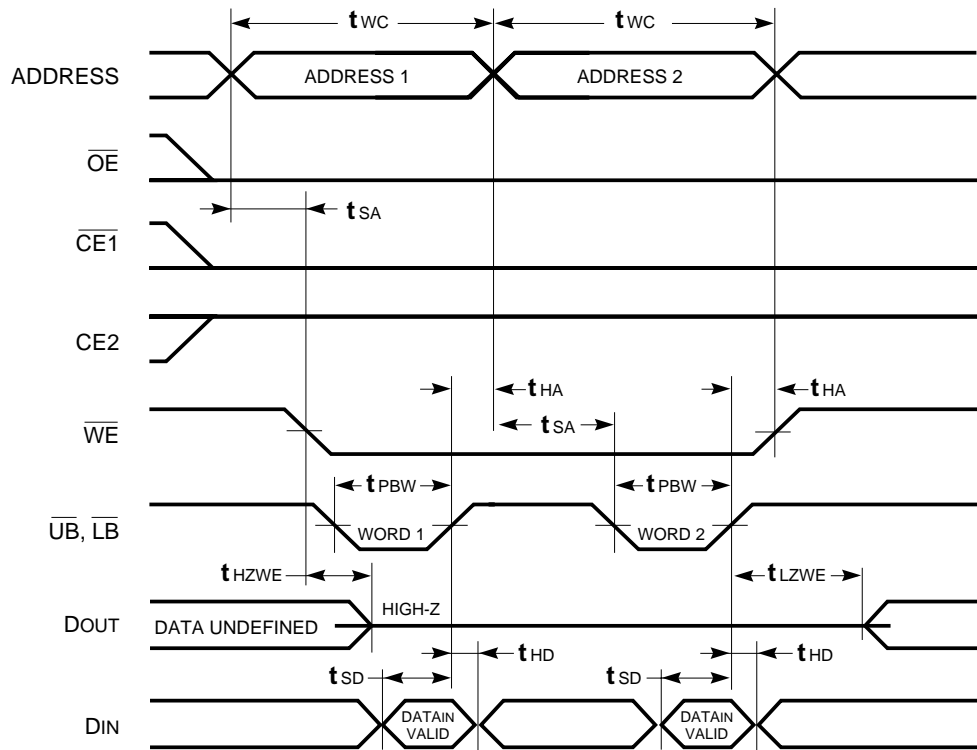
**WRITE CYCLE NO. 2** ( $\overline{WE}$  Controlled;  $\overline{OE}$  is HIGH During Write Cycle)



**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled;  $\overline{OE}$  is LOW During Write Cycle)



**WRITE CYCLE NO. 4** ( $\overline{UB}$  /  $\overline{LB}$  Controlled)



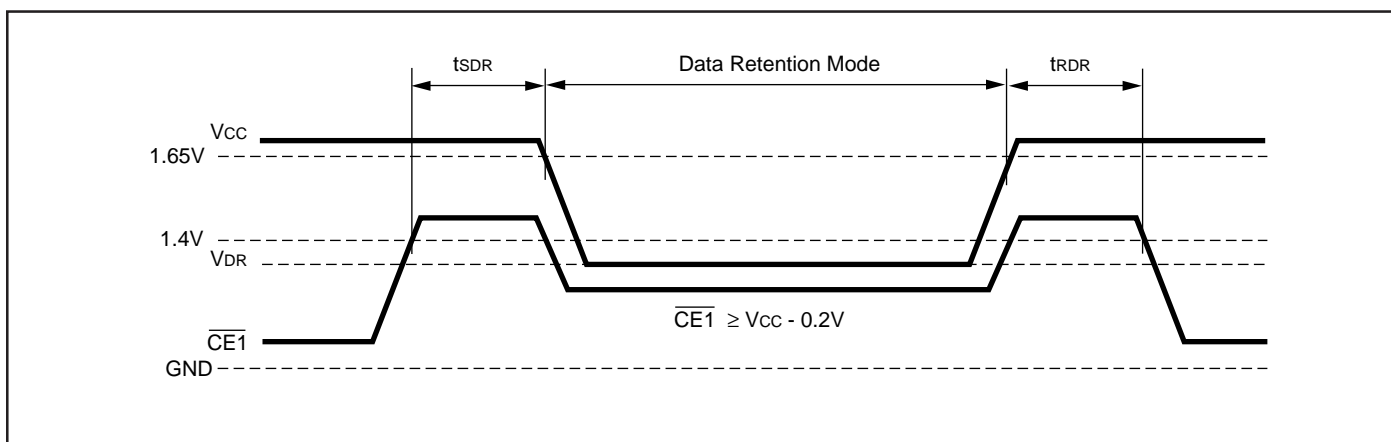
**DATA RETENTION SWITCHING CHARACTERISTICS**

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention	See Data Retention Waveform	1.5	3.6	V
$I_{DR}$	Data Retention Current	$V_{CC} = 1.5V$ , $\overline{CE1} \geq V_{CC} - 0.2V^{(1)}$			$\mu A$
		Com. (-L)	—	20	
		Com. (-LL)	—	13	
		Ind. (-L)	—	30	
		Ind. (-LL)	—	23	
$t_{SDR}$	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
$t_{RDR}$	Recovery Time	See Data Retention Waveform	10	—	ns

**Notes:**

- 1)  $\overline{CE1} \geq V_{CC} - 0.2V$ ,  $\overline{CE2} \geq V_{CC} - 0.2V$ , ( $\overline{CE1}$  controlled) or
- 2)  $0V \leq \overline{CE2} \leq 0.2V$  ( $\overline{CE2}$  controlled) or
- 3)  $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2V$ ,  $\overline{CE2} \geq V_{CC} - 0.2V$  ( $\overline{LB}/\overline{UB}$  controlled)

## DATA RETENTION WAVEFORM ( $\overline{CE1}$ Controlled)



## ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IC62LV51216L-55T	TSOP-2
	IC62LV51216L-55B	8*10mm TF-BGA
70	IC62LV51216L-70T	TSOP-2
	IC62LV51216L-70B	8*10mm TF-BGA
100	IC62LV51216L-100T	TSOP-2
	IC62LV51216L-100B	8*10mm TF-BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IC62LV51216L-55TI	TSOP-2
	IC62LV51216L-55BI	8*10mm TF-BGA
70	IC62LV51216L-70TI	TSOP-2
	IC62LV51216L-70BI	8*10mm TF-BGA
100	IC62LV51216L-100TI	TSOP-2
	IC62LV51216L-100BI	8*10mm TF-BGA

## ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IC62LV51216LL-55T	TSOP-2
	IC62LV51216LL-55B	8*10mm TF-BGA
70	IC62LV51216LL-70T	TSOP-2
	IC62LV51216LL-70B	8*10mm TF-BGA
100	IC62LV51216LL-100T	TSOP-2
	IC62LV51216LL-100B	8*10mm TF-BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IC62LV51216LL-55TI	TSOP-2
	IC62LV51216LL-55BI	8*10mm TF-BGA
70	IC62LV51216LL-70TI	TSOP-2
	IC62LV51216LL-70BI	8*10mm TF-BGA
100	IC62LV51216LL-100TI	TSOP-2
	IC62LV51216LL-100BI	8*10mm TF-BGA



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