



GENERAL DESCRIPTION



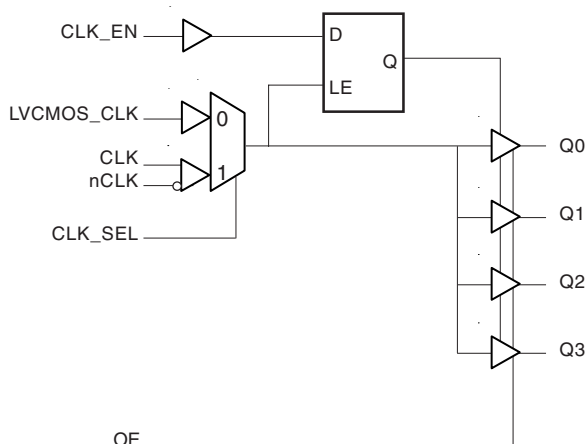
The ICS8305I is a low skew, 1-to-4, Differential/LVCMOS-to-LVCMOS/LVTTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8305I has selectable clock inputs that accept either differential or single ended input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin. Outputs are forced LOW when the clock is disabled. A separate output enable pin controls whether the outputs are in the active or high impedance state.

Guaranteed output and part-to-part skew characteristics make the ICS8305I ideal for those applications demanding well-defined performance and repeatability.

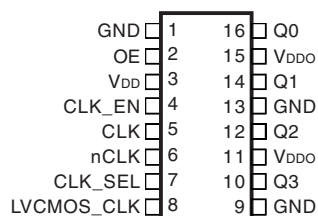
FEATURES

- 4 LVCMOS/LVTTL outputs
- Selectable differential or LVCMOS/LVTTL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- LVCMOS_CLK supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 350MHz
- Output skew: 40ps (maximum)
- Part-to-part skew: 700ps (maximum)
- Additive phase jitter, RMS: 0.04ps (typical)
- 3.3V core, 3.3V, 2.5V or 1.8V output operating supply
- -40°C to 85°C ambient operating temperature
- Lead-Free package fully RoHS compliant

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8305I

16-Lead TSSOP

4.4mm x 3.0mm x 0.92mm package body

G Package

Top View



TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|----------------|------------------|--------|---------------------|--|
| 1, 9, 13 | GND | Power | | Power supply ground. |
| 2 | OE | Input | Pullup | Output enable. When LOW, outputs are in HIGH impedance state. When HIGH, outputs are active. LVCMOS / LVTTL interface levels. |
| 3 | V _{DD} | Power | | Core supply pin. |
| 4 | CLK_EN | Input | Pullup | Synchronizing clock enable. When LOW, the output clocks are disabled. When HIGH, output clocks are enabled. LVCMOS / LVTTL interface levels. |
| 5 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 6 | nCLK | Input | Pullup/ Pulldown | Inverting differential clock input. V _{DD} /2 default when left floating. |
| 7 | CLK_SEL | Input | Pullup | Clock select input. When HIGH, selects CLK, nCLK inputs. When LOW, selects LVCMOS_CLK input. LVCMOS / LVTTL interface levels. |
| 8 | LVCMOS_CLK | Input | Pulldown | LVCMOS / LVTTL clock input. |
| 10, 12, 14, 16 | Q3, Q2, Q1, Q0 | Output | | Clock outputs. LVCMOS / LVTTL interface levels. |
| 11, 15 | V _{DDO} | Power | | Output supply pins. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|--|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |
| C _{PD} | Power Dissipation Capacitance (per output) | | | 11 | | pF |
| R _{OUT} | Output Impedance | | 5 | 7 | 12 | Ω |



TABLE 3A. CONTROL INPUT FUNCTION TABLE

| Inputs | | | | Outputs |
|--------|--------|---------|-----------------|---------------|
| OE | CLK_EN | CLK_SEL | Selected Source | Q0:Q3 |
| 1 | 0 | 0 | LVCMOS_CLK | Disabled; LOW |
| 1 | 0 | 1 | CLK, nCLK | Disabled; LOW |
| 1 | 1 | 0 | LVCMOS_CLK | Enabled |
| 1 | 1 | 1 | CLK, nCLK | Enabled |
| 0 | X | X | | HiZ |

NOTE: After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

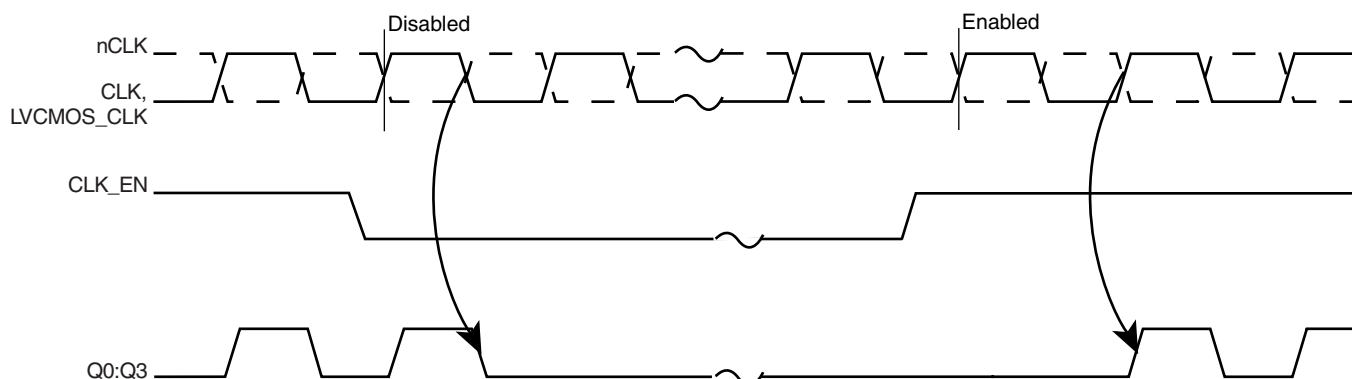


FIGURE 1. CLK_EN TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| | |
|--|---------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, V_O | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, θ_{JA} | 89°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| | | | 2.375 | 2.5 | 2.625 | V |
| | | | 1.65 | 1.8 | 1.95 | V |
| I_{DD} | Power Supply Current | | | | 21 | mA |
| I_{DDO} | Output Supply Current | | | | 5 | mA |

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|------------------------------|----------------------------|--------------------------------|---------|----------------|---------------|
| V_{IH} | Input High Voltage | CLK_EN, CLK_SEL, OE | 2 | | $V_{DD} + 0.3$ | V |
| | | LVCMOS_CLK | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | CLK_EN, CLK_SEL, OE | -0.3 | | 0.8 | V |
| | | LVCMOS_CLK | -0.3 | | 1.3 | V |
| I_{IH} | Input High Current | CLK_EN, CLK_SEL, OE | $V_{DD} = V_{IN} = 3.465V$ | | 5 | μA |
| | | LVCMOS_CLK | $V_{DD} = V_{IN} = 3.465V$ | | 150 | μA |
| I_{IL} | Input Low Current | CLK_EN, CLK_SEL, OE | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | μA |
| | | LVCMOS_CLK | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | μA |
| V_{OH} | Output High Voltage; NOTE 1 | $V_{DDO} = 3.3V \pm 5\%$ | 2.6 | | | V |
| | | $V_{DDO} = 2.5V \pm 5\%$ | 1.8 | | | V |
| | | $V_{DDO} = 1.8V \pm 0.15V$ | $V_{DDO} - 0.3$ | | | V |
| V_{OL} | Output Low Voltage; NOTE 1 | $V_{DDO} = 3.3V \pm 5\%$ | | | 0.5 | V |
| | | $V_{DDO} = 2.5V \pm 5\%$ | | | 0.5 | V |
| | | $V_{DDO} = 1.8V \pm 0.15V$ | | | 0.4 | V |
| I_{OZL} | Output Tristate Current Low | | -5 | | | μA |
| I_{OZH} | Output Tristate Current High | | | | 5 | μA |

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information, Output Load Test Circuit.



TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|---|--|-----------|---------|-----------------|---------|
| I_{IH} | Input High Current | nCLK $V_{IN} = V_{DD} = 3.465V$ | | | 150 | μA |
| | | CLK $V_{IN} = V_{DD} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | nCLK $V_{IN} = 0V, V_{DD} = 3.465V$ | -150 | | | μA |
| | | CLK $V_{IN} = 0V, V_{DD} = 3.465V$ | -5 | | | μA |
| V_{PP} | Peak-to-Peak Input Voltage | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | GND + 0.5 | | $V_{DD} - 0.85$ | V |

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is $V_{DD} + 0.3V$.

NOTE 2: Common mode voltage is defined as V_{IH} .

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|---|---|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | Ref = CLK/nCLK | | | 350 | MHz |
| | | Ref = LVCMOS_CLK | | | 300 | MHz |
| t_{pLH} | Propagation Delay, Low to High | LVCMOS_CLK; NOTE 1A CLK, nCLK; NOTE 1B | 1.75 | | 2.8 | ns |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 6 | Measured on the Rising Edge | | | 40 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 6 | | | | 700 | ps |
| f_{jit} | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5 | | | 0.04 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 100 | | 700 | ps |
| odc | Output Duty Cycle | $f \leq 200MHz$ | 45 | | 55 | % |
| | | $f > 200MHz$ | 42 | | 58 | % |
| t_{EN} | Output Enable Time; NOTE 4 | | | | 5 | ns |
| t_{DIS} | Output Disable Time; NOTE 4 | | | | 5 | ns |

NOTE 1A: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 1B: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at $V_{DDO}/2$.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

NOTE 5: Driving only one input clock.

NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.



TABLE 5B. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|---|---|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | Ref = CLK/nCLK | | | 350 | MHz |
| | | Ref = LVCMOS_CLK | | | 300 | MHz |
| t_{pLH} | Propagation Delay, Low to High | LVCMOS_CLK; NOTE 1A CLK, nCLK; NOTE 1B | 1.75 | | 2.95 | ns |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 6 | Measured on the Rising Edge | | | 40 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 6 | | | | 800 | ps |
| t_{jit} | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5 | | | 0.04 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 100 | | 700 | ps |
| odc | Output Duty Cycle | $f \leq 166MHz$ | 45 | | 55 | % |
| | | $f > 166MHz$ | 42 | | 58 | % |
| t_{EN} | Output Enable Time; NOTE 4 | | | | 5 | ns |
| t_{DIS} | Output Disable Time; NOTE 4 | | | | 5 | ns |

NOTE 1A: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 1B: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

NOTE 5: Driving only one input clock.

NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.15V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|---|---|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | Ref = CLK/nCLK | | | 350 | MHz |
| | | Ref = LVCMOS_CLK | | | 300 | MHz |
| t_{pLH} | Propagation Delay, Low to High | LVCMOS_CLK; NOTE 1A CLK, nCLK; NOTE 1B | 1.75 | | 3.7 | ns |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 6 | Measured on the Rising Edge | | | 45 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 6 | | | | 900 | ps |
| t_{jit} | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5 | | | 0.04 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 100 | | 700 | ps |
| odc | Output Duty Cycle | $f \leq 166MHz$ | 45 | | 55 | % |
| | | $f > 166MHz$ | 42 | | 58 | % |
| t_{EN} | Output Enable Time; NOTE 4 | | | | 5 | ns |
| t_{DIS} | Output Disable Time; NOTE 4 | | | | 5 | ns |

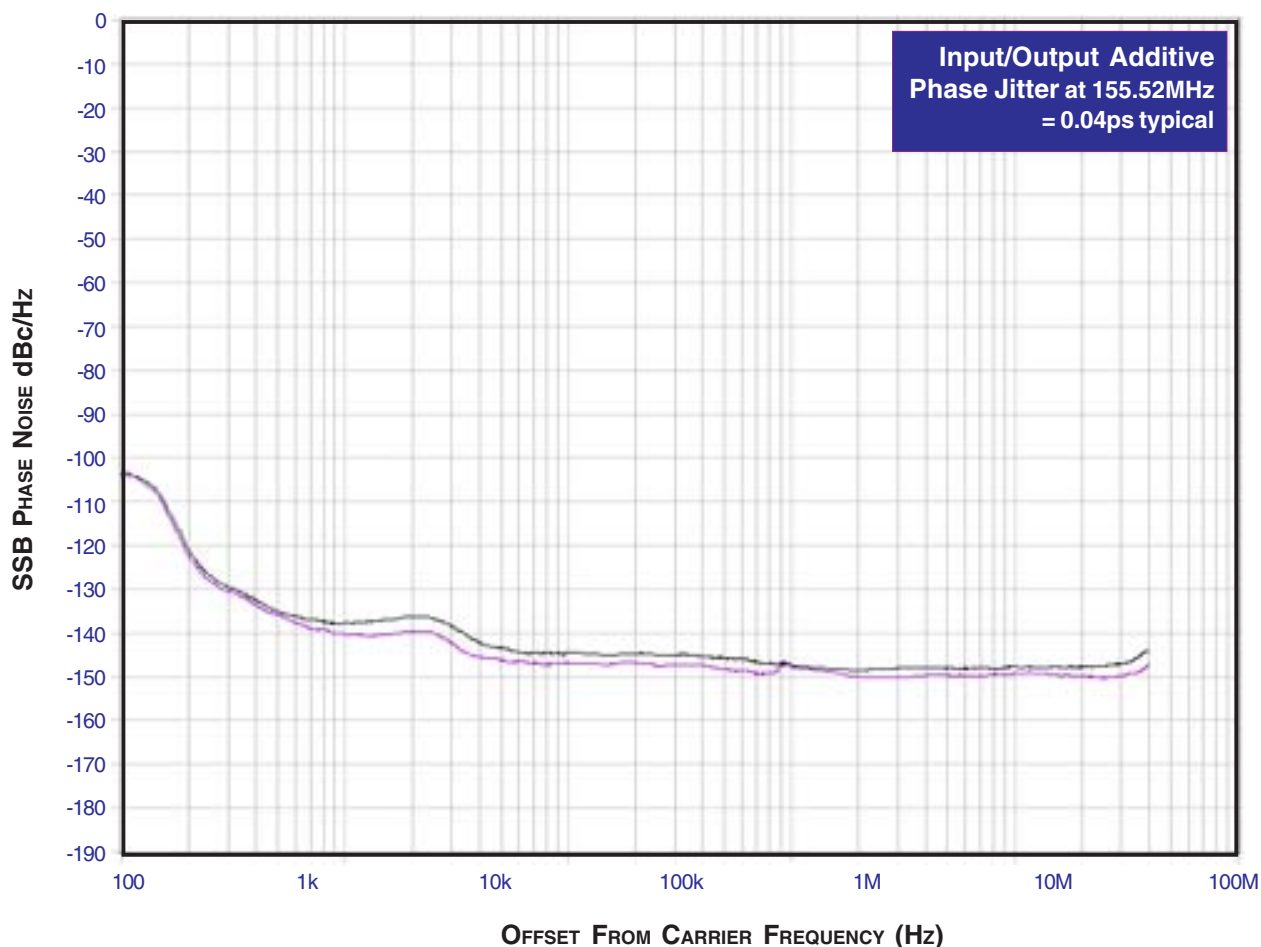
For notes, see Table 5B.



ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in

the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

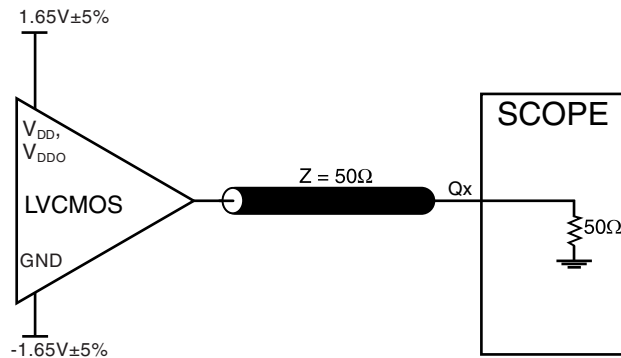


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The de-

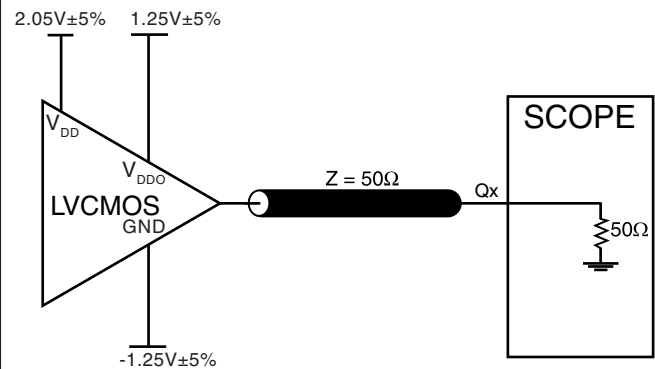
vice meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.



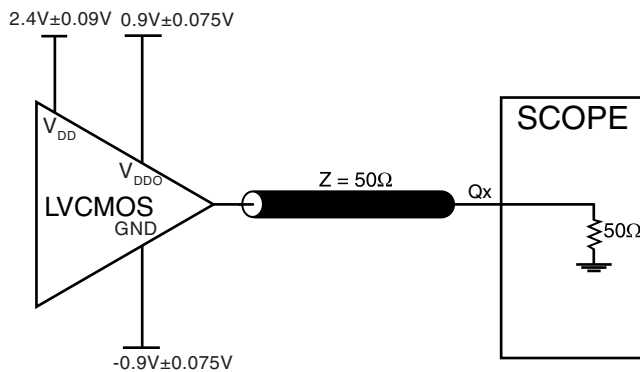
PARAMETER MEASUREMENT INFORMATION



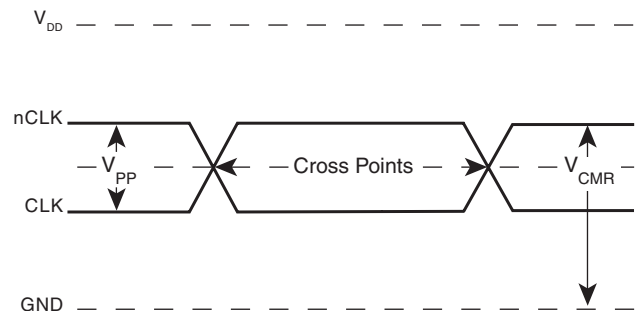
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



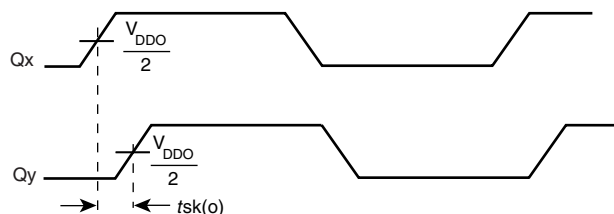
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



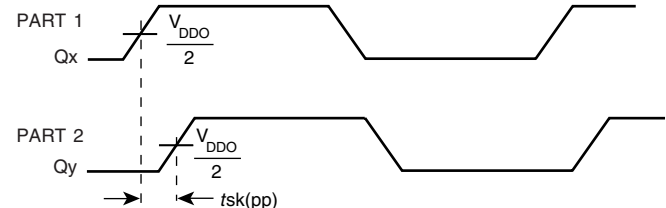
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



DIFFERENTIAL INPUT LEVEL



OUTPUT SKEW



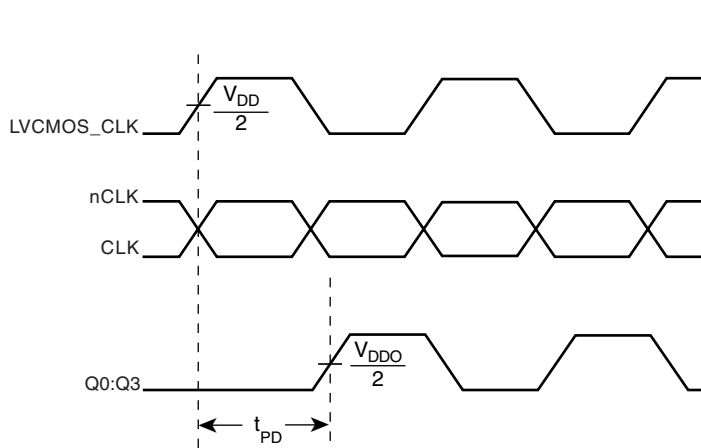
PART-TO-PART SKEW



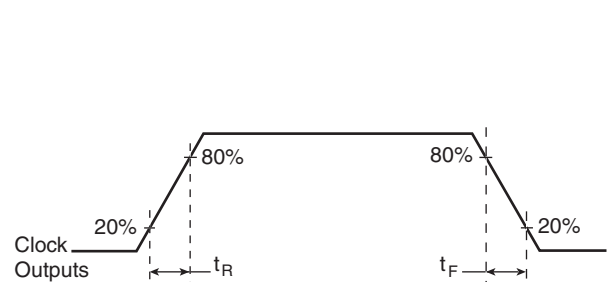
Integrated
Circuit
Systems, Inc.

ICS8305I

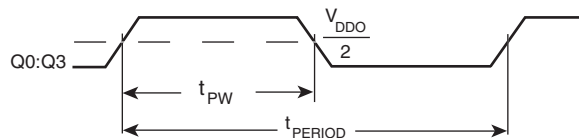
LOW SKEW, 1-TO-4, MULTIPLEXED DIFFERENTIAL/
LVCMOS-TO-LVCMOS/LVTTL FANOUT BUFFER



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



$$\text{odc} = \frac{t_{\text{PW}}}{t_{\text{PERIOD}}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

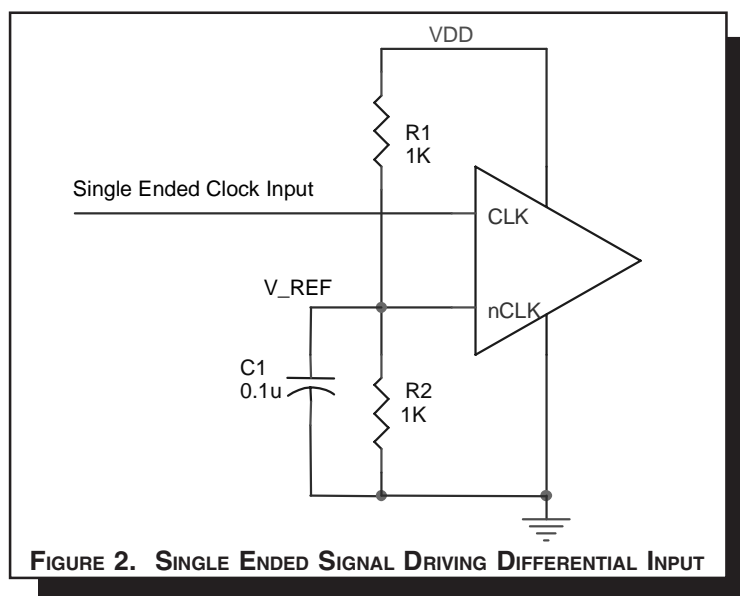


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT



DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A*, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

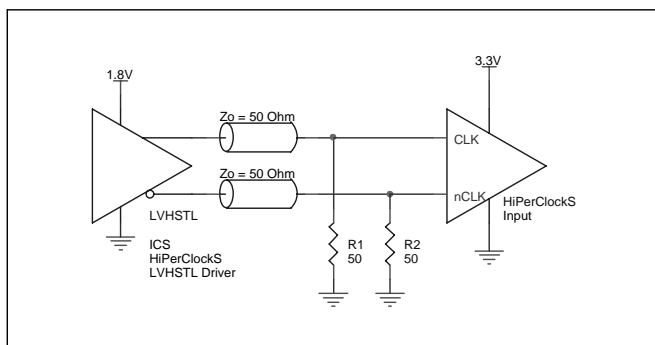


FIGURE 3A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER

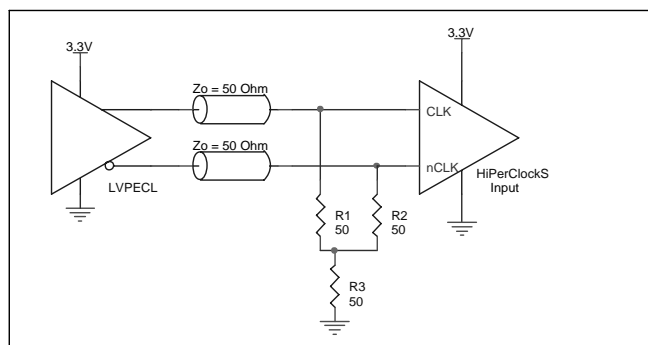


FIGURE 3B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

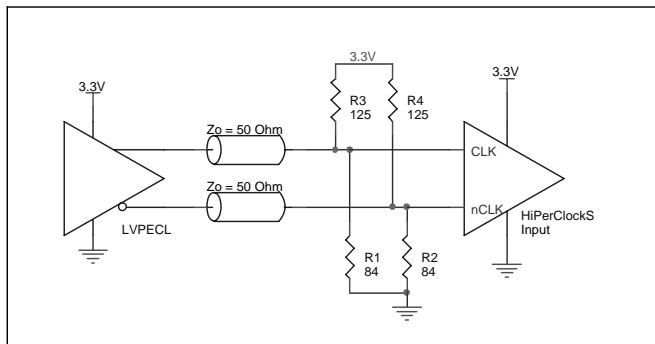


FIGURE 3C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

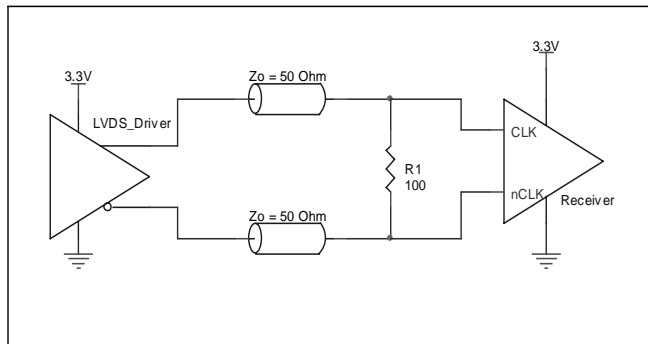


FIGURE 3D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

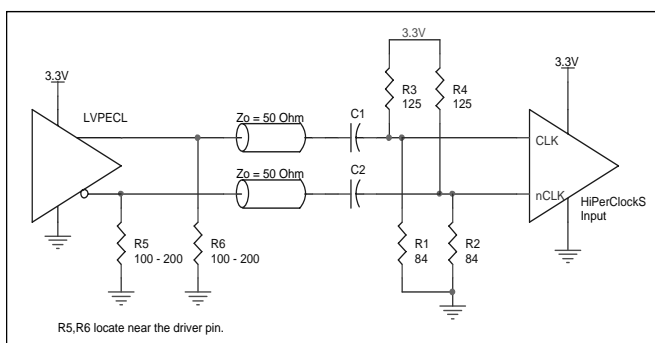


FIGURE 3E. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE



SCHEMATIC EXAMPLE

This application note provides general design guide using ICS8305I LVCMOS buffer. Figure 4 shows a schematic example of the ICS8305I LVCMOS clock buffer. In this example, the input

is driven by an LVCMOS driver. CLK_EN is set at logic low to select LVCMOS_CLK input.

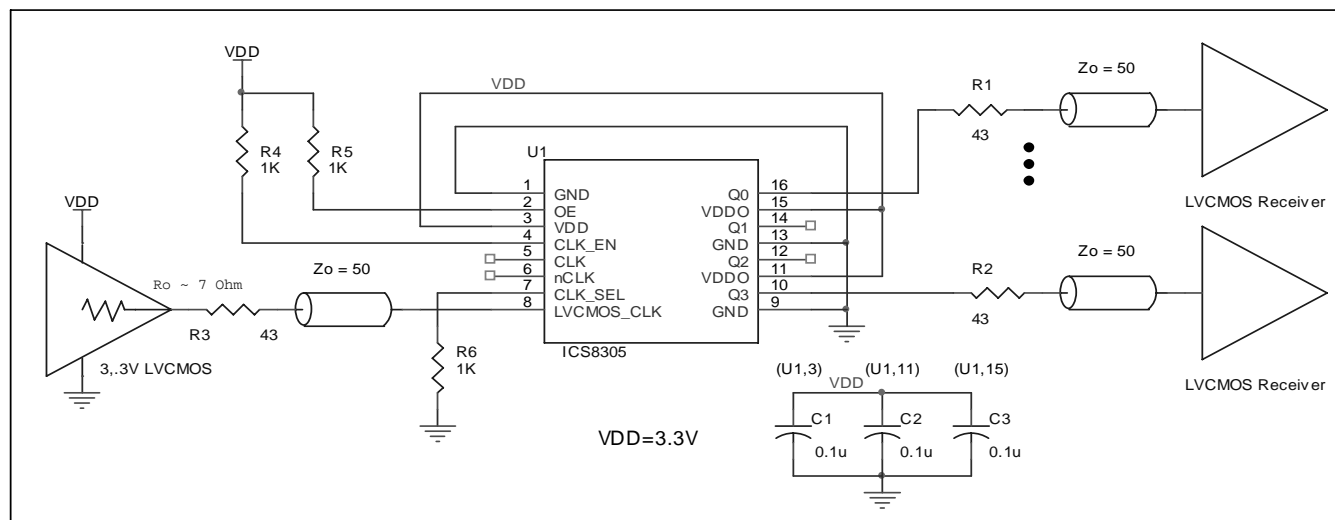


FIGURE 4. EXAMPLE ICS8305I LVCMOS CLOCK OUTPUT BUFFER SCHEMATIC

RELIABILITY INFORMATION

TABLE 6. θ_{JA} vs. AIR FLOW TABLE FOR 16 LEAD TSSOP

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|-----------|-----------|-----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 137.1°C/W | 118.2°C/W | 106.8°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 89.0°C/W | 81.8°C/W | 78.1°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8305I is: 459



PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

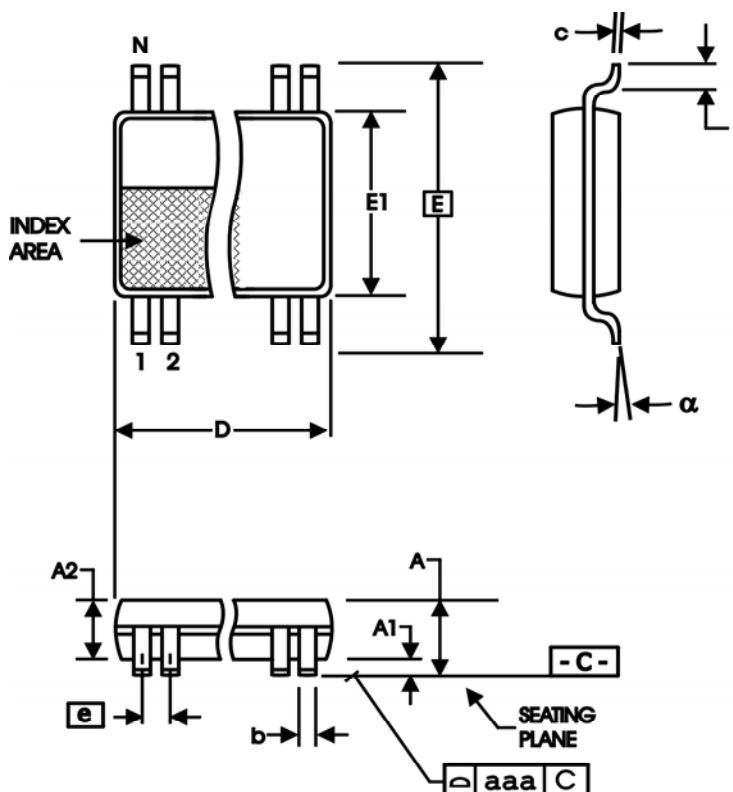


TABLE 7. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|---------|
| | Minimum | Maximum |
| N | 16 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 4.90 | 5.10 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153



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ICS8305I

LOW SKEW, 1-TO-4, MULTIPLEXED DIFFERENTIAL/ LVCMOS-TO-LVCMOS/LVTTL FANOUT BUFFER

TABLE 8. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|----------|---------------------------|--------------------|---------------|
| ICS8305AGI | 8305AGI | 16 Lead TSSOP | tube | -40°C to 85°C |
| ICS8305AGIT | 8305AGI | 16 Lead TSSOP | 2500 tape & reel | -40°C to 85°C |
| ICS8305AGILF | 8305AGIL | 16 Lead "Lead-Free" TSSOP | tube | -40°C to 85°C |
| ICS8305AGILFT | 8305AGIL | 16 Lead "Lead-Free" TSSOP | 2500 tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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LOW SKEW, 1-TO-4, MULTIPLEXED DIFFERENTIAL/
LVCMOS-TO-LVCMOS/LVTTL FANOUT BUFFER

REVISION HISTORY SHEET

| Rev | Table | Page | Description of Change | Date |
|-----|-----------|------------|---|---------|
| A | T8 | 14 | Ordering Information table - corrected Part/Order Number typo from ICS88305AGIT to ICS8305AGIT. | 1/20/04 |
| B | T5A - T5C | 5 & 6 7 | AC Characteristics Tables - changed tjit from 0.05ps typical to 0.04ps typical. Updated Additive Phase Jitter plot. | 2/26/04 |
| B | T1 | 2 | Pin Description Table - corrected CLK_EN description. | 12/7/04 |
| B | T8 | 14 | Ordering Information Table - added Lead-Free part number | 5/19/05 |