



Description

The ICS181-01 generates a low EMI output clock from a clock or crystal input. The device uses ICS' proprietary mix of analog and digital Phase-Locked Loop (PLL) technology to spread the frequency spectrum of the output, thereby reducing the frequency amplitude peaks by several dB.

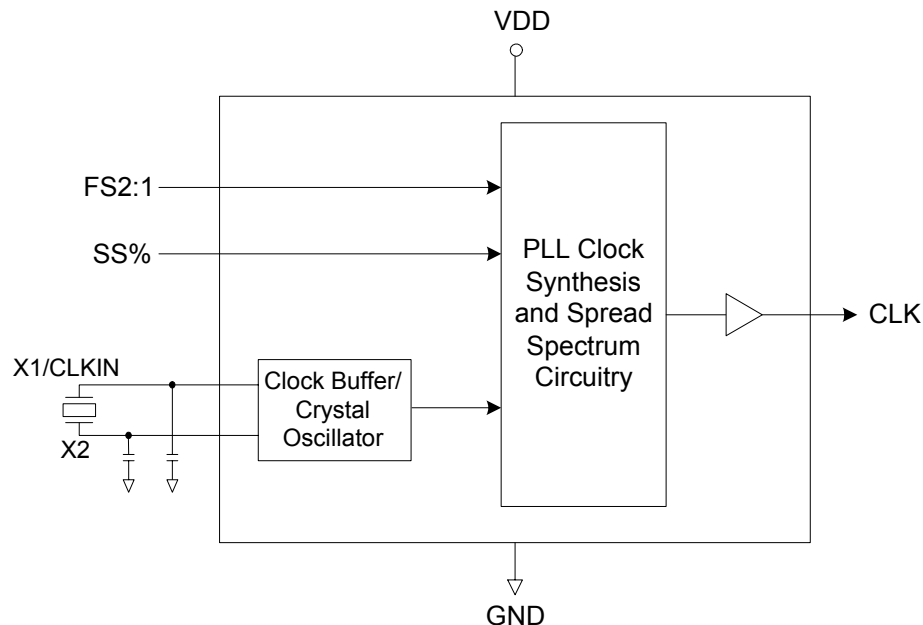
The ICS181-01 offers down spread selection of -1.25% and -3.75%. Refer to the MK1714-01/02 for the widest selection of input frequencies and multipliers.

ICS offers a complete line of EMI reducing clock generators. Consult us when you need to remove crystals and oscillators from your board.

Features

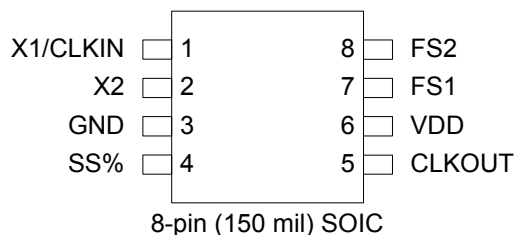
- Pin and function compatible to Cypress W181-01
- Packaged in 8-pin SOIC
- Provides a spread spectrum output clock
- Accepts a clock input and provides same frequency dithered output
- Input frequency of 28 to 75 MHz for Clock input
- Peak reduction by 7dB - 14dB typical on 3rd - 19th odd harmonics
- Spread percentage selection for -1.25% and -3.75%
- Operating voltage of 3.3 V and 5 V
- Available in Pb (lead) free package
- Industrial temperature range available
- Advanced, low-power CMOS process

Block Diagram





Pin Assignment



Spread Spectrum Select Table

SS% (Pin 4)	Spread Direction	Spread Percentage (%)
0	Down	-1.25%
1	Down	-3.75%

0 = connect to GND

1 = connect directly to VDD

Note: SS% pin has an internal pull-up resistor

Frequency Range Selection Table

FS2 (Pin 8)	FS1 (Pin 7)	Frequency Range Selection (MHz)
0	0	28-38
0	1	38-48
1	0	46-60
1	1	58-75

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/CLKIN	Input	Crystal or Clock input.
2	X2	Output	Crystal output. Float for a clock input.
3	GND	Power	Connect to ground.
4	SS%	Input	Select pin for spread amount. See table above. Internal pull-up resistor.
5	CLKOUT	Output	Spread spectrum clock output per table above.
6	VDD	Power	Connect to 3.3 V or 5 V.
7	FS1	Input	Select pin for input frequency. See table above. Internal pull-up resistor.
8	FS2	Input	Select pin for input frequency. See table above. Internal pull-up resistor.



External Components

The ICS181-01 requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of $0.01\mu\text{F}$ must be connected between VDD and GND on pins 6 and 3, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock output and the load is over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω .

value of these capacitors is given by the following equation:

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS181-01. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (commercial)	0 to +70°C
Ambient Operating Temperature (industrial)	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.135		+5.5	V



DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V \pm 5%**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Supply Current	IDD	No load, at 3.3 V		18	32	mA
Input High Voltage	V _{IH}		2.4			V
Input Low Voltage	V _{IL}				0.8	V
Output High Voltage	V _{OH}	I _{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V _{OH}	I _{OH} = -15 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 15 mA			0.4	V
Input Capacitance	C _{IN}	All pins except CLKIN		5	7	pF
		CLKIN pin only		6	10	pF
Output Impedance	R _{out}			25		ohms
Input Pull-up Resistor				500		K Ω
Power-up Time		First locked clock cycle after steady power			5	ms

Unless stated otherwise, **VDD = 5 V, \pm 10%**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		4.5	5	5.5	V
Supply Current	IDD	No load, at 3.3 V		30	50	mA
Input High Voltage	V _{IH}		0.7VDD			V
Input Low Voltage	V _{IL}				0.15VDD	V
Output High Voltage	V _{OH}	I _{OH} = -24 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 24 mA			0.4	V
Output Impedance	R _{out}			20		ohms
Input Capacitance	C _{IN}	All pins except CLKIN		5	7	pF
		CLKIN pin only		6	10	pF
Input Pull-up Resistor				500		K Ω
Power-up Time		First locked clock cycle after steady power			5	ms



AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V \pm 5% or 5 V \pm 10%**, Ambient Temperature -40 to +85°C, C_L=15 pf

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input/Output Clock Frequency			28		75	MHz
Input Crystal Frequency			28		40	MHz
Input Clock Duty Cycle		Time above VDD/2	40		60	%
Output Clock Duty Cycle		Note 1	40	50	60	%
Output Rise Time	t _{OR}	0.8 to 2.4 V, note 1		2	5	ns
Output Fall Time	t _{OF}	2.4 to 0.8 V, note 1		2	5	ns
Jitter		Cycle-to-cycle		250	300	ps

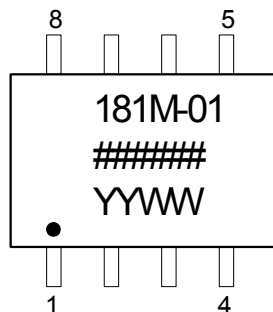
Note 1: Measured with 15 pF load

Thermal Characteristics

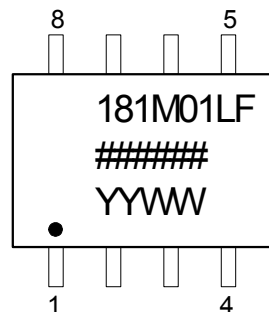
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W



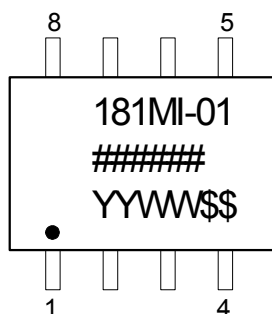
Marking Diagram (ICS181M-01)



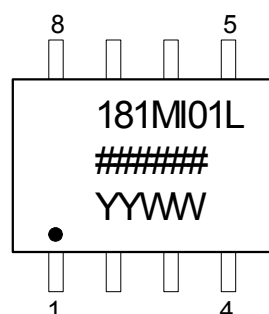
Marking Diagram (ICS181M-01LF)



Marking Diagram (ICS181MI-01)



Marking Diagram (ICS181MI-01LF)



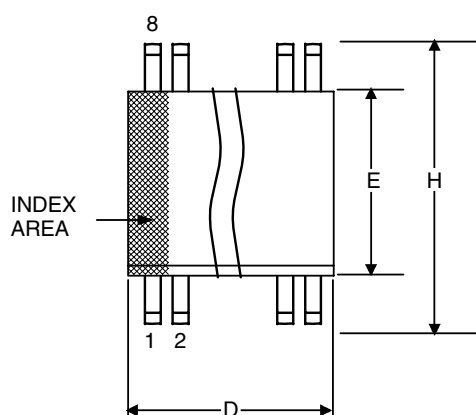
Notes:

1. ##### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. "LF" denotes Pb (lead) free package.
4. "I" denotes industrial temperature range.
5. Bottom marking: country of origin.

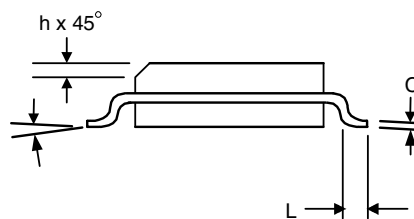
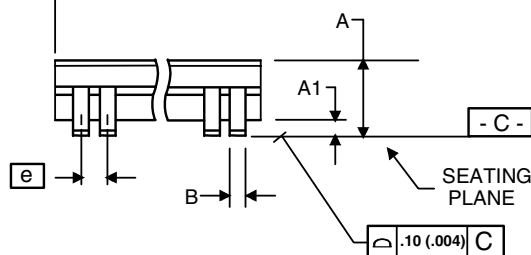


Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS181M-01	see page 6	Tubes	8-pin SOIC	0 to +70° C
ICS181M-01T		Tape and Reel	8-pin SOIC	0 to +70° C
ICS181M-01LF		Tubes	8-pin SOIC	0 to +70° C
ICS181M-01LFT		Tape and Reel	8-pin SOIC	0 to +70° C
ICS181MI-01	see page 6	Tubes	8-pin SOIC	-40 to +85° C
ICS181MI-01T		Tape and Reel	8-pin SOIC	-40 to +85° C
ICS181MI-01LF		Tubes	8-pin SOIC	-40 to +85° C
ICS181MI-01LFT		Tape and Reel	8-pin SOIC	-40 to +85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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