



Clock Slicer User Configurable PECL Output Zero Delay Buffer

Description

The ICS527-03 is the most flexible way to generate an output clock from an input clock with zero skew. The user can easily configure the device to produce nearly any output clock that is multiplied or divided from the input clock. The part supports non-integer multiplications and divisions. Using Phase-Locked Loop (PLL) techniques, the device accepts an input clock up to 200 MHz and produces an output clock up to 160 MHz.

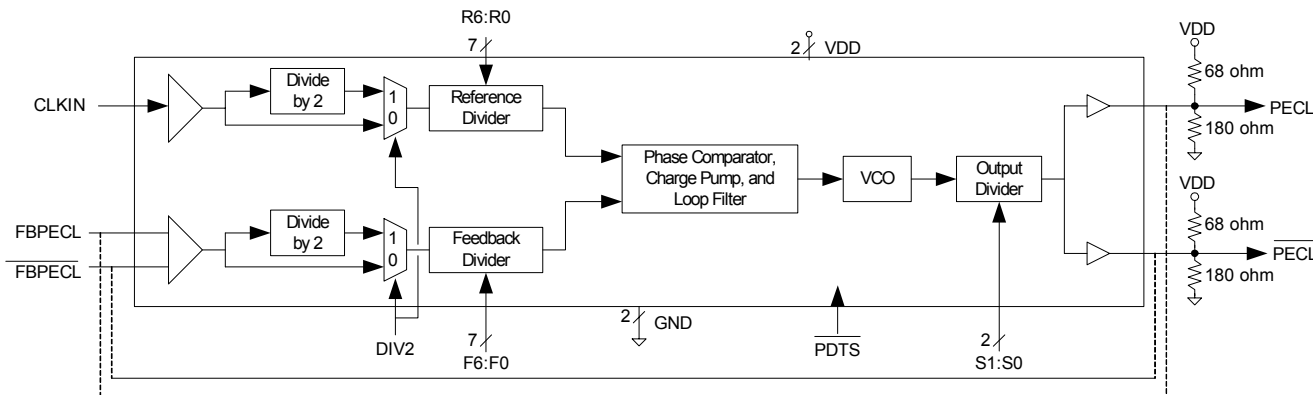
The ICS527-03 aligns rising edges on CLKIN with FBPECL at a ratio determined by the reference and feedback dividers.

For a PECL input and output clock with zero delay, use the ICS527-04.

Features

- Packaged as 28 pin SSOP (150 mil body)
- Synchronizes fractional clocks rising edges
- CMOS in to PECL out
- Pin selectable dividers
- Zero input to output skew
- User determines the output frequency - no software needed
- Slices frequency or period
- Input clock frequency of 1.5 MHz to 200 MHz
- Output clock frequencies from 2.5 MHz to 160 MHz
- Very low jitter
- Duty cycle of 45/55
- Operating voltage of 3.3 V
- Advanced, low power CMOS process

Block Diagram





Pin Assignment

| | | | | | |
|--------|--------------------------|----|----|--------------------------|------|
| R5 | <input type="checkbox"/> | 1 | 28 | <input type="checkbox"/> | R4 |
| R6 | <input type="checkbox"/> | 2 | 27 | <input type="checkbox"/> | R3 |
| DIV2 | <input type="checkbox"/> | 3 | 26 | <input type="checkbox"/> | R2 |
| S0 | <input type="checkbox"/> | 4 | 25 | <input type="checkbox"/> | R1 |
| S1 | <input type="checkbox"/> | 5 | 24 | <input type="checkbox"/> | R0 |
| VDD | <input type="checkbox"/> | 6 | 23 | <input type="checkbox"/> | VDD |
| FBPECL | <input type="checkbox"/> | 7 | 22 | <input type="checkbox"/> | PECL |
| FBPECL | <input type="checkbox"/> | 8 | 21 | <input type="checkbox"/> | PECL |
| GND | <input type="checkbox"/> | 9 | 20 | <input type="checkbox"/> | GND |
| CLKIN | <input type="checkbox"/> | 10 | 19 | <input type="checkbox"/> | RES |
| PDTS | <input type="checkbox"/> | 11 | 18 | <input type="checkbox"/> | F6 |
| F0 | <input type="checkbox"/> | 12 | 17 | <input type="checkbox"/> | F5 |
| F1 | <input type="checkbox"/> | 13 | 16 | <input type="checkbox"/> | F4 |
| F2 | <input type="checkbox"/> | 14 | 15 | <input type="checkbox"/> | F3 |

28 pin 150 mil body SSOP

Output Frequency and Output Divider Table

| S1 | S0 | Output Divider | Output Frequency (MHz) |
|----|----|----------------|------------------------|
| 0 | 0 | 2 | 10 - 80 |
| 0 | 1 | 4 | 5 - 40 |
| 1 | 0 | 8 | 2.5 - 20 |
| 1 | 1 | 1 | 20 - 160 |

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|---------------|----------|--|
| 1,2, 24-28 | R5, R6, R0-R4 | Input | Reference divider word input pins determined by user. Forms a binary number from 0 to 127. Internal pull-up. |
| 3 | DIV2 | Input | Selects CLK2 function to output a SYNC signal or a divide by 2 of CLK1 based on the table above. Internal pull-up. |
| 4, 5 | S0, S1 | Input | Select pins for output divider determined by user. See table above. Internal pull-up. |
| 6, 23 | VDD | Power | Connect to +3.3 V. |
| 7 | FPECL | Input | PECL feedback input. |
| 8 | FPECL | Input | Complementary PECL feedback input. |
| 9, 20 | GND | Power | Connect to ground |
| 10 | CLKIN | Input | Clock input. |
| 11 | PDTS | Input | Power Down. Active low. Turns off entire chip when low, both clock outputs are tri-stated. Internal pull-up. |
| 12-18 | F0-F6 | Input | Feedback divider word input pins determined by user. Forms a binary number from 0 to 127. Internal pull-up |
| 19 | RES | BIAS | Resistor connection to VDD for setting level of PECL outputs. |
| 21 | PECL | Output | Complementary PECL input clock. |
| 22 | PECL | Output | PECL input clock. |



External Components

Decoupling Capacitors

As with any high performance mixed-signal IC, the ICS527-03 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01μF must be connected between each VDD and the PCB ground plane. They must be connected close to the device to minimize lead inductance.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Determining (setting) the ICS527-03 Dividers

The user has full control in setting the desired output clock over the range shown in the table on page 2. The user should connect the divider select input pins directly to ground (or VDD, although this is not required because of internal pull-ups) during Printed Circuit Board layout, so the ICS527-03 automatically produces the correct clock when all components are soldered. It is also possible to connect the inputs to parallel I/O ports in order to switch frequencies.

The output of the ICS527-03 can be determined by the following simple equation:

$$\text{FB Frequency} = \text{Input Frequency} \times \frac{\text{FDW} + 2}{\text{RDW} + 2}$$

Where:

Reference Divider Word (RDW) = 0 to 127

Feedback Divider Word (FDW) = 0 to 127

FB Frequency is the same as either CLK1 or CLK2 depending on feedback connection

Also, the following operating ranges should be observed:

$$300\text{kHz} < \frac{\text{Input Frequency}}{\text{RDW} + 2} < 20\text{ MHz}$$

The output divide should be selected depending on the frequency of CLK1. The table on page 2 gives the ranges.

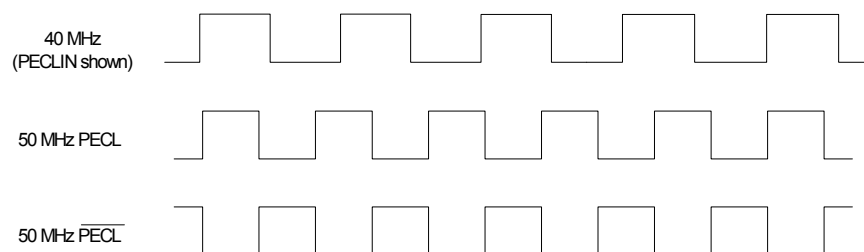
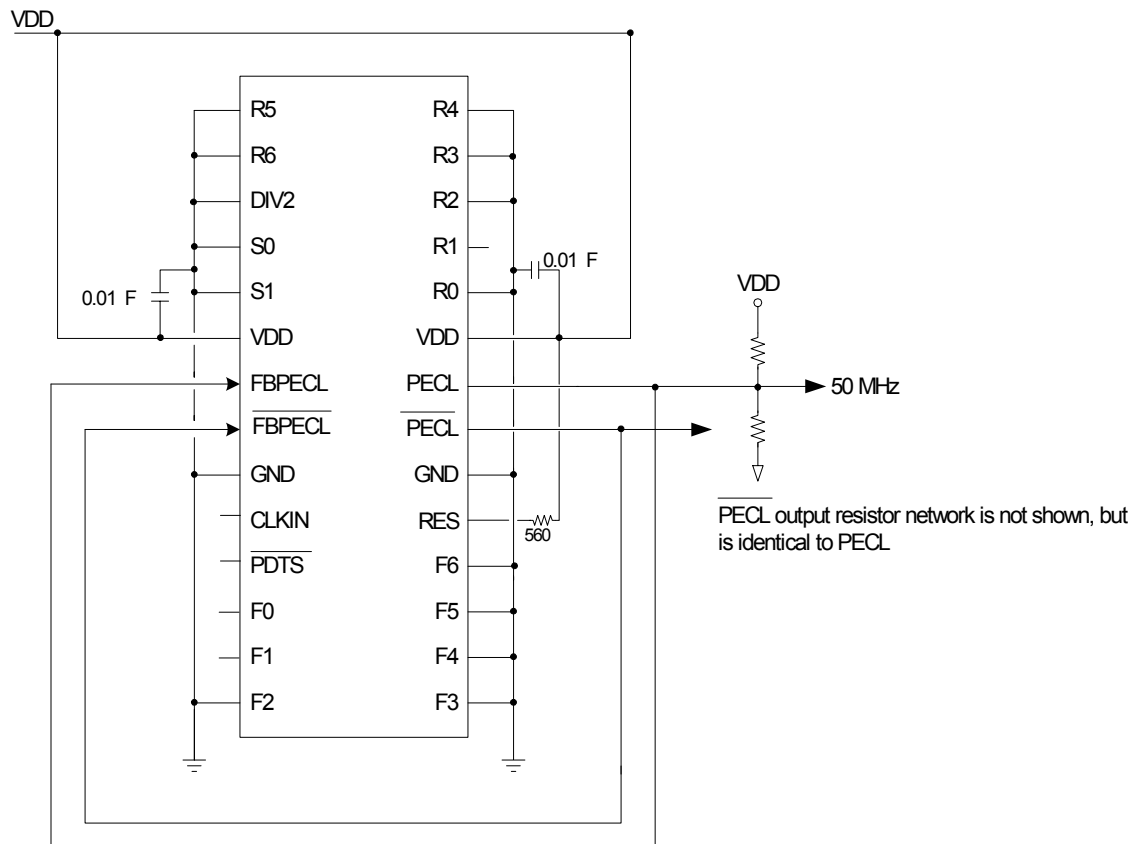
The dividers are expressed as integers. For example, if a 50 MHz output on CLK1 is desired from a 40 MHz input, the reference divider word (RDW) should be 2 and the feedback divider word (FDW) should be 3 which gives the required 5/4 multiplication. If multiple choices of dividers are available, then the lowest numbers should be used. In this example, the output divide (OD) should be selected to be 2. Then R6:R0 is 0000010, F6:F0 is 0000011 and S1:S0 is 00. Also, this example assumes CLK1 is connected to FBIN.

If you need assistance determining the optimum divider settings, please send an e-mail to ics-mk@icst.com with the desired input clock and the desired output frequency.



Typical Example

The following connection diagram shows the implementation of the example from the previous section. This will generate a 50 MHz clock synchronously with a 40 MHz input. The layout diagram below will produce the waveforms shown on the right.



Note: The series termination resistor is located before the feedback



Multiple Output Example

In this example, an output clock of 125 MHz is used. Four copies of 50 MHz are required, de-skewed and aligned to the 125 MHz input clock. The following solution uses the ICS554-01A which has buffers with low pin to pin skew. The layout diagram below will produce the waveforms shown on the bottom.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) Each 0.01 μ F decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No via's should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) PECL termination networks should be located as close to the outputs as possible.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS527-03. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS527-03. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|-------------------------------|-------------------|
| Supply Voltage, VDD | 7V |
| All Inputs and Outputs | -0.5V to VDD+0.5V |
| Ambient Operating Temperature | 0 to +70°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 175°C |
| Soldering Temperature | 260°C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|-------|------|-------|-------|
| Ambient Operating Temperature, ICS527R-02 | 0 | | +70 | °C |
| Ambient Operating Temperature, ICS527R-02I | 0 | | +70 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.15 | +3.3 | +3.45 | V |

DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3V \pm 5%, Ambient Temperature 0 to +70°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-------------------------------------|-----------------|--------------------------------|---------|------|---------|---------|
| Operating Voltage | VDD | | 3.15 | 3.3 | 3.45 | V |
| Supply Current | IDD | 15 MHz in, 60MHz out, no load | | 15 | | mA |
| Supply Current, Power Down | IDDPD | $\overline{PDT\overline{S}}=0$ | | 20 | | μ A |
| Input High Voltage | V _{IH} | | 2 | | | V |
| Input Low Voltage | V _{IL} | | | | 0.8 | V |
| Input High Voltage, PECLIN and FBIN | V _{IH} | | VDD/2+1 | | | V |
| Input Low Voltage, PECLIN and FBIN | V _{IL} | | | | VDD/2-1 | V |
| Output High Voltage | V _{OH} | I _{OH} = -12 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 12 mA | | | 0.4 | V |



| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|----------|------------|------|----------|------|------------|
| Input Capacitance, except PECLIN and FBIN | C_{IN} | | | 5 | | pF |
| Short Circuit Current | I_{OS} | | | ± 70 | | mA |
| On-chip pull-up resistor | R_{PU} | | | 270 | | k Ω |

AC Electrical Characteristics

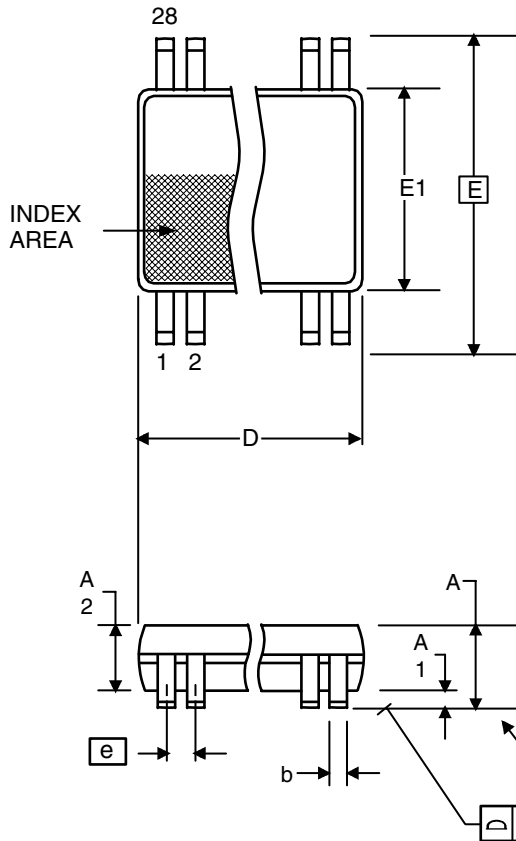
Unless stated otherwise, VDD = 3.3V \pm 5%, Ambient Temperature 0 to +70°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-----------|---------------------------------|------|----------|------|-------|
| Input Frequency | F_{IN} | | 1.5 | | 200 | MHz |
| Output Frequency, CLK1 | F_{OUT} | 0 to +70°C | 2.5 | | 160 | MHz |
| | | -40 to +85°C | 4 | | 140 | MHz |
| Output Rise Time | t_{OR} | 0.8 to 2.0V, $C_L=15$ pF | | 1 | | ns |
| Output Fall Time | t_{OF} | 2.0 to 0.8V, $C_L=15$ pF | | 1 | | ns |
| Output Duty Cycle (% high time) | t_{OD} | Measured at VDD/2, $C_L=15$ pF | 45 | 50 | 55 | % |
| Power Down Time, $\overline{PDT\overline{S}}$ low to clocks tri-stated | | | | | 50 | ns |
| Power Up ime, $\overline{PDT\overline{S}}$ high to clocks stable | | | | | 10 | ms |
| Absolute Clock Period Jitter | t_{ja} | Deviation from mean | | ± 90 | | ps |
| One sigma Clock Period Jitter | t_{js} | | | 40 | | ps |
| Input to output skew | t_{IO} | PECLIN to CLK1, Note 1 | -250 | | 250 | ps |
| Device to device skew | t_{pi} | Common PECLIN, measured at FBIN | | 0 | 500 | ps |

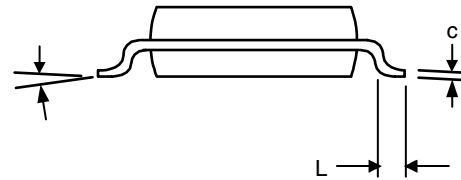
Note 1: Assumes clocks with same rise time, measured from rising edges at VDD/2.

**Package Outline and Package Dimensions (28 pin SSOP, 150 mil Body, 0.025 mm Pitch)**

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



| | Millimeters | | Inches | |
|----------|-------------|-------|-------------|-------|
| Symbol | Min | Max | Min | Max |
| A | 1.35 | 1.75 | .053 | .069 |
| A1 | 0.10 | 0.25 | .0040 | .010 |
| A2 | -- | 1.50 | -- | .059 |
| b | 0.20 | 0.30 | .008 | .012 |
| C | 0.18 | 0.25 | .007 | .010 |
| D | 9.80 | 10.00 | .386 | .394 |
| E | 5.80 | 6.20 | .228 | .244 |
| E1 | 3.80 | 4.00 | .150 | .157 |
| e | 0.635 Basic | | 0.025 Basic | |
| L | 0.40 | 1.27 | .016 | .050 |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | 0.004 |

**Ordering Information**

| Part / Order Number | Marking | Shipping packaging | Package | Temperature |
|---------------------|------------|--------------------|-------------|-------------|
| ICS527R-03 | ICS527R-03 | Tubes | 28 pin SSOP | 0 to +70°C |
| ICS527R-03T | ICS527R-03 | Tape and Reel | 28 pin SSOP | 0 to +70°C |

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