



### GENERAL DESCRIPTION



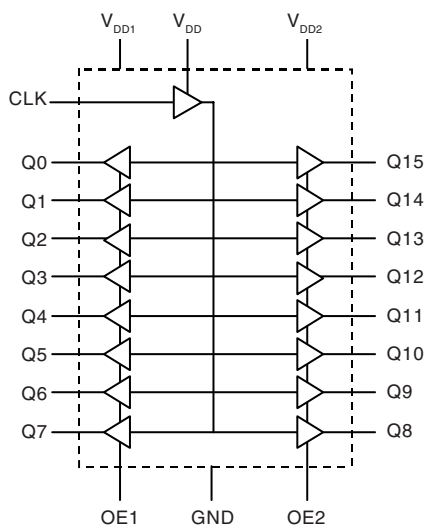
The ICS8343-01 is a low skew, 1-to-16 LVCMOS/ LVTTTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8343-01 single ended clock input accepts LVCMOS or LVTTTL input levels.

The ICS8343-01 operates at 3.3V, 2.5V and mixed 3.3V input and 2.5V supply modes over the commercial temperature range. Guaranteed output and part-to-part skew characteristics make the ICS8343-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

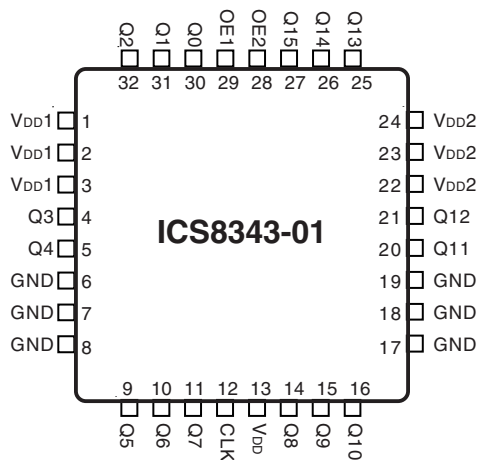
### FEATURES

- 16 LVCMOS/LVTTTL outputs
- 1 LVCMOS/LVTTTL clock input
- CLK can accept the following input levels: LVCMOS, LVTTTL
- Maximum output frequency: 200MHz
- Dual output enable inputs facilitates 1-to-16 or 1-to-8 input to output modes
- All inputs are 5V tolerant
- Output skew: 250ps (maximum)
- Part-to-part skew: 700ps (maximum)
- Full 3.3V and 2.5V or mixed 3.3V core/2.5V operating supply
- 0°C to 70°C ambient operating temperature
- Lead-Free package available
- Industrial temperature information available upon request

### BLOCK DIAGRAM



### PIN ASSIGNMENT



**32-Lead LQFP**  
7mm x 7mm x 1.4mm body package  
**Y Package**  
(Top View)



**TABLE 1. PIN DESCRIPTIONS**

| Number                 | Name          | Type   |          | Description   |
|------------------------|---------------|--------|----------|---|
| 1, 2, 3                | $V_{DD1}$     | Power  |          | Q0 thru Q7 output supply pins.  |
| 4, 5                   | Q3, Q4        | Output |          | LVCMOS/LVTTTL clock outputs. 7 $\Omega$ typical output impedance.   |
| 6, 7, 8,<br>17, 18, 19 | GND           | Power  |          | Power supply ground.  |
| 9, 10, 11              | Q5, Q6, Q7    | Output |          | LVCMOS/LVTTTL clock outputs. 7 $\Omega$ typical output impedance.   |
| 12                     | CLK           | Input  | Pulldown | LVCMOS/LVTTTL clock input / 5V tolerant.  |
| 13                     | $V_{DD}$      | Power  |          | Core supply pin.  |
| 14, 15, 16             | Q8, Q9, Q10   | Output |          | LVCMOS/LVTTTL clock outputs. 7 $\Omega$ typical output impedance.   |
| 20, 21                 | Q11, Q12      | Output |          | LVCMOS/LVTTTL clock outputs. 7 $\Omega$ typical output impedance.   |
| 22, 23, 24             | $V_{DD2}$     | Power  |          | Q8 thru Q15 output supply pins.   |
| 25, 26, 27             | Q13, Q14, Q15 | Output |          | LVCMOS/LVTTTL clock outputs. 7 $\Omega$ typical output impedance.   |
| 28                     | OE2           | Input  | Pullup   | Output enable. When low forces outputs Q8 thru Q15 to HiZ state. 5V tolerant. LVCMOS/LVTTTL interface levels. |
| 29                     | OE1           | Input  | Pullup   | Output enable. When low forces outputs Q0 thru Q7 to HiZ state. 5V tolerant. LVCMOS/LVTTTL interface levels.  |
| 30, 31, 32             | Q0, Q1, Q2    | Output |          | LVCMOS/LVTTTL clock outputs. 7 $\Omega$ typical output impedance.   |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol         | Parameter                                  | Test Conditions                     | Minimum | Typical | Maximum | Units      |
|----------------|--|-------------------------------------|---------|---------|---------|------------|
| $C_{IN}$       | Input Capacitance                          |                                     |         | 4       |         | pF         |
| $C_{PD}$       | Power Dissipation Capacitance (per output) | $V_{DD}, V_{DD1}, V_{DD2} = 3.465V$ |         | 11      |         | pF         |
|                |  | $V_{DD1}, V_{DD2} = 2.63V$          |         | 9       |         | pF         |
| $R_{PULLUP}$   | Input Pullup Resistor                      |                                     |         | 51      |         | K $\Omega$ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor                    |                                     |         | 51      |         | K $\Omega$ |
| $R_{OUT}$      | Output Impedance                           | $V_{DD}, V_{DD1}, V_{DD2} = 3.3V$   | 5       | 7       | 12      | $\Omega$   |

**TABLE 3. FUNCTION TABLE**

| Inputs |     | Outputs |        |
|--------|-----|---------|--------|
| OE1    | OE2 | Q0:Q7   | Q8:Q15 |
| 0      | 0   | HiZ     | HiZ    |
| 1      | 0   | Active  | HiZ    |
| 0      | 1   | HiZ     | Active |
| 1      | 1   | Active  | Active |

NOTE: OE1 and OE2 are 5V tolerant.



#### ABSOLUTE MAXIMUM RATINGS

|  |                           |
|--|---------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                      |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5V$  |
| Outputs, $V_O$                           | -0.5V to $V_{DDx} + 0.5V$ |
| Package Thermal Impedance, $\theta_{JA}$ | 47.9°C/W (0 lfpm)         |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C            |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DD1} = V_{DD2} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = 0^\circ$  TO  $70^\circ C$**

| Symbol    | Parameter                     | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage           |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDx}$ | Output Supply Voltage; NOTE 1 |                 | 3.135   | 3.3     | 3.465   | V     |
|           |                               |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$  | Power Supply Current          |                 |         |         | 35      | mA    |
| $I_{DDx}$ | Output Supply Current; NOTE 2 |                 |         |         | 14      | mA    |

NOTE 1:  $V_{DDx}$  denotes  $V_{DD1}$  and  $V_{DD2}$ .

NOTE 2:  $I_{DDx}$  denotes the sum of  $I_{DD1}$  and  $I_{DD2}$ .

**TABLE 4B. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DD1} = V_{DD2} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ$  TO  $70^\circ C$**

| Symbol    | Parameter                     | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage           |                 | 2.375   | 2.5     | 2.625   | V     |
| $V_{DDx}$ | Output Supply Voltage; NOTE 1 |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$  | Power Supply Current          |                 |         |         | 34      | mA    |
| $I_{DDx}$ | Output Supply Current; NOTE 2 |                 |         |         | 13      | mA    |

NOTE 1:  $V_{DDx}$  denotes  $V_{DD1}$  and  $V_{DD2}$ .

NOTE 2:  $I_{DDx}$  denotes the sum of  $I_{DD1}$  and  $I_{DD2}$ .



**TABLE 4C. LVC MOS / LV TTL DC CHARACTERISTICS,  $V_{DD} = V_{DD1} = V_{DD2} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ;  
 $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DD1} = V_{DD2} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ$  TO  $70^\circ C$**

| Symbol    | Parameter                    | Test Conditions                          | Minimum  | Typical | Maximum        | Units   |
|-----------|------------------------------|--|--|---------|----------------|---------|
| $V_{IH}$  | Input High Voltage           | OE1, OE2                                 | 2  |         | $V_{DD} + 0.3$ | V       |
|           |                              | CLK                                      | 2  |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$  | Input Low Voltage            | OE1, OE2                                 | -0.3   |         | 0.8            | V       |
|           |                              | CLK                                      | -0.3   |         | 1.3            | V       |
| $I_{IH}$  | Input High Current           | OE1, OE2                                 | $V_{DD} = V_{IN} = 3.465V$ or $2.625V$           |         | 5              | $\mu A$ |
|           |                              | CLK                                      | $V_{DD} = V_{IN} = 3.465V$ or $2.625V$           |         | 150            | $\mu A$ |
| $I_{IL}$  | Input Low Current            | OE1, OE2                                 | $V_{DD} = 3.465V$ or $2.625V$ ,<br>$V_{IN} = 0V$ | -150    |                | $\mu A$ |
|           |                              | CLK                                      | $V_{DD} = 3.465V$ or $2.625V$ ,<br>$V_{IN} = 0V$ | -5      |                | $\mu A$ |
| $V_{OH}$  | Output High Voltage; NOTE 1  | $V_{DD1} = V_{DD2} = 3.465V$             | 2.6  |         |                | V       |
|           |                              | $V_{DD1} = V_{DD2} = 2.625V$             | 1.8  |         |                | V       |
| $V_{OL}$  | Output Low Voltage; NOTE 1   | $V_{DD1} = V_{DD2} = 3.465V$ or $2.625V$ |  |         | 0.5            | V       |
| $I_{OZL}$ | Output Tristate Current Low  |  |  |         | 5              | $\mu A$ |
| $I_{OZH}$ | Output Tristate Current High |  |  |         | 5              | $\mu A$ |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDX}/2$ . See Parameter Measurement Information, "Output Load Test Circuit Diagrams".

**TABLE 5A. AC CHARACTERISTICS,  $V_{DD} = V_{DD1} = V_{DD2} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ$  TO  $70^\circ C$**

| Symbol       | Parameter                       | Test Conditions                       | Minimum               | Typical        | Maximum               | Units |
|--------------|---------------------------------|---------------------------------------|-----------------------|----------------|-----------------------|-------|
| $f_{MAX}$    | Output Frequency                |                                       |                       |                | 200                   | MHz   |
| $t_{PLH}$    | Propagation Delay;<br>NOTE 1    | $f \leq 200MHz$                       | 2.0                   |                | 4.0                   | ns    |
| $t_{sk(o)}$  | Output Skew; NOTE 2, 4          | Measured on rising edge @ $V_{DDX}/2$ |                       |                | 250                   | ps    |
| $t_{sk(pp)}$ | Part-to-Part Skew;<br>NOTE 3, 4 | Measured on rising edge @ $V_{DDX}/2$ |                       |                | 700                   | ps    |
| $t_R / t_F$  | Output Rise/Fall Time           | 20% to 80%                            | 0.4                   |                | 1.5                   | ns    |
| odc          | Output Duty Cycle               | $f \leq 133MHz$                       | 45                    |                | 55                    | %     |
| $t_{PW}$     | Output Pulse Width              | $f > 133MHz$                          | $t_{PERIOD}/2 - 0.25$ | $t_{PERIOD}/2$ | $t_{PERIOD}/2 + 0.25$ | ns    |

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDX}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDX}/2$ .

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDX}/2$ .

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



**TABLE 5B. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DD1} = V_{DD2} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ$  TO  $70^\circ C$**

| Symbol      | Parameter                    | Test Conditions                       | Minimum | Typical | Maximum | Units |
|-------------|------------------------------|---------------------------------------|---------|---------|---------|-------|
| $f_{MAX}$   | Output Frequency             |                                       |         |         | 200     | MHz   |
| $t_{PLH}$   | Propagation Delay; NOTE 1    | $f \leq 200MHz$                       | 2.0     |         | 4.5     | ns    |
| $tsk(o)$    | Output Skew; NOTE 2, 4       | Measured on rising edge @ $V_{DDX}/2$ |         |         | 250     | ps    |
| $tsk(pp)$   | Part-to-Part Skew; NOTE 3, 4 | Measured on rising edge @ $V_{DDX}/2$ |         |         | 700     | ps    |
| $t_R / t_F$ | Output Rise/Fall Time        | 20% to 80%                            | 0.4     |         | 1.0     | ns    |
| odc         | Output Duty Cycle            | $f \leq 133MHz$                       | 40      |         | 60      | %     |

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDX}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDX}/2$ .

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDX}/2$ .

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 5C. AC CHARACTERISTICS,  $V_{DD} = V_{DD2} = 3.3V \pm 5\%$ ,  $V_{DD1} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ$  TO  $70^\circ C$**

| Symbol    | Parameter           | Test Conditions                       | Minimum | Typical | Maximum | Units |
|-----------|---------------------|---------------------------------------|---------|---------|---------|-------|
| $f_{MAX}$ | Output Frequency    |                                       |         |         | 200     | MHz   |
| $tsk(o)$  | Output Skew; NOTE 1 | Measured on rising edge @ $V_{DDX}/2$ |         |         | 250     | ps    |

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Defined as skew across outputs at the same supply voltages within a bank, and with equal load conditions.

**TABLE 5D. AC CHARACTERISTICS,  $V_{DD} = V_{DD1} = V_{DD2} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ$  TO  $70^\circ C$**

| Symbol      | Parameter                    | Test Conditions                       | Minimum | Typical | Maximum | Units |
|-------------|------------------------------|---------------------------------------|---------|---------|---------|-------|
| $f_{MAX}$   | Output Frequency             |                                       |         |         | 133     | MHz   |
| $t_{PLH}$   | Propagation Delay; NOTE 1    | $f \leq 200MHz$                       | 2.0     |         | 4.0     | ns    |
| $tsk(o)$    | Output Skew; NOTE 2, 4       | Measured on rising edge @ $V_{DDX}/2$ |         |         | 250     | ps    |
| $tsk(pp)$   | Part-to-Part Skew; NOTE 3, 4 | Measured on rising edge @ $V_{DDX}/2$ |         |         | 1       | ns    |
| $t_R / t_F$ | Output Rise/Fall Time        | 20% to 80%                            | 0.4     |         | 1.0     | ns    |
| odc         | Output Duty Cycle            | $f \leq 133MHz$                       | 40      |         | 60      | %     |

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDX}/2$  of the output.

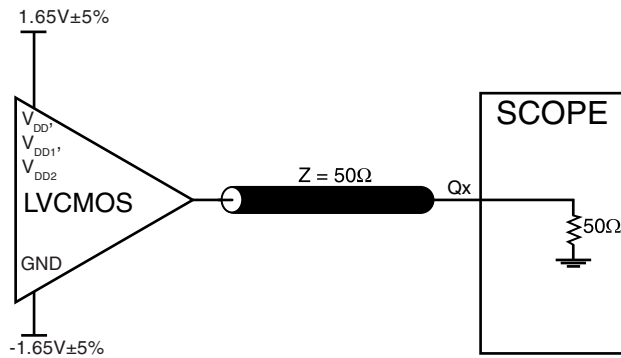
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDX}/2$ .

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDX}/2$ .

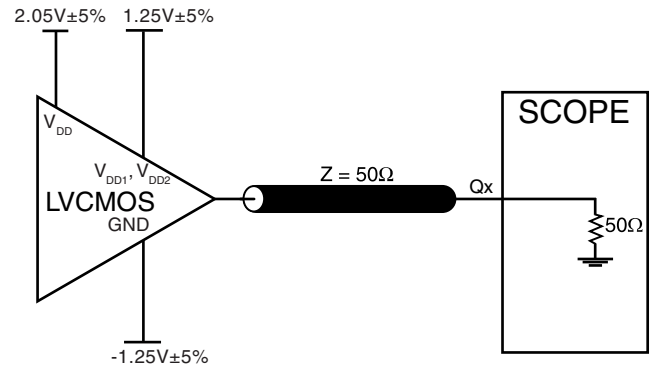
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



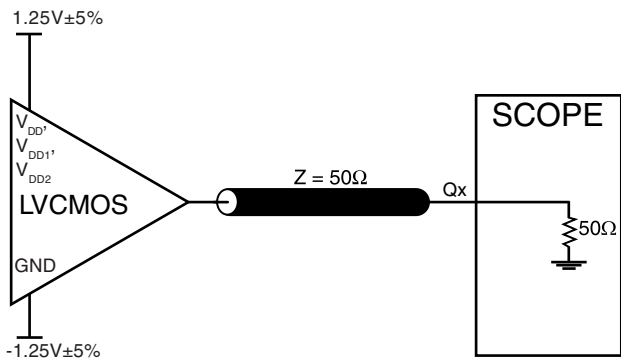
## PARAMETER MEASUREMENT INFORMATION



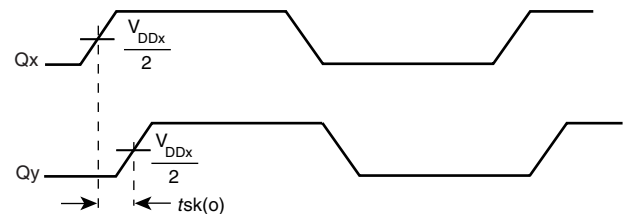
**3.3V CORE/ 3.3V OUTPUT LOAD AC TEST CIRCUIT**



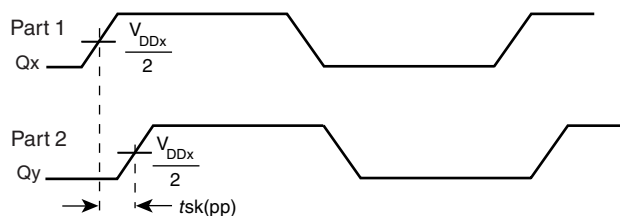
**3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT**



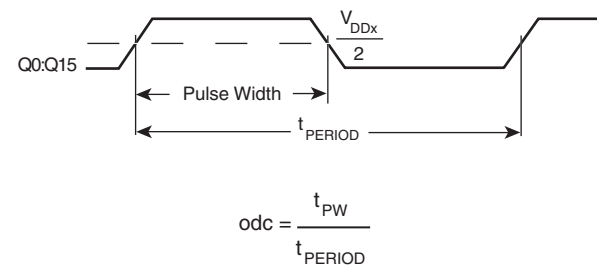
**2.5V CORE/ 2.5V OUTPUT LOAD AC TEST CIRCUIT**



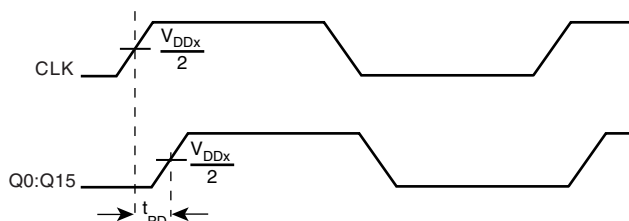
**OUTPUT SKEW**



**PART-TO-PART SKEW**

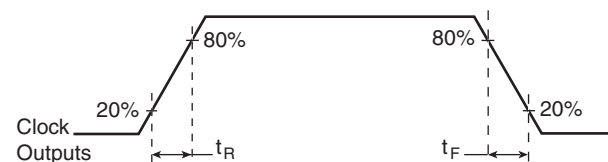


**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



**PROPAGATION DELAY**

**OUTPUT RISE/FALL TIME**





## RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 32 LEAD LQFP

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |          |          |          |
|--|----------|----------|----------|
|  | 0        | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards       | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 47.9°C/W | 42.1°C/W | 39.4°C/W |

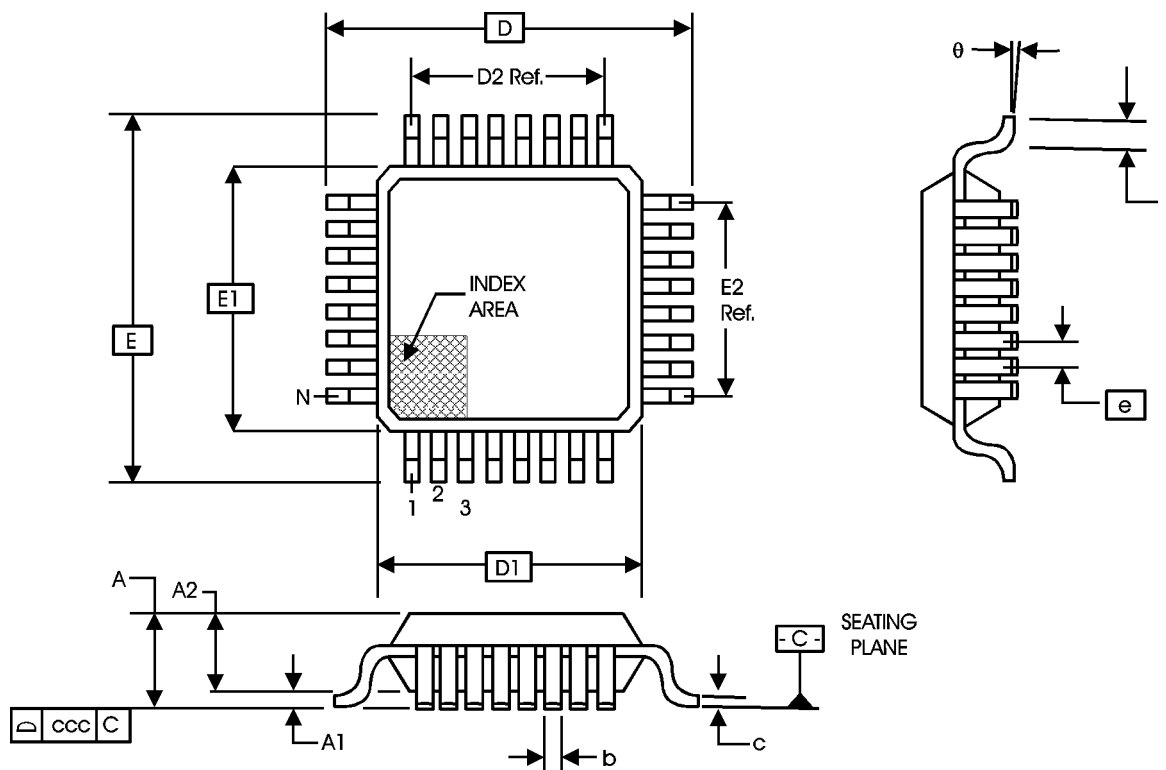
**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS8343-01 is: 985



**PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP**



**TABLE 7. PACKAGE DIMENSIONS**

| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS |            |         |         |
|--|------------|---------|---------|
| SYMBOL   | BBA        |         |         |
|  | MINIMUM    | NOMINAL | MAXIMUM |
| N  | 32         |         |         |
| A  | --         | --      | 1.60    |
| A1   | 0.05       | --      | 0.15    |
| A2   | 1.35       | 1.40    | 1.45    |
| b  | 0.30       | 0.37    | 0.45    |
| c  | 0.09       | --      | 0.20    |
| D  | 9.00 BASIC |         |         |
| D1   | 7.00 BASIC |         |         |
| D2   | 5.60 Ref.  |         |         |
| E  | 9.00 BASIC |         |         |
| E1   | 7.00 BASIC |         |         |
| E2   | 5.60 Ref.  |         |         |
| e  | 0.80 BASIC |         |         |
| L  | 0.45       | 0.60    | 0.75    |
| θ  | 0°         | --      | 7°      |
| ccc  | --         | --      | 0.10    |

Reference Document: JEDEC Publication 95, MS-026





Integrated  
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Systems, Inc.

# ICS8343-01

## LOW SKEW, 1-TO-16

### LVC MOS / LVTTTL FANOUT BUFFER

**TABLE 8. ORDERING INFORMATION**

| Part/Order Number | Marking      | Package                                   | Count        | Temperature |
|-------------------|--------------|---|--------------|-------------|
| ICS8343AY-01      | ICS8343AY-01 | 32 Lead LQFP                              | 250 per tray | 0°C to 70°C |
| ICS8343AY-01T     | ICS8343AY-01 | 32 Lead LQFP on Tape and Reel             | 1000         | 0°C to 70°C |
| ICS8343AY-01LF    | ICS8343AY01L | 32 Lead "Lead-Free" LQFP                  | 250 per tray | 0°C to 70°C |
| ICS8343AY-01LFT   | ICS8343AY01L | 32 Lead "Lead-Free" LQFP on Tape and Reel | 1000         | 0°C to 70°C |

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Integrated  
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**ICS8343-01**  
**LOW SKEW, 1-TO-16**  
**LVC MOS / LV TTL FANOUT BUFFER**

| REVISION HISTORY SHEET |       |      |   |         |
|------------------------|-------|------|---|---------|
| Rev                    | Table | Page | Description of Change   | Date    |
| A                      | T2    | 2    | Pin Characteristics Table - changed $C_{IN}$ 4pF max to 4pF typical.<br>Added to $R_{OUT}$ , 5 $\Omega$ min. and 12 $\Omega$ max. | 9/18/03 |
|                        | T8    | 11   | Ordering Information correct package column from 48 Lead to 32 Lead.  |         |
| B                      | T5C   | 5    | Added Mixed AC Characteristics Table.<br>Updated format.  | 8/13/04 |
| B                      | T8    | 9    | Added Lead-Free marking to Ordering Information Table.  | 9/16/04 |