



GENERAL DESCRIPTION



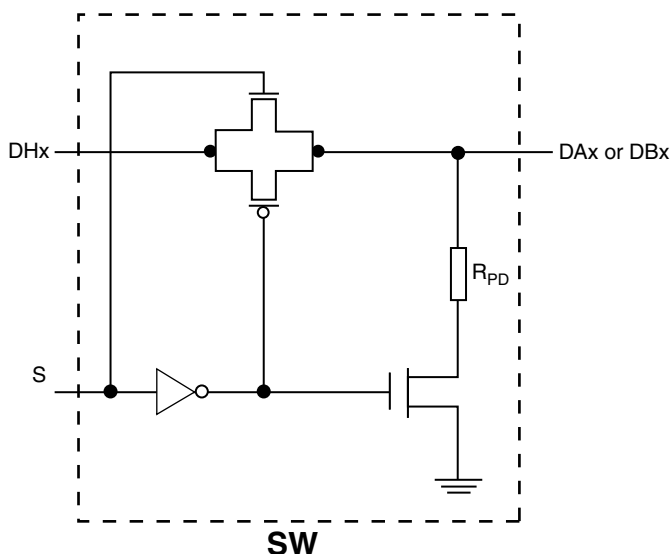
The ICS83841 is a 20 Bit, DDR SDRAM 2:1 MUX and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The device has 20 host lines and each host line can be passed to 2 data ports. The host/data ports are compatible with single-ended SSTL-2 and the device operates from a 2.5V supply.

Guaranteed low output skew makes the ICS83841 ideal for demanding applications which require well defined performance and repeatability.

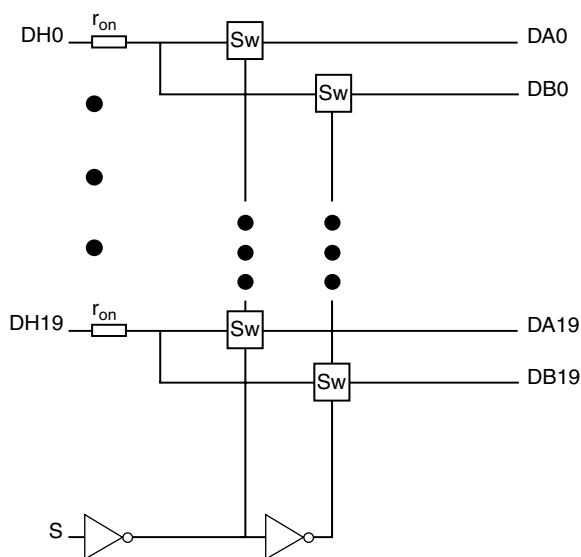
FEATURES

- Forty low skew single-ended DIMM ports
- One SSTL-2 compatible select input
- Maximum Switching Speed: 3ns
- Output skew: 180ps (maximum)
- $r_{on} = 20\Omega$ (typical)
- Full 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

SIMPLIFIED SCHEMATIC



LOGIC DIAGRAM



PIN ASSIGNMENT

	1	2	3	4	5	6	7	8	9	10
A	DB ₁₇	DA ₁₇	DB ₁₆	DB ₁₅	DA ₁₅	DB ₁₄	DA ₁₄	DA ₁₃	DB ₁₂	DA ₁₂
B	DA ₁₈	DH ₁₇	DH ₁₆	DA ₁₆	DH ₁₅	DH ₁₄	DB ₁₃	DH ₁₃	DH ₁₂	DB ₁₁
C	DB ₁₈	DH ₁₈			GND	GND			DH ₁₁	DA ₁₁
D	DA ₁₉	GND							GND	DB ₁₀
E	DB ₁₉	DH ₁₉	S					V _{DD}	DH ₁₀	DA ₁₀
F	DA ₀	DH ₀	V _{DD}					V _{DD}	DH ₉	DB ₉
G	DB ₀	GND							GND	DA ₉
H	DA ₁	DH ₁			GND	GND			DH ₈	DB ₈
J	DB ₁	DH ₂	DH ₃	DB ₃	DH ₄	DH ₅	DA ₆	DH ₆	DH ₇	DA ₈
K	DA ₂	DB ₂	DA ₃	DA ₄	DB ₄	DA ₅	DB ₅	DB ₆	DA ₇	DB ₇

ICS83841
72-Ball TFBGA
6mm x 6mm x 1.2mm
package body
H Package
Top View



TABLE 1. PIN DESCRIPTIONS

Number	Name	Type	Description
E8, F3, F8	V_{DD}	Power	Positive supply pins.
C5, C6, D2, D9, G2, G9, H5, H6	GND	Power	Power supply ground.
E3	S	Input	Control Input. Selects Host Port function per Table 3.
B2, B3, B5, B6, B8, B9, C2 C9, E2, E9, F2, F9, H2, H9, J2, J3, J5, J6, J8, J9	DH17, DH16, DH15, DH14, DH13, DH12, DH18, DH11, DH19, DH10, DH0, DH9, DH1, DH8, DH2, DH3, DH4, DH5, DH6, DH7	Port	Host ports.
A2, A5, A7, A8, A10, B1, B4, C10, D1, E10, F1, G10, H1, J7, J10, K1, K3, K4, K6, K9	DA17, DA15, DA14, DA13, DA12, DA18, DA16, DA11, DA19, DA10, DA0, DA9, DA1, DA6, DA8, DA2, DA3, DA4, DA5, DA7	Port	DIMM ports.
A1, A3, A4, A6, A9, B7, B10, C1, D10, E1, F10, G1, H10, J1, J4, K2, K5, K7, K8, K10	DB17, DB16, DB15, DB14, DB12, DB13, DB11, DB18, DB10, DB19, DB9, DB0, DB8, DB1, DB3, DB2, DB4, DB5, DB6, DB7	Port	DIMM ports.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Control Pin Capacitance	$V_I = 0V$ or V_{DD}			5	pF
C_{ON}	Channel on Capacitance	$V_{IN} = 1.5V$			10	pF

TABLE 3. FUNCTION TABLE

Control Input	Function
S	
L	Host Port = B DIMM Ports A DIMM Port = 140Ω to GND
H	Host Port = A DIMM Ports B DIMM Port = 140Ω to GND



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	-0.5V to +3.3V
Inputs, V_I	-0.3V to $V_{DD} + 0.3V$
Ports	
DC Input Clamp Current, I_{IK}	-50mA
Package Thermal Impedance, θ_{JA}	50.04°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.3	2.5	2.7	V
I_{DD}	Power Supply Current			20		μA

TABLE 4B. DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	S	1.6			V
V_{IL}	Input Low Voltage	S			0.9	V
V_{IK}	Input Clamp Voltage	$V_{DD} = 2.3V$; $I_I = -18mA$			-1.2	V
I_L	Input Leakage Current	S			± 100	μA
		Host Port			± 100	μA
		DIMM Port			± 100	μA
r_{ON}	On Resistance; NOTE 1	$V_{DD} = 2.5V$; $V_A = 0.8V$; $V_B = 1.0V$	16	20	30	Ω
		$V_{DD} = 2.5V$; $V_A = 1.7V$; $V_B = 1.5V$	16	20	30	Ω

NOTE 1: Measured by the current between the Host and the DIMM terminals at the indicated voltages on each side of the switch.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = 2.5V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
t_{PD}	Propagation Delay; NOTE 1, 3	From DHx or DAx/DBx to DAx/DBx or DHx		125	240	ps
t_{EN}	Output Enable Time	From S to DHx or DAx/DBx	1.2			ns
t_{DIS}	Output Disable Time	From S to DHx or DAx/DBx	1.2			ns
t_{OSK}	Output Skew; NOTE 2, 3	Any Port to any Port			180	ps

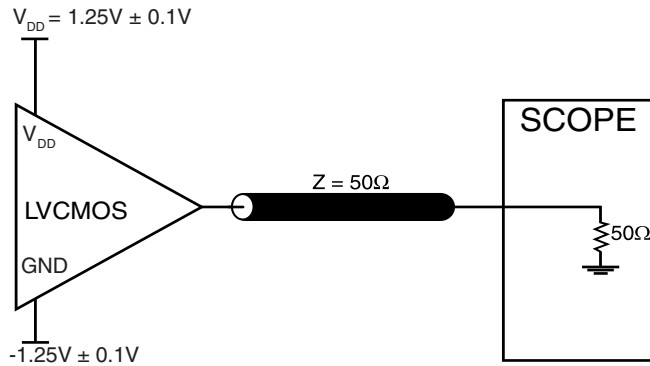
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DD}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}/2$.

NOTE 3: Not production tested, guaranteed by characterization.

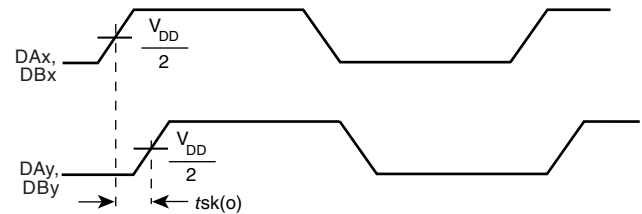


PARAMETER MEASUREMENT INFORMATION

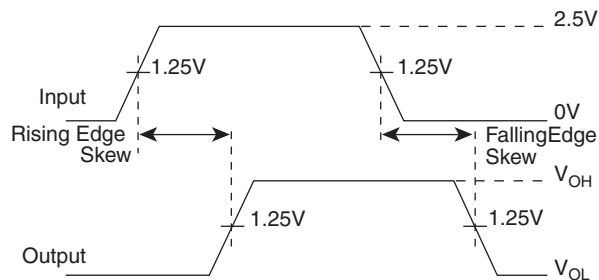


This circuit is used for test purposes only,
not intended for application use.

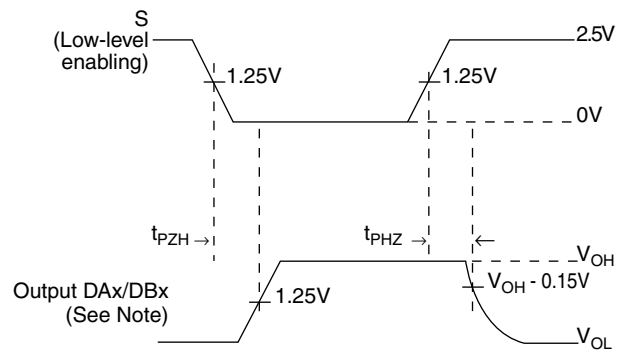
2.5V OUTPUT LOAD AC TEST CIRCUIT



OUTPUT SKEW

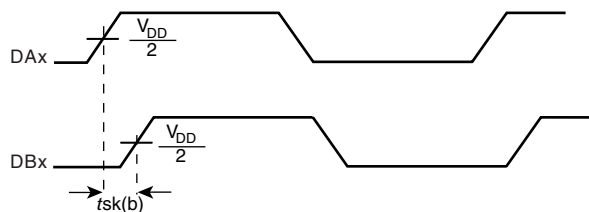


RISE & FALLING EDGE SKEW

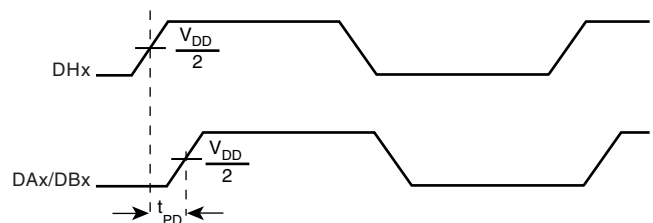


NOTE: The output is high except when disabled by the S control.

3-STATE OUTPUT ENABLE/DISABLE TIMES



BANK SKEW



PROPAGATION DELAY



RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR A 72-BALL TFBGA

θ_{JA} by Velocity (Millimeter Feet per Second)			
	0	1	2
Two-Layer PCB, JEDEC Standard Test Boards	50.04°C/W	43.18°C/W	41.17°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

TRANSISTOR COUNT

The transistor count for ICS83841 is: 261



PACKAGE OUTLINE - H SUFFIX FOR A 72-BALL TFBGA

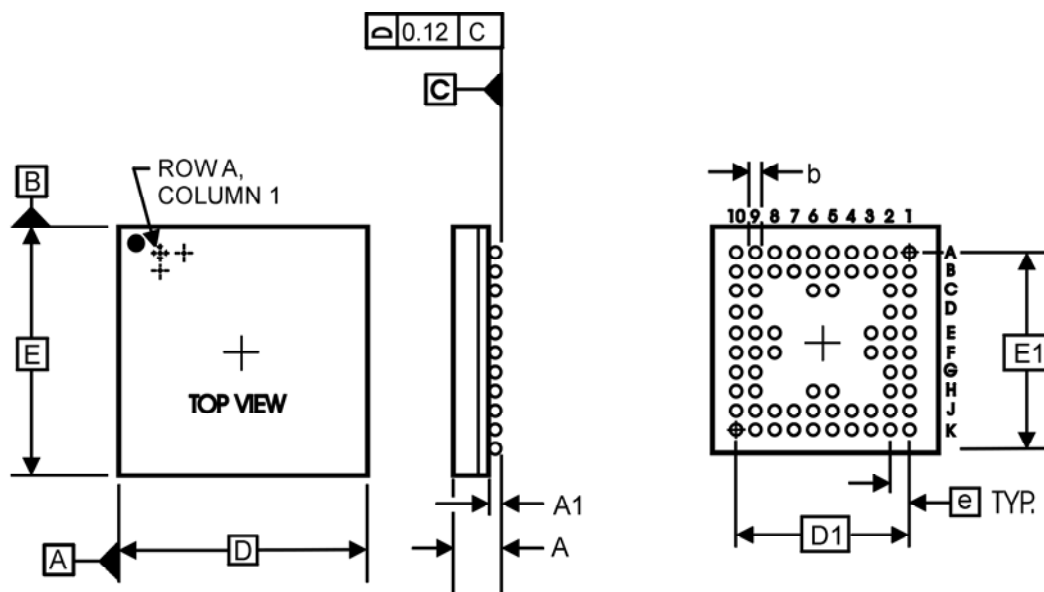


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	FBGA		
	MINIMUM	NOMINAL	MAXIMUM
	72 Balls, 6x6mm, 10x10 Pattern		
A	1.0	1.1	1.2
A1	0.165	0.2	0.235
b	0.25	0.3	0.35
D	6.00 BSC		
D1	4.50 BSC		
E	6.00 BSC		
E1	4.50 BSC		
e	0.50 BSC		

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MO-195



Integrated
Circuit
Systems, Inc.

ICS83841

20 Bit, DDR SDRAM 2:1 MUX

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS83841BH	ICS83841BH	72-Ball TFBGA	TBD	0°C to 70°C
ICS83841BHT	ICS83841BH	72-Ball TFBGA	2500 Tape & Reel	0°C to 70°C
ICS83841BHLF	ICS83841BHLF	72-Ball, Lead Free, TFBGA	TBD	0°C to 70°C
ICS83841BHLFT	ICS83841BHLF	72-Ball, Lead Free, TFBGA	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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20 Bit, DDR SDRAM 2:1 MUX

REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
A	T8	8	Ordering Information table - corrected Lead-Free marking and added Lead-Free note.	1/20/06