



GENERAL DESCRIPTION

The ICS843404 is a low phase noise Fibre Channel Clock Generator and is a member of the HiPerClockS™ family of high performance clock solutions from ICS. The device provides two banks of one LVPECL output per bank and one bank of two LVDS outputs. Each bank can be independently set by using their respective frequency select pins for the following output frequencies: 318.75MHz, 212.5MHz, 159.375MHz or 106.25MHz, using a 25.5MHz 18pF parallel resonant crystal. The ICS843404 can also be driven from a 25.5MHz single-ended reference clock. For system debug or test purposes, the PLL can be bypassed using the VCO_SEL pin.

PIN ASSIGNMENT

MR	1	28	LVDS_FSEL0
VCO_SEL	2	27	LVDS_FSEL1
VDDO_LVDS	3	26	VDDO_LVPECL
LVDS0	4	25	LVPECLA0
nLVDS0	5	24	nLVPECLA0
LVDS1	6	23	LVPECLB0
nLVDS1	7	22	nLVPECLB0
nc	8	21	XTAL_SEL
LVPECL_FSELB0	9	20	TEST_CLK
LVPECL_FSELB1	10	19	GND
nc	11	18	GND
VDDA	12	17	XTAL_IN
LVPECL_FSELA0	13	16	XTAL_OUT
VDD	14	15	LVPECL_FSELA1

ICS843404

28-Lead TSSOP, 173-MIL
4.4mm x 9.7mm x 0.92mm
body package

G Package
Top View

FEATURES

- Three banks of outputs: one bank of two LVDS outputs and two banks of one LVPECL output
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended reference clock input
- Four independently selectable output frequency on each bank: 318.75MHz, 212.5MHz, 159.375MHz and 106.25MHz
- Maximum output frequency: 318.75MHz
- Crystal input frequency: 25.5MHz
- V_{DDO_LVPECL} can be set for 3.3V or 2.5V, allowing the device to generate 3.3V or 2.5V LVPECL levels
- RMS phase jitter at 106.25MHz, using a 25.5MHz crystal (637kHz to 10MHz intergration): 2.65ps (typical)

Offset	Noise Power
100Hz	-89.1 dBc/Hz
1kHz	-112.7 dBc/Hz
10kHz	-128.0 dBc/Hz
100kHz	-130.2 dBc/Hz

- Supply voltage modes:
 - $V_{DD} = V_{DDA} = 3.3V$
 - $V_{DDO_LVPECL} = 3.3V$ or $2.5V$
 - $V_{DDO_LVDS} = 3.3V$
- 0°C to 70°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages
- Industrial temperature information available upon request

BLOCK DIAGRAM

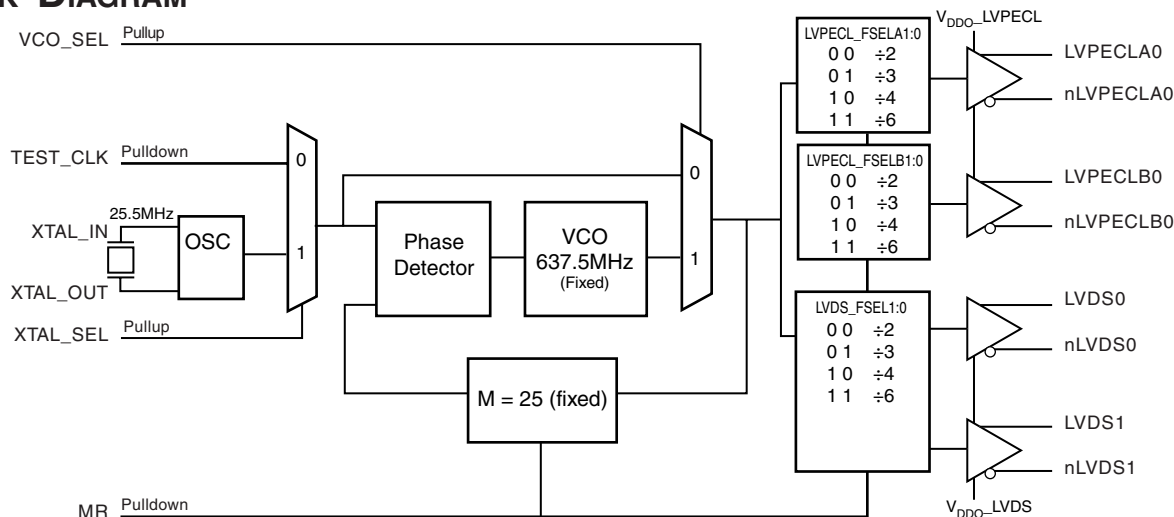




TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs LVPECLx/LVDSx to go low and the inverted outputs nLVPECLx/nLVDSx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
2	VCO_SEL	Input	Pullup	VCO select pin. When HIGH, PLL is enabled. When LOW, PLL is in Bypass mode. LVCMOS/LVTTL interface levels.
3	V _{DDO} —LVDS	Power		Output supply pin for LVDS outputs.
4, 5	LVDS0, nLVDS0	Output		Differential output pair. LVDS interface levels.
6, 7	LVDS1, nLVDS1	Output		Differential output pair. LVDS interface levels.
8, 11	nc	Unused		No connect.
9	LVPECL_FSELB0	Input	Pulldown	Frequency select pin for LVPECLB outputs. See Table 3B. LVCMOS/LVTTL interface levels.
10	LVPECL_FSELB1	Input	Pullup	Frequency select pin for LVPECLB outputs. See Table 3B. LVCMOS/LVTTL interface levels.
12	V _{DDA}	Power		Analog supply pin.
13	LVPECL_FSELA0	Input	Pulldown	Frequency select pin for LVPECLA outputs. See Table 3B. LVCMOS/LVTTL interface levels.
14	V _{DD}	Power		Core supply pin.
15	LVPECL_FSELA1	Input	Pullup	Frequency select pin for LVPECLA outputs. See Table 3B. LVCMOS/LVTTL interface levels.
16, 17	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_IN is the input, XTAL_OUT is the output.
18, 19	GND	Power		Negative supply pin.
20	TEST_CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
21	XTAL_SEL	Input	Pullup	Selects between crystal or TEST_CLK inputs as the the PLL Reference source. Selects XTAL inputs when HIGH. Selects TEST_CLK when LOW. LVCMOS/LVTTL interface levels.
22, 23	nLVPECLB0, LVPECLB0	Output		Differential output pair. LVPECL interface levels.
24, 25	nLVPECLA0, LVPECLA0	Output		Differential output pair. LVPECL interface levels.
26	V _{DDO} —LVPECL	Power		Output supply pin for LVPECL outputs.
27, 28	LVDS_FSEL1, LVDS_FSEL0	Input	Pulldown	Frequency select pins for LVDS outputs. See Table 3A. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ



TABLE 3A. LVDS FREQUENCY SELECT FUNCTION TABLE

Inputs			LVDS Output Frequency (MHz) (25.5MHz Crystal)
LVDS_FSEL1	LVDS_FSEL0	LVDS Output Divider	
0	0	2	318.75 (default)
0	1	3	212.5
1	0	4	159.375
1	1	6	106.25

TABLE 3B. LVPECLA0 FREQUENCY SELECT FUNCTION TABLE

Inputs			LVPECLA0 Output Frequency (MHz) (25.5MHz Crystal)
LVPECL_FSELA1	LVPECL_FSELA0	LVPECLA0 Output Divider	
0	0	2	318.75
0	1	3	212.5
1	0	4	159.375 (default)
1	1	6	106.25

TABLE 3C. LVPECLB0 FREQUENCY SELECT FUNCTION TABLE

Inputs			LVPECLB0 Output Frequency (MHz) (25.5MHz Crystal)
LVPECL_FSELB1	LVPECL_FSELB0	LVPECLB0 Output Divider	
0	0	2	318.75
0	1	3	212.5
1	0	4	159.375 (default)
1	1	6	106.25



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, I_O (LVPECL Outputs)	
Continuous Current	50mA
Surge Current	100mA
Outputs, I_O (LVDS Outputs)	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	49.8°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO_LVPECL} = V_{DDO_LVDS} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO_LVPECL}	Output Supply Voltage		3.135	3.3	3.465	V
V_{DDO_LVDS}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			100		mA
I_{DDA}	Analog Supply Current			25		mA
I_{DDO_LVPECL}	Output Supply Current			20		mA
I_{DDO_LVDS}	Output Supply Current			55		mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO_LVPECL} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO_LVPECL}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			70		mA
I_{DDA}	Analog Supply Current			20		mA
I_{DDO_LVPECL}	Output Supply Current			20		mA



TABLE 4C. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO_LVPECL} = V_{DDO_LVDS} = 3.3V \pm 5\%$,

$V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO_LVPECL} = 2.5V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	TEST_CLK, MR, LVPECL_FSELA0, LVPECL_FSELB0, LVDS_FSEL0, LVDS_FSEL1	$V_{DD} = V_{IN} = 3.465V$		150	μA
		LVPECL_FSELA1, LVPECL_FSELB1, VCO_SEL, XTAL_SEL	$V_{DD} = V_{IN} = 3.465V$	5		μA
I_{IL}	Input Low Current	TEST_CLK, MR, LVPECL_FSELA0, LVPECL_FSELB0, LVDS_FSEL0, LVDS_FSEL1	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		μA
		LVPECL_FSELA1, LVPECL_FSELB1, VCO_SEL, XTAL_SEL	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		μA

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO_LVPECL} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO_LVPECL} - 1.4$		$V_{DDO_LVPECL} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO_LVPECL} - 2.0$		$V_{DDO_LVPECL} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO_LVPECL} - 2V$.

TABLE 4E. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO_LVDS} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			4		mV
V_{OS}	Offset Voltage			1.35		V
ΔV_{OS}	V_{OS} Magnitude Change			5		mV

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25.5		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.



TABLE 6A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO_LVPECL} = V_{DDO_LVDS} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Crystal Input Frequency			25.5		MHz
f_{MAX}	Output Frequency				318.75	MHz
$tsk(b)$	Bank Skew; NOTE 1	LVDS			30	ps
		LVPECL			65	ps
$tsk(o)$	Output Skew; NOTE 2, 3				585	ps
$f_{jit}(\emptyset)$	RMS Phase Jitter, (Random); NOTE 4	LVPECL	318.75MHz (12kHz - 20MHz)		3.22	ps
			212.5MHz (1.274MHz - 20MHz)		3.18	ps
			159.375MHz (12kHz - 20MHz)		3.06	ps
			106.25MHz (637kHz - 10MHz)		2.65	ps
		LVDS	318.75MHz (12kHz - 20MHz)		2.84	ps
			212.5MHz (1.274MHz - 20MHz)		2.93	ps
			159.375MHz (12kHz - 20MHz)		4.32	ps
			106.25MHz (637kHz - 10MHz)		3.81	ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	350		850	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the differential cross point.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: All phase noise plots are taken using 25.5MHz crystal. Refer to the Phase Noise Plots on the next page.

TABLE 6B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO_LVPECL} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

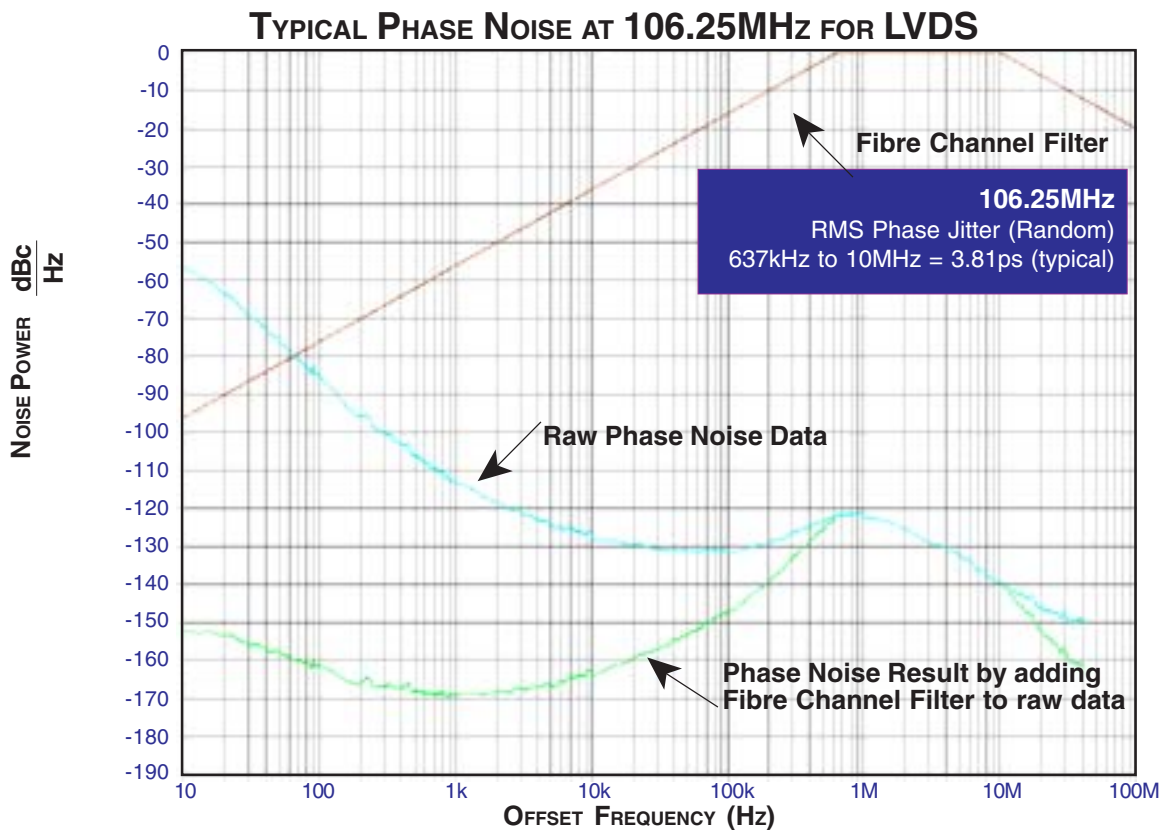
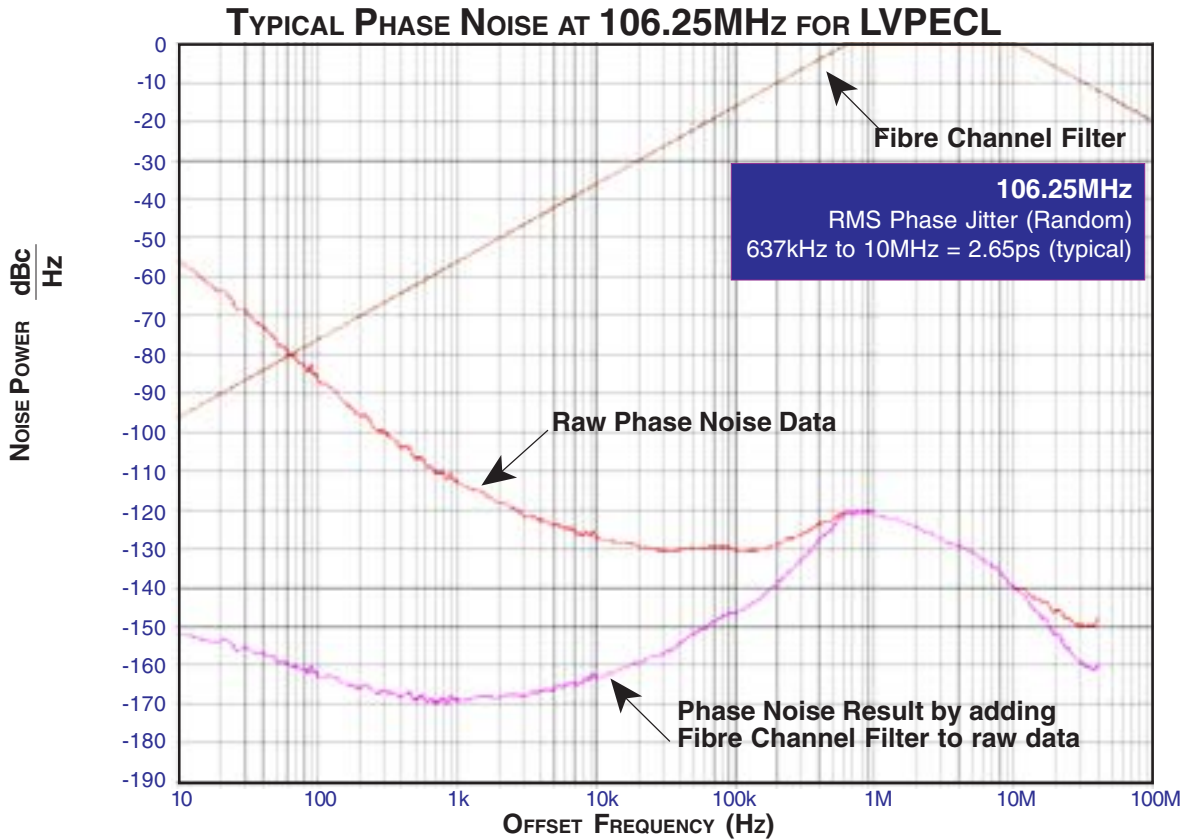
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Crystal Input Frequency			25.5		MHz
f_{MAX}	Output Frequency				318.75	MHz
$tsk(b)$	Bank Skew; NOTE 1	LVDS			30	ps
		LVPECL			65	ps
$tsk(o)$	Output Skew; NOTE 2, 3				585	ps
$f_{jit}(\emptyset)$	RMS Phase Jitter, (Random); NOTE 4	LVPECL	318.75MHz (12kHz - 20MHz)		2.84	ps
			212.5MHz (1.274MHz - 20MHz)		4.22	ps
			159.375MHz (12kHz - 20MHz)		4.74	ps
			106.25MHz (637kHz - 10MHz)		3.96	ps
		LVDS	318.75MHz (12kHz - 20MHz)		2.84	ps
			212.5MHz (1.274MHz - 20MHz)		2.93	ps
			159.375MHz (12kHz - 20MHz)		4.32	ps
			106.25MHz (637kHz - 10MHz)		3.81	ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	350		850	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the differential cross point.

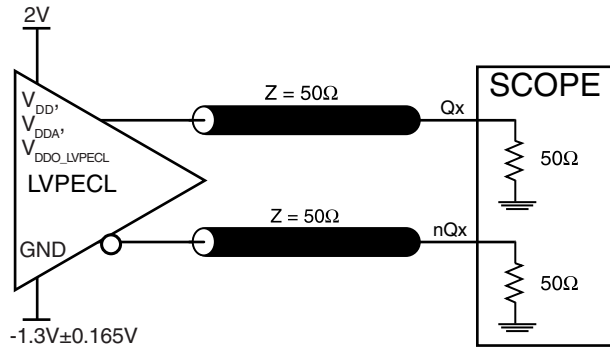
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: All phase noise plots are taken using 25.5MHz crystal. Refer to the Phase Noise Plots on the next page.

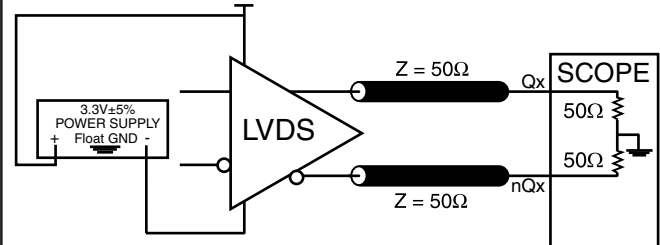




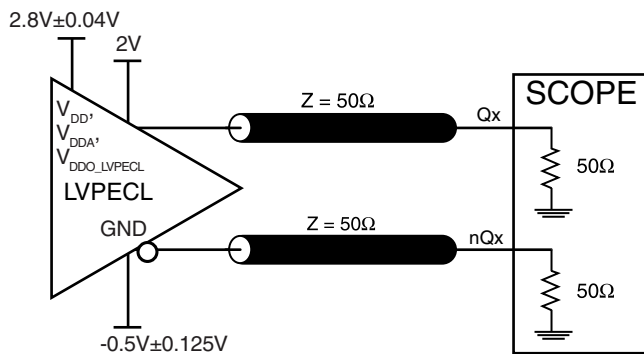
PARAMETER MEASUREMENT INFORMATION



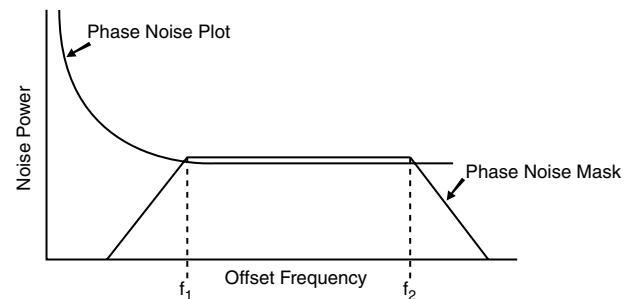
LVPECL 3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



LVDS 3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT

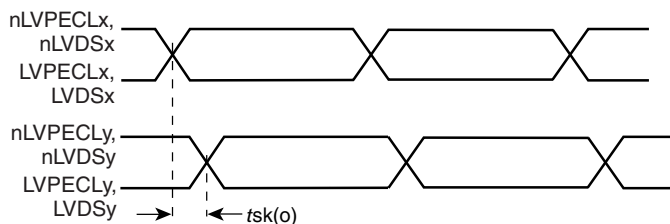


LVPECL 3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT

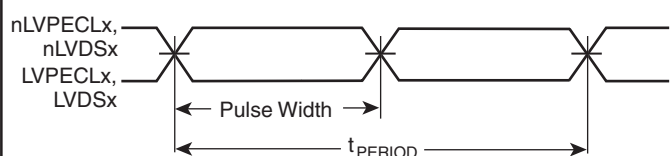


$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

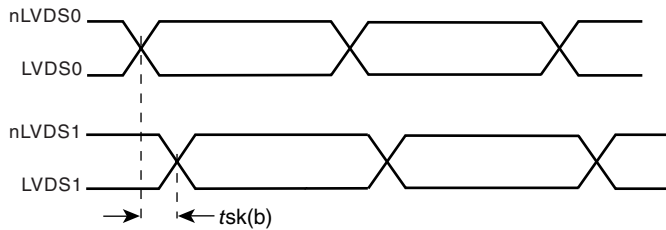
RMS PHASE JITTER



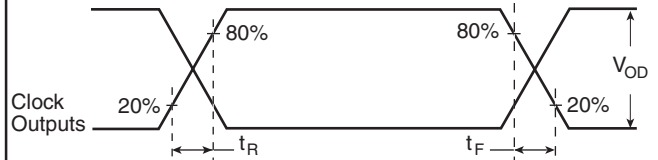
OUTPUT SKEW



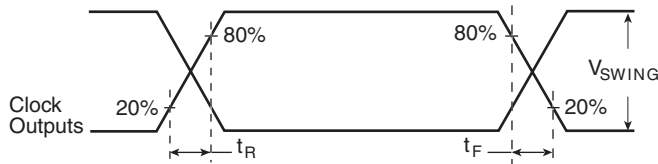
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



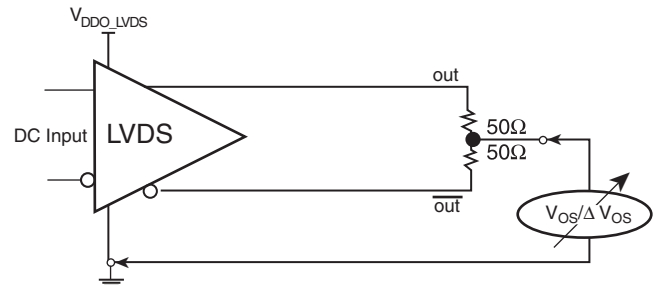
LVDS BANK SKEW (MAXIMUM VALUE)



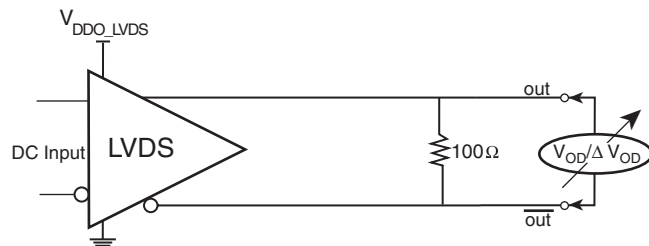
LVDS OUTPUT RISE/FALL TIME



LVPECL OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP



APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843404 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} , and V_{DDO_X} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 24Ω resistor along with a $10\mu\text{F}$ and a $.01\mu\text{F}$ bypass capacitor should be connected to each V_{DDA} . The 24Ω resistor can also be replaced by a ferrite bead.

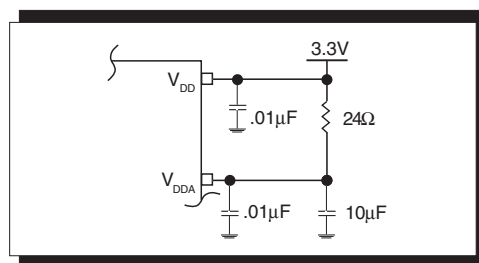


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843404 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2*

below were determined using a 25.5MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

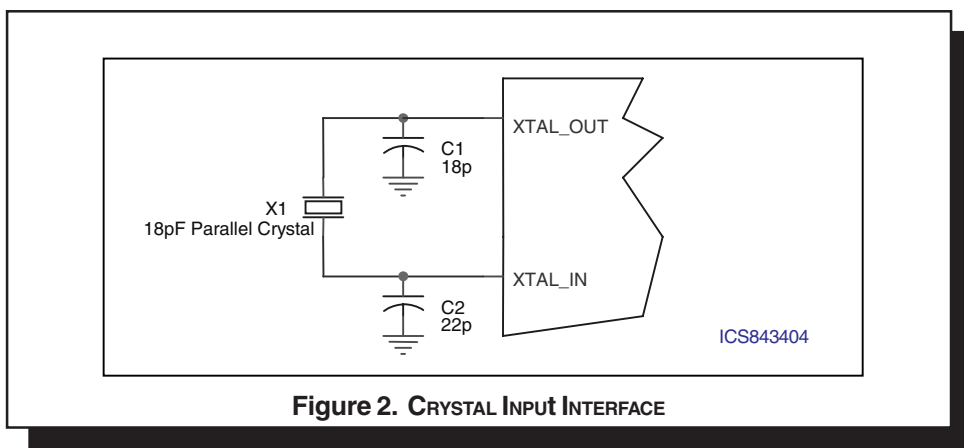


Figure 2. CRYSTAL INPUT INTERFACE



RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from XTAL_IN to ground.

TEST_CLK INPUT:

For applications not requiring the use of the clock, it can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from the TEST_CLK to ground.

LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

OUTPUTS:

LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS OUTPUT

All unused LVDS output pairs can be either left floating or terminated with 100 Ω across. If they are left floating, we recommend that there is no trace attached.

LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 3*. In a 100 Ω differential transmission line environment, LVDS drivers require a matched load termination of 100 Ω across near

the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.

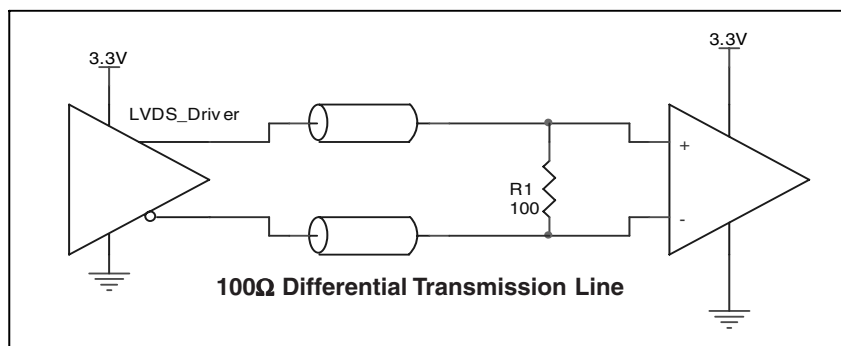


FIGURE 3. TYPICAL LVDS DRIVER TERMINATION



TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are

designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

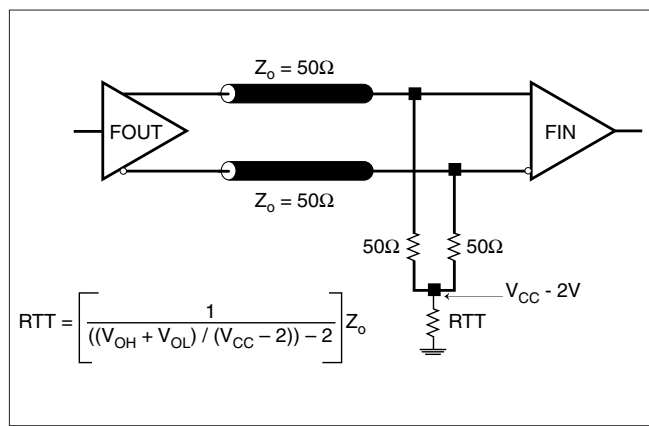


FIGURE 4A. LVPECL OUTPUT TERMINATION

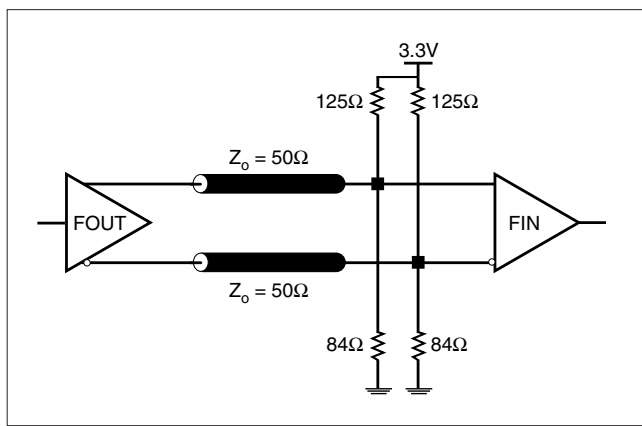


FIGURE 4B. LVPECL OUTPUT TERMINATION



TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{DD} - 2V$. For $V_{DDO} = 2.5V$, the $V_{DDO} - 2V$ is very close to

ground level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

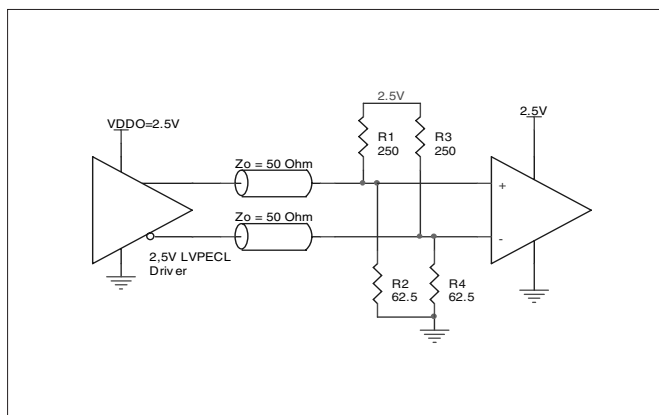


FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

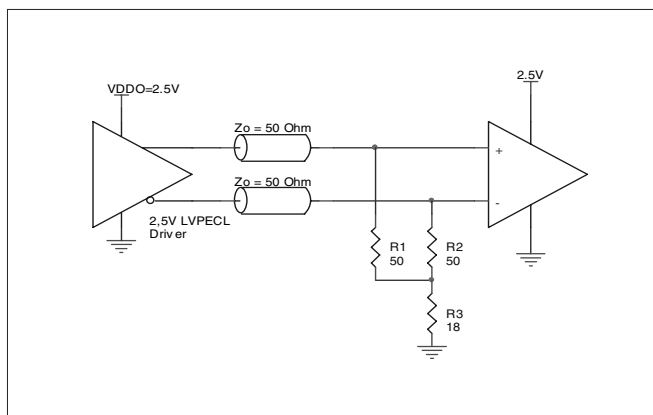


FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

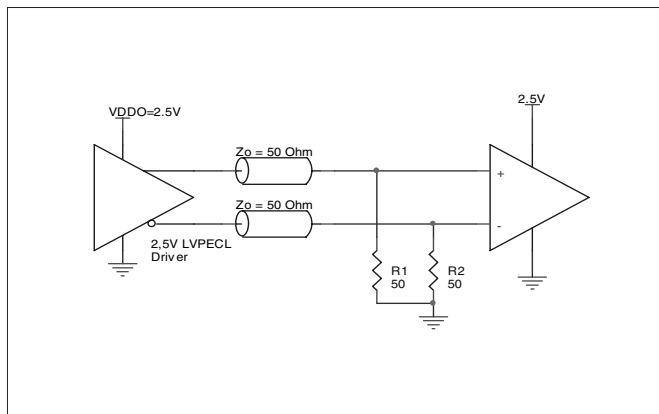
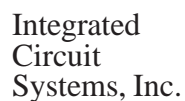


FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE



LAYOUT GUIDELINE

18pF parallel resonant 25.5MHz crystal is used. The C1=27pF and C2=33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

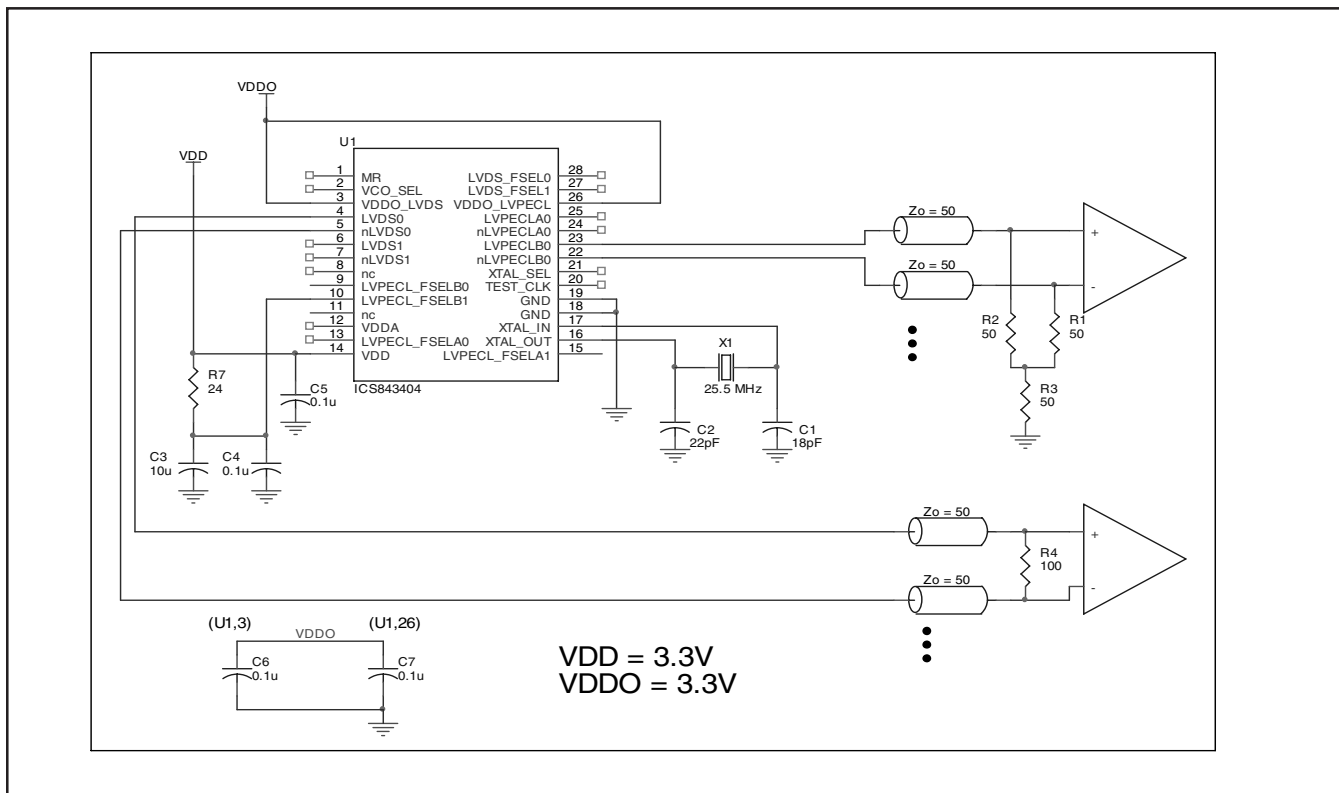


FIGURE 6. ICS843404 SCHEMATIC EXAMPLE



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843404. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843404 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{DD_TYP} = 3.465V * 100mA = 346.5mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is $2 * 30mW = 60mW$

Total Power_{MAX} (3.465V, with all outputs switching) = $346.5mW + 60mW = 406.5mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 43.9°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$70°C + 0.407W * 43.9°C/W = 87.8°C$. This is well below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 28-PIN TSSOP, FORCED CONVECTION

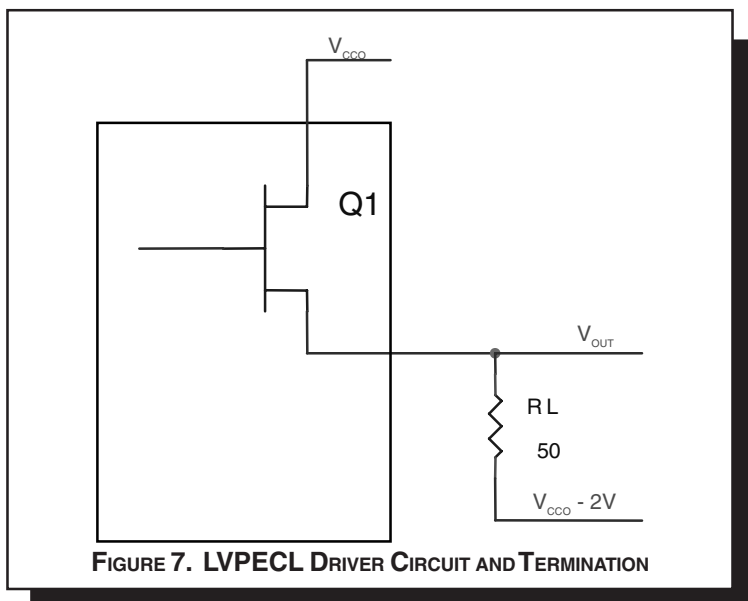
θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	82.9°C/W	68.7°C/W	60.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	49.8°C/W	43.9°C/W	41.2°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			



3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in Figure 7.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{DD} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.9V$

$$(V_{DD_MAX} - V_{OH_MAX}) = 0.9V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.7V$

$$(V_{DD_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{DD_MAX} - 2V))/R_L] * (V_{DD_MAX} - V_{OH_MAX}) = [(2V - (V_{DD_MAX} - V_{OH_MAX}))/R_L] * (V_{DD_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd_L = [(V_{OL_MAX} - (V_{DD_MAX} - 2V))/R_L] * (V_{DD_MAX} - V_{OL_MAX}) = [(2V - (V_{DD_MAX} - V_{OL_MAX}))/R_L] * (V_{DD_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

Total Power Dissipation per output pair = $Pd_H + Pd_L = \mathbf{30mW}$



RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 28 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	82.9°C/W	68.7°C/W	60.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	49.8°C/W	43.9°C/W	41.2°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

TRANSISTOR COUNT

The transistor count for ICS843404 is: 2314



PACKAGE OUTLINE - G SUFFIX FOR 28 LEAD TSSOP

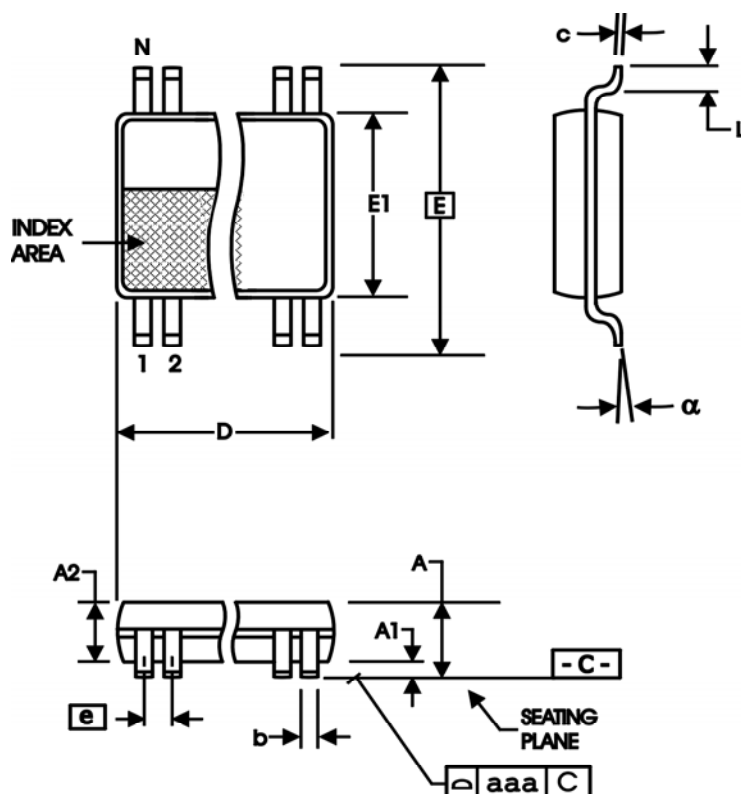


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	28	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153



Integrated
Circuit
Systems, Inc.

ICS843404

LVCMOS/CRYSTAL-TO-3.3V LVPECL AND LVDS CLOCK GENERATOR

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843404AG	ICS843404AG	28 Lead TSSOP	tube	0°C to 70°C
ICS843404AGT	ICS843404AG	28 Lead TSSOP	1000 tape & reel	0°C to 70°C
ICS843404AGLF	ICS843404AGLF	28 Lead "Lead Free" TSSOP	tube	0°C to 70°C
ICS843404AGLFT	ICS843404AGLF	28 Lead "Lead Free" TSSOP	1000 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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