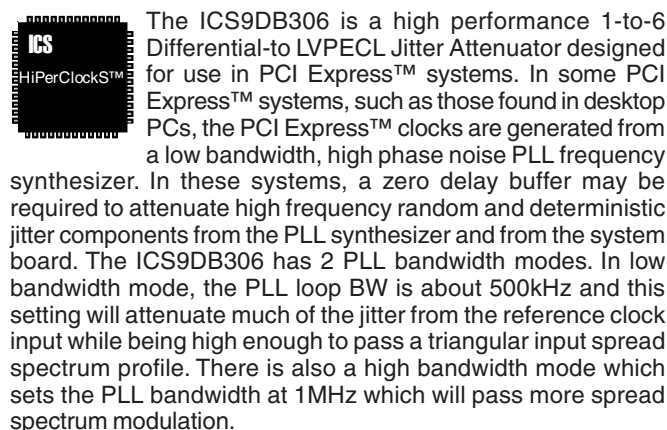


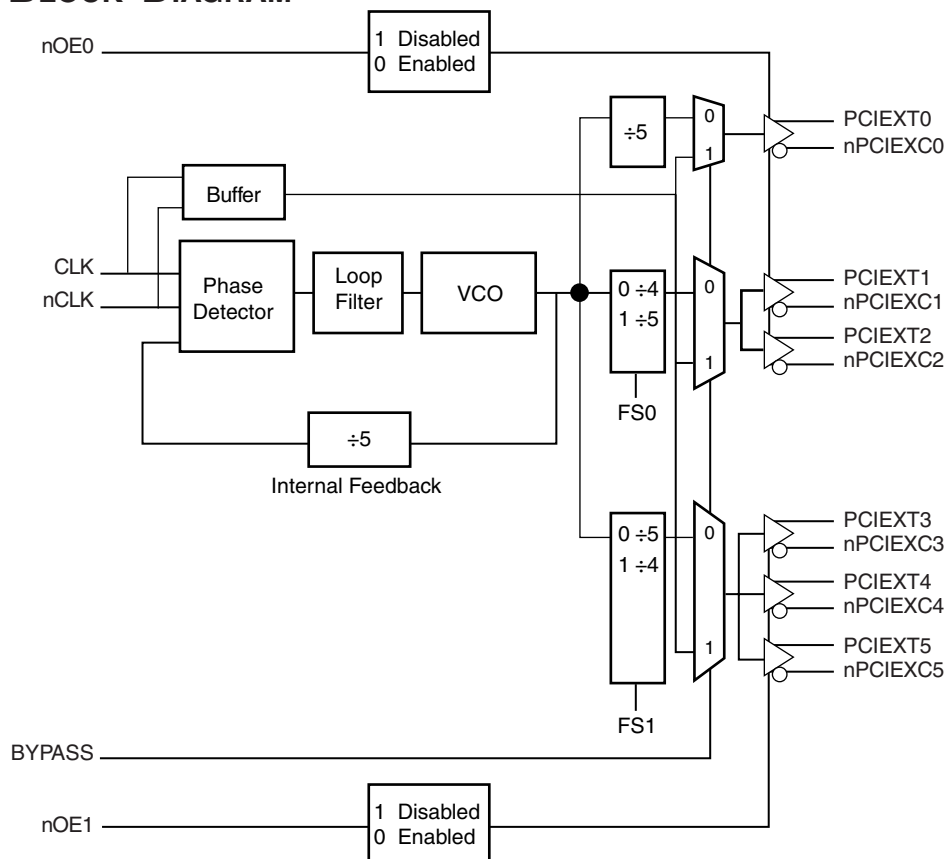
## GENERAL DESCRIPTION



## Features

- Six differential LVPECL output pairs
- 1 differential clock input
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 140MHz
- Output skew: 135ps (maximum)
- Cycle-to-Cycle jitter: 25ps (maximum)
- RMS phase jitter @ 100MHz, (1.5MHz - 22MHz): 3ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Lead-Free package fully RoHS compliant
- Industrial temperature information available upon request

## BLOCK DIAGRAM



## PIN ASSIGNMENT

V <sub>EE</sub>	1	28	V <sub>CC</sub>
PCIEXT1	2	27	PCIEXC0
PCIEXC1	3	26	PCIEXT0
PCIEXT2	4	25	FS0
PCIEXC2	5	24	nCLK
V <sub>CC</sub>	6	23	CLK
nOE0	7	22	PLL_BW
nOE1	8	21	V <sub>CCA</sub>
V <sub>CC</sub>	9	20	V <sub>EE</sub>
PCIEXC3	10	19	BYPASS
PCIEXT3	11	18	FS1
PCIEXC4	12	17	PCIEXT5
PCIEXT4	13	16	PCIEXC5
V <sub>EE</sub>	14	15	V <sub>CC</sub>

## ICS9DB306

**28-Lead TSSOP, 173-MIL**  
4.4mm x 9.7mm x 0.92mm  
body package  
**L Package**  
Top View

## ICS9DB306

**28-Lead, 209-MIL SSOP**  
5.3mm x 10.2mm x 1.75mm  
body package  
**F Package**  
Top View



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 14, 20	V <sub>EE</sub>	Power		Negative supply pins.
2, 3	PCIEXT1, PCIEXC1	Output		Differential output pairs. LVPECL interface levels.
4, 5	PCIEXT2, PCIEXC2	Output		Differential output pairs. LVPECL interface levels.
6, 9, 15, 28	V <sub>CC</sub>	Power		Core supply pins.
7, 8	nOE0, nOE1	Input	Pulldown	Output enable. When HIGH, forces true outputs (PCIEXTx) to go LOW and the inverted outputs (PCIEXCx) to go HIGH. When LOW, outputs are enabled. LVCMOS/LVTTL interface levels.
10, 11	PCIEXC3, PCIEXT3	Output		Differential output pairs. LVPECL interface levels.
12, 13	PCIEXC4, PCIEXT4	Output		Differential output pairs. LVPECL interface levels.
16, 17	PCIEXC5, PCIEXT5	Output		Differential output pairs. LVPECL interface levels.
18	FS1		Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
19	BYPASS	Input	Pulldown	Bypass select pin. When HIGH, the PLL is in bypass mode, and the device can function as a 1:6 buffer. LVCMOS/LVTTL interface levels.
21	V <sub>CCA</sub>	Power		Analog supply pin. Requires 24Ω series resistor.
22	PLL_BW	Input	Pullup	Selects PLL Bandwidth input. LVCMOS/LVTTL interface levels.
23	CLK	Input	Pulldown	Non-inverting differential clock input.
24	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. V <sub>CC</sub> /2 default when left floating.
25	FS0	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
26, 27	PCIEXT0, PCIEXC0	Output		Differential output pairs. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		KΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		KΩ

**TABLE 3A. RATIO OF OUTPUT FREQUENCY TO INPUT FREQUENCY FUNCTION TABLE, FS0**

Inputs	Outputs		
FS0	PCIEX0	PCIEX1	PCIEX2
0	1	5/4	5/4
1	1	1	1

**TABLE 3B. RATIO OF OUTPUT FREQUENCY TO INPUT FREQUENCY FUNCTION TABLE, FS1**

Inputs	Outputs		
FS1	PCIEX3	PCIEX4	PCIEX5
0	1	1	1
1	5/4	5/4	5/4

**TABLE 3C. OUTPUT ENABLE FUNCTION TABLE, nOE0**

Inputs	Outputs
nOE0	PCIEX0:2
0	Enabled
1	Disabled

**TABLE 3D. OUTPUT ENABLE FUNCTION TABLE, nOE1**

Inputs	Outputs
nOE1	PCIEX3:5
0	Enabled
1	Disabled

**TABLE 3E. PLL BANDWIDTH FUNCTION TABLE**

Inputs	Bandwidth
PLL_BW	
0	500kHz
1	1MHz

**TABLE 3F. PLL MODE FUNCTION TABLE**

Inputs	PLL Mode
BYPASS	
1	Disabled
0	Enabled



#### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	49.8°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$I_{CC}$	Power Supply Current				135	mA
$I_{CCA}$	Analog Supply Current				25	mA

**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{CC} + 0.3$	mV
$V_{IL}$	Input Low Voltage		-0.3		0.8	mV
$I_{IH}$	Input High Current	nOE0, nOE1, FS1, BYPASS	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		FS0, PLL_BW			5	$\mu A$
$I_{IL}$	Input Low Current	nOE0, nOE1, FS1, BYPASS	$V_{CC} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		FS0, PLL_BW		-150		$\mu A$

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK, nCLK	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
$I_{IL}$	Input Low Current	CLK, nCLK	$V_{CC} = 3.465V, V_{IN} = 0V$		150	$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is  $V_{CC} + 0.3V$ .



**TABLE 4D. LVPECL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**TABLE 5. AC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				140	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 2			55	135	ps
$f_{jit(cc)}$	Cycle-to-Cycle Jitter, NOTE 2				25	ps
$f_{jit(\emptyset)}$	RMS Phase Jitter (Random); NOTE 3	Integration Range: 1.5MHz - 22MHz		3		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		48		52	%

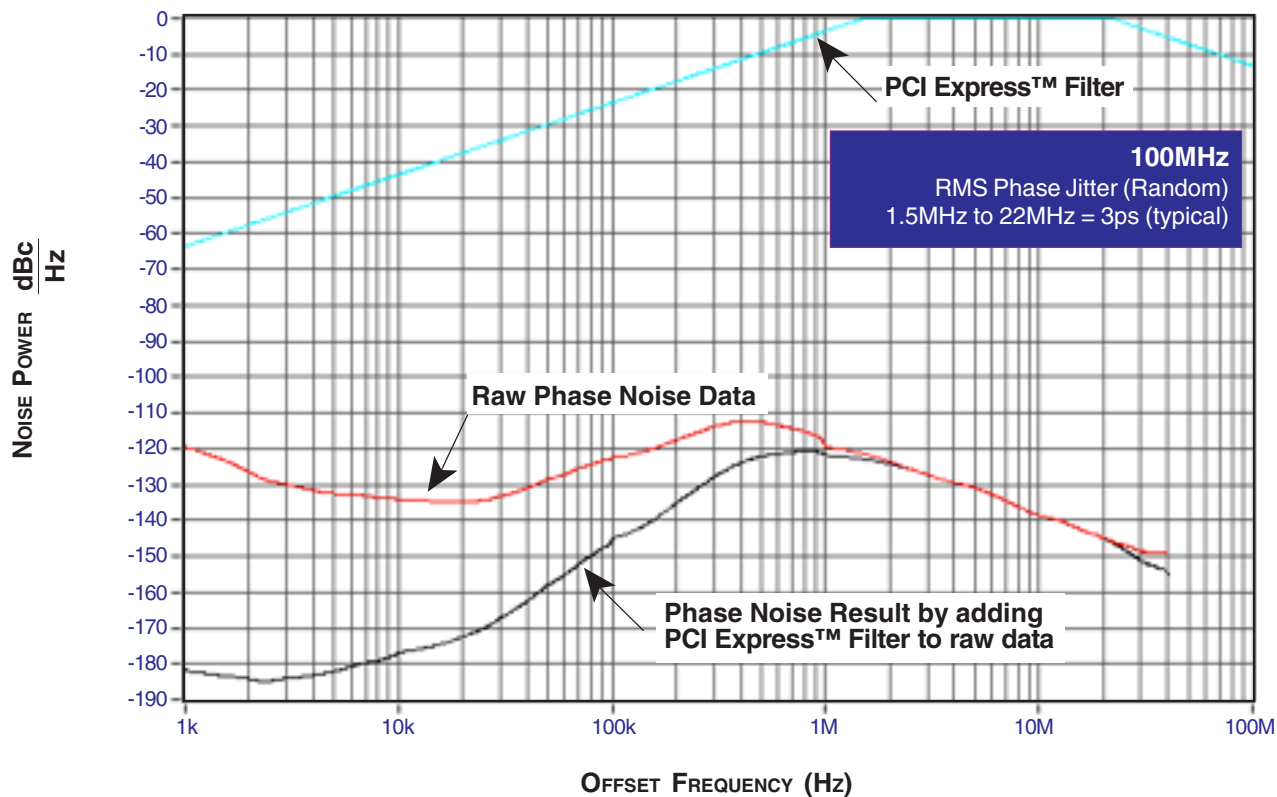
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions.  
Measured at the output differential cross points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plot following this section.



### TYPICAL PHASE NOISE AT 100MHz



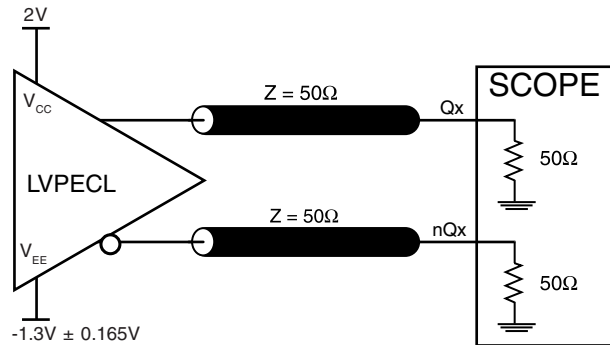
The illustrated phase noise plot was taken using a low phase noise signal generator, the noise floor of the signal generator is less than that of the device under test.

Using this configuration allows one to see the true spectral purity or phase noise performance of the PLL in the device under

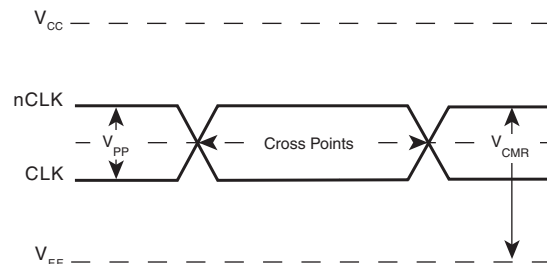
test. Due to the tracking ability of a PLL, it will track the input signal up to its loop bandwidth. Therefore, if the input phase noise is greater than that of the VCO, it will increase the output phase noise performance of the device. It is recommended that the phase noise performance of the input is verified in order to achieve the above phase noise performance.



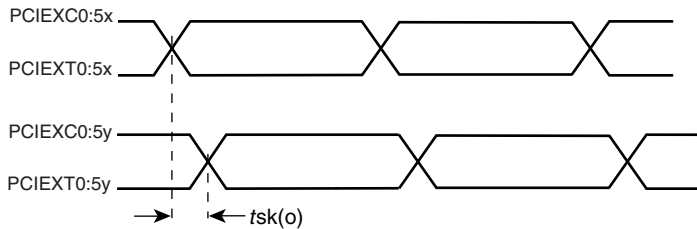
## PARAMETER MEASUREMENT INFORMATION



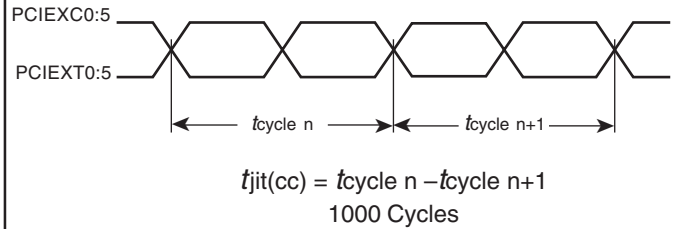
**3.3V OUTPUT LOAD AC TEST CIRCUIT**



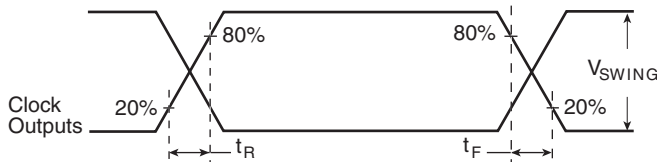
**DIFFERENTIAL INPUT LEVEL**



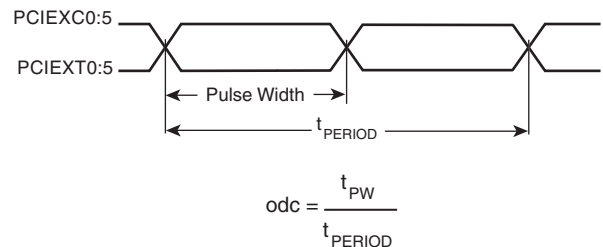
**OUTPUT SKEW**



**CYCLE-TO-CYCLE JITTER**



**OUTPUT RISE/FALL TIME**



**OUTPUT DUTY CYCLE/PULSE WIDTH PERIOD**



## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS9DB306 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$  and  $V_{CCA}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $24\Omega$  resistor along with a  $10\mu F$  and a  $.01\mu F$  bypass capacitor should be connected to each  $V_{CCA}$  pin.

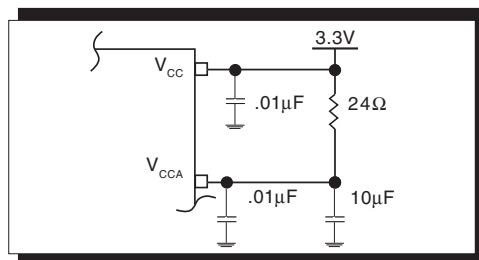


FIGURE 1. POWER SUPPLY FILTERING

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors  $R1$ ,  $R2$  and  $C1$ . This bias circuit should be located as close as possible to the input pin. The ratio

of  $R1$  and  $R2$  might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

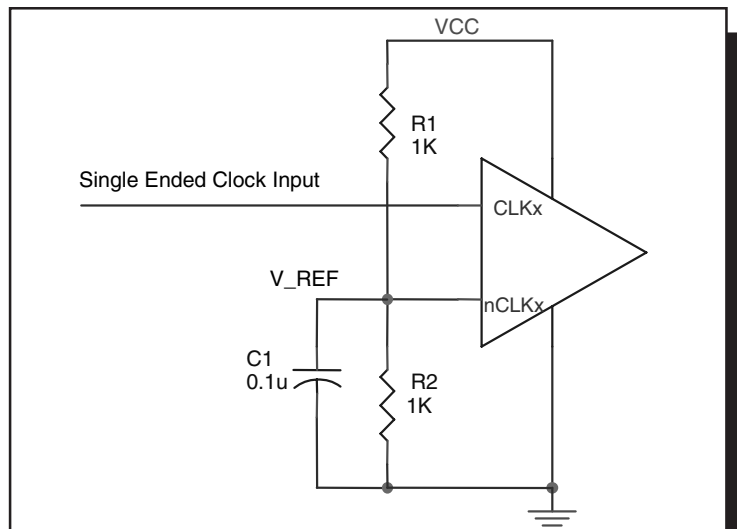


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT



## TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive

50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

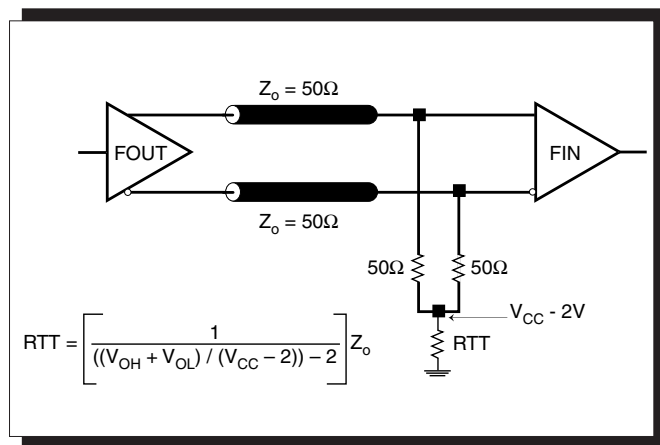


FIGURE 3A. LVPECL OUTPUT TERMINATION

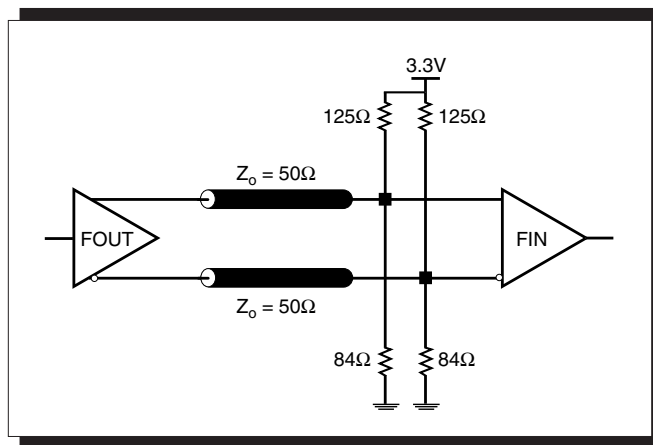


FIGURE 3B. LVPECL OUTPUT TERMINATION

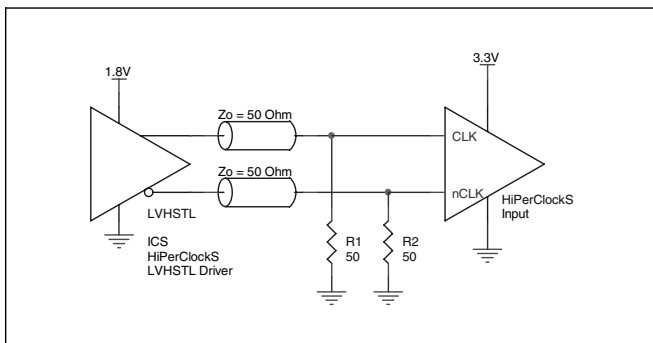




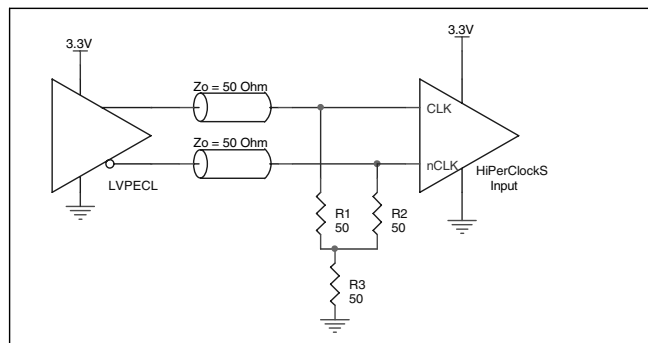
## DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{\text{SWING}}$  and  $V_{\text{OH}}$  must meet the  $V_{\text{PP}}$  and  $V_{\text{CMR}}$  input requirements. Figures 4A to 4D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

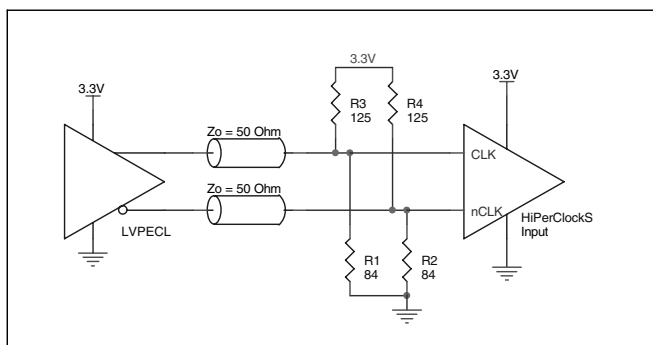
here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A*, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



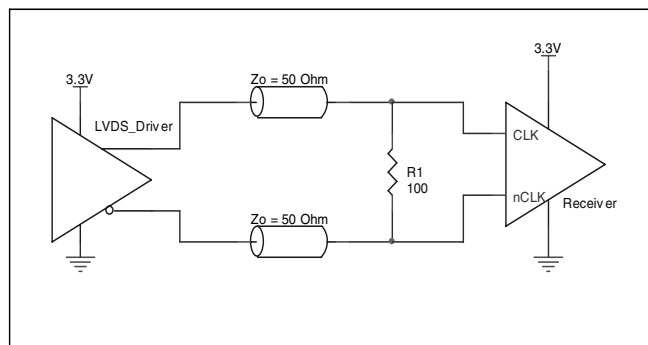
**FIGURE 4A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER**



**FIGURE 4B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 4C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 4D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**



## SCHEMATIC EXAMPLE

Figure 5 shows an example of ICS9DB306 application schematic. In this example, the device is operated at  $V_{CC} = 3.3V$ . The decoupling capacitor should be located as close as possible to the power pin. The input is driven by a HCSL driver. For

LVPECL output drivers, one of terminations approaches is shown in this schematic. For additional termination approaches, please refer to the LVPECL Termination Application Note.

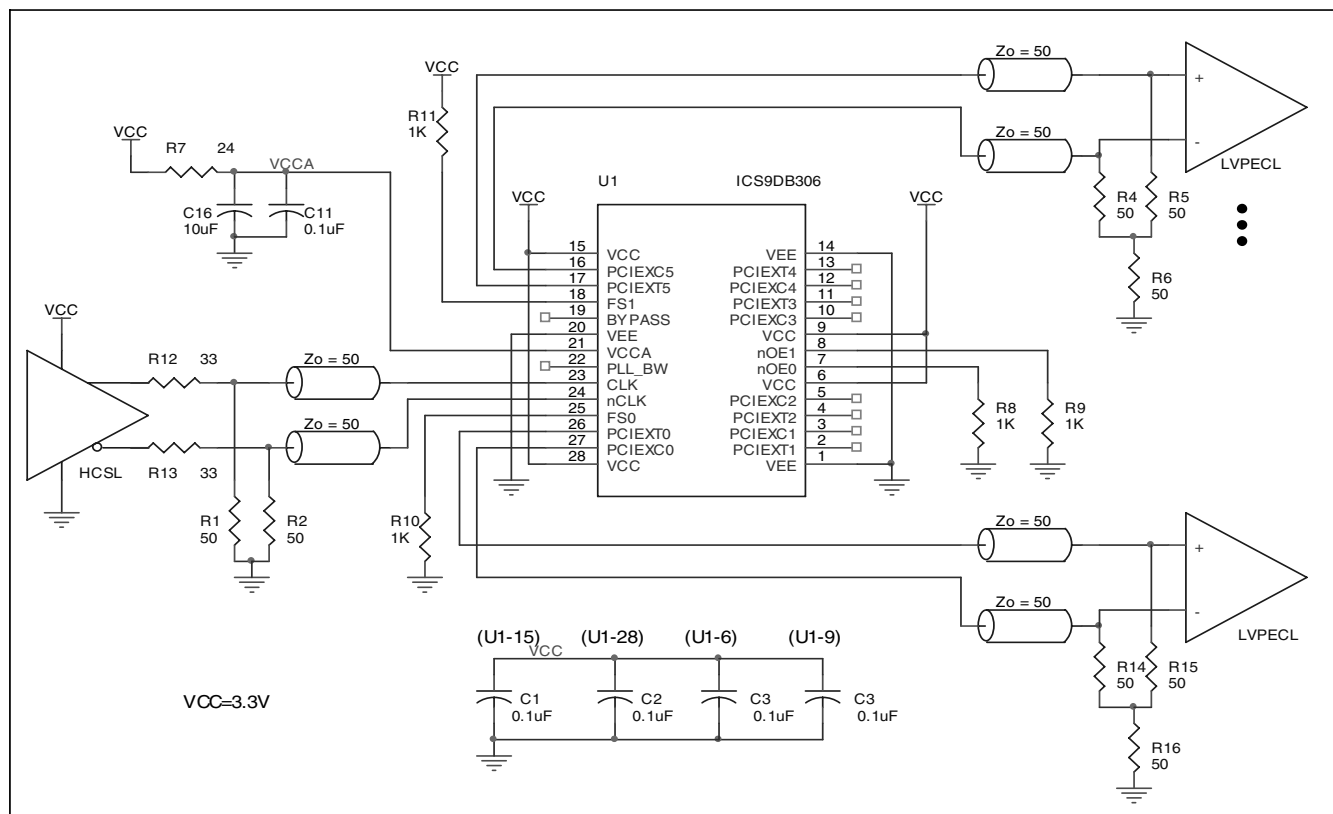


FIGURE 5. EXAMPLE OF ICS9DB306 SCHEMATIC



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS9DB306. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS9DB306 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 135mA = 467.8mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $6 * 30mW = 180mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 467.8mW + 180mW = 647.8mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 43.9°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.648W * 43.9^\circ C/W = 98.4^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 28-PIN TSSOP, FORCED CONVECTION**

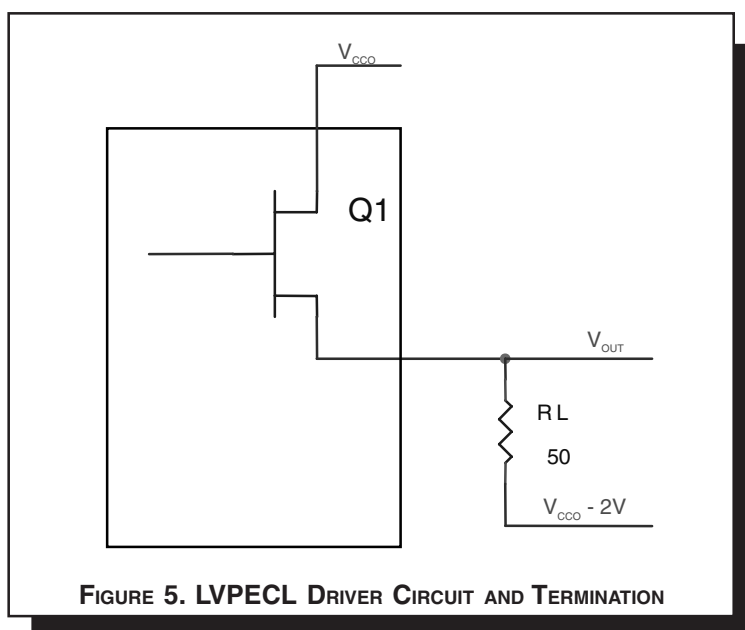
$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	82.9°C/W	68.7°C/W	60.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	49.8°C/W	43.9°C/W	41.2°C/W
<b>NOTE:</b> Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			



### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in Figure 5.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.9V$

$$(V_{CCO\_MAX} - V_{OH\_MAX}) = 0.9V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.7V$

$$(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.7V$$

$Pd\_H$  is power dissipation when the output drives high.  
 $Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = 30mW$



## RELIABILITY INFORMATION

**TABLE 7A.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 28 LEAD TSSOP PACKAGE**

<b><math>\theta_{JA}</math> by Velocity (Linear Feet per Minute)</b>			
	<b>0</b>	<b>200</b>	<b>500</b>
Single-Layer PCB, JEDEC Standard Test Boards	82.9°C/W	68.7°C/W	60.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	49.8°C/W	43.9°C/W	41.2°C/W
<b>NOTE:</b> Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

**TABLE 7B.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 28 LEAD SSOP PACKAGE**

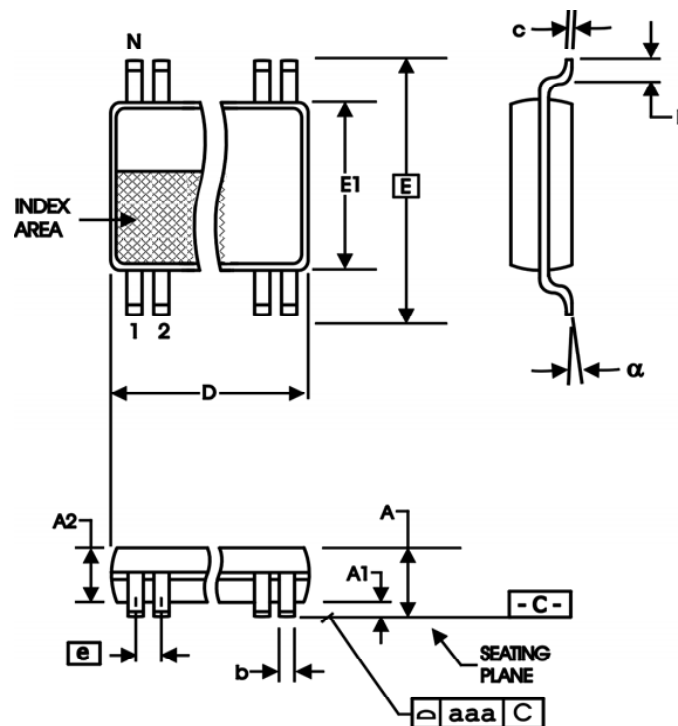
<b><math>\theta_{JA}</math> by Velocity (Linear Feet per Minute)</b>			
	<b>0</b>	<b>200</b>	<b>500</b>
Multi-Layer PCB, JEDEC Standard Test Boards	49°C/W	36°C/W	30°C/W

### TRANSISTOR COUNT

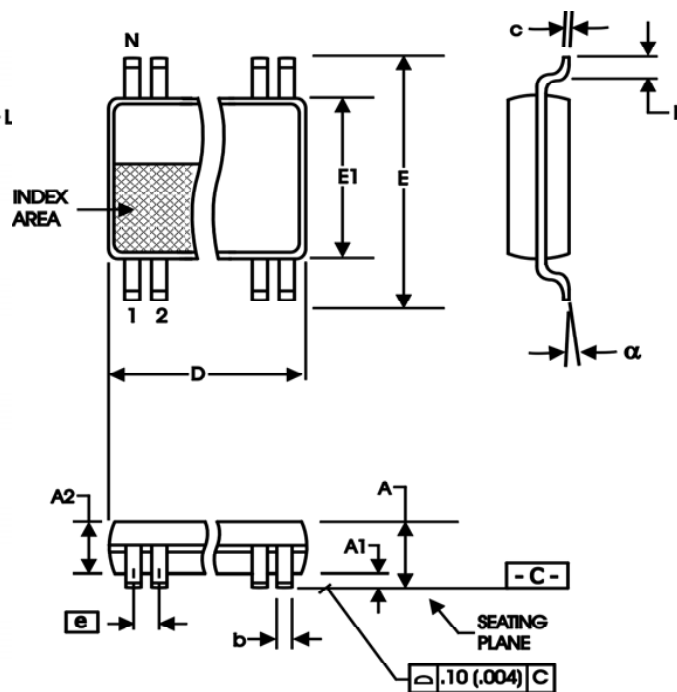
The transistor count for ICS9DB306 is: 2190



**PACKAGE OUTLINE - L SUFFIX FOR 28 LEAD TSSOP**



**PACKAGE OUTLINE - F SUFFIX FOR 28 LEAD SSOP**



**TABLE 8A. PACKAGE DIMENSIONS**

SYMBOL	Millimeters	
	Minimum	Maximum
N	28	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

**TABLE 8B. PACKAGE DIMENSIONS**

SYMBOL	Millimeters	
	Minimum	Maximum
N	28	
A		2.00
A1	0.05	
A2	1.65	1.85
b	0.22	0.38
c	0.09	0.25
D	9.90	10.50
E	7.40	8.20
E1	5.00	5.60
e	0.65 BASIC	
L	0.55	0.95
$\alpha$	0°	8°

Reference Document: JEDEC Publication 95, MO-150



**TABLE 9. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Count	Temperature
ICS9DB306BL	ICS9DB306BL	28 Lead TSSOP	48 per Tube	0°C to 70°C
ICS9DB306BLT	ICS9DB306BL	28 Lead TSSOP on Tape and Reel	1000	0°C to 70°C
ICS9DB306BLLF	ICS9DB306BLLF	28 Lead "Lead-Free" TSSOP	48 per Tube	0°C to 70°C
ICS9DB306BLLFT	ICS9DB306BLLF	28 Lead "Lead-Free" TSSOP on Tape and Reel	1000	0°C to 70°C
ICS9DB306BF	ICS9DB306BF	28 Lead SSOP	46 per Tube	0°C to 70°C
ICS9DB306BFT	ICS9DB306BF	28 Lead SSOP on Tape and Reel	1000	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

The aforementioned trademark, HiPerClockS™ is a trademark of Integrated Circuit Systems, Inc. or its subsidiaries in the United States and/or other countries.

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.



Integrated  
Circuit  
Systems, Inc.

# ICS9DB306

## PCI EXPRESS, JITTER ATTENUATOR

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	3F	2	Added PLL Mode Function Table.	4/7/05