



## 25-Bit Configurable Registered Buffer

### Recommended Application:

- DDR2 Memory Modules
- Provides complete DDR DIMM logic solution with ICS97U877

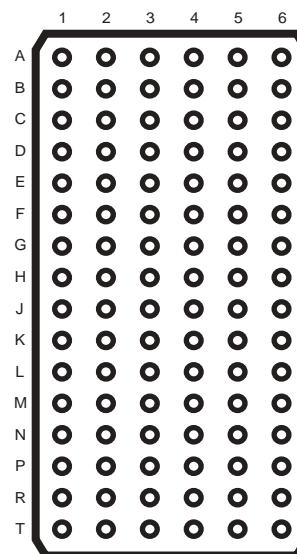
### Product Features:

- 25-bit 1:1 or 14-bit 1:2 configurable registered buffer with parity check functionality
- Supports SSTL\_18 JEDEC specification on data inputs and outputs
- Supports LVCMOS switching levels on CSR# and RESET# inputs
- Low voltage operation  
 $V_{DD} = 1.7V$  to  $1.9V$
- Available in 96 BGA package

### Functionality Truth Table

| Inputs |                  |                  |                  |                  |                      | Outputs |       |               |
|--------|------------------|------------------|------------------|------------------|----------------------|---------|-------|---------------|
| RST#   | DCS#             | CSR#             | CK               | CK#              | Dn,<br>DODT,<br>DCKE | Qn      | QCS#  | QODT,<br>QCKE |
| H      | L                | L                | ↑                | ↓                | L                    | L       | L     | L             |
| H      | L                | L                | ↑                | ↓                | H                    | H       | L     | H             |
| H      | L                | L                | L or H           | L or H           | X                    | $Q_0$   | $Q_0$ | $Q_0$         |
| H      | L                | H                | ↑                | ↓                | L                    | L       | L     | L             |
| H      | L                | H                | ↑                | ↓                | H                    | H       | L     | H             |
| H      | L                | H                | L or H           | L or H           | X                    | $Q_0$   | $Q_0$ | $Q_0$         |
| H      | H                | L                | ↑                | ↓                | L                    | L       | H     | L             |
| H      | H                | L                | ↑                | ↓                | H                    | H       | H     | H             |
| H      | H                | L                | L or H           | L or H           | X                    | $Q_0$   | $Q_0$ | $Q_0$         |
| H      | H                | H                | ↑                | ↓                | L                    | $Q_0$   | H     | L             |
| H      | H                | H                | ↑                | ↓                | H                    | $Q_0$   | H     | H             |
| H      | H                | H                | L or H           | L or H           | X                    | $Q_0$   | $Q_0$ | $Q_0$         |
| L      | X or<br>Floating | X or<br>Floating | X or<br>Floating | X or<br>Floating | X or<br>Floating     | L       | L     | L             |

### Pin Configuration



96 Ball BGA  
(Top View)



## Ball Assignments

### 25 bit 1:1 Register

|   |        |       |                  |                 |      |     |
|---|--------|-------|------------------|-----------------|------|-----|
| A | DCKE   | PPO   | V <sub>REF</sub> | V <sub>DD</sub> | QCKE | NC  |
| B | D2     | D15   | GND              | GND             | Q2   | Q15 |
| C | D3     | D16   | V <sub>DD</sub>  | V <sub>DD</sub> | Q3   | Q16 |
| D | DODT   | QERR# | GND              | GND             | QODT | NC  |
| E | D5     | D17   | V <sub>DD</sub>  | V <sub>DD</sub> | Q5   | Q17 |
| F | D6     | D18   | GND              | GND             | Q6   | Q18 |
| G | PAR_IN | RST#  | V <sub>DD</sub>  | V <sub>DD</sub> | C1   | C0  |
| H | CK     | DCS#  | GND              | GND             | QCS# | NC  |
| J | CK#    | CSR#  | V <sub>DD</sub>  | V <sub>DD</sub> | ZOH  | ZOL |
| K | D8     | D19   | GND              | GND             | Q8   | Q19 |
| L | D9     | D20   | V <sub>DD</sub>  | V <sub>DD</sub> | Q9   | Q20 |
| M | D10    | D21   | GND              | GND             | Q10  | Q21 |
| N | D11    | D22   | V <sub>DD</sub>  | V <sub>DD</sub> | Q11  | Q22 |
| P | D12    | D23   | GND              | GND             | Q12  | Q23 |
| R | D13    | D24   | V <sub>DD</sub>  | V <sub>DD</sub> | Q13  | Q24 |
| T | D14    | D25   | V <sub>REF</sub> | V <sub>DD</sub> | Q14  | Q25 |

1 2 3 4 5 6  
**C0 = 0, C1 = 0**

### 14 bit 1:2 Registers

|   |        |       |                  |                 |       |       |
|---|--------|-------|------------------|-----------------|-------|-------|
| A | DCKE   | PPO   | V <sub>REF</sub> | V <sub>DD</sub> | QCKEA | QCKEB |
| B | D2     | NC    | GND              | GND             | Q2A   | Q2B   |
| C | D3     | NC    | V <sub>DD</sub>  | V <sub>DD</sub> | Q3A   | Q3B   |
| D | DODT   | QERR# | GND              | GND             | QODTA | QODTB |
| E | D5     | NC    | V <sub>DD</sub>  | V <sub>DD</sub> | Q5A   | Q5B   |
| F | D6     | NC    | GND              | GND             | Q6A   | Q6B   |
| G | PAR_IN | RST#  | V <sub>DD</sub>  | V <sub>DD</sub> | C1    | C0    |
| H | CK     | DCS#  | GND              | GND             | QCSA# | QCSB# |
| J | CK#    | CSR#  | V <sub>DD</sub>  | V <sub>DD</sub> | ZOH   | ZOL   |
| K | D8     | NC    | GND              | GND             | Q8A   | Q8B   |
| L | D9     | NC    | V <sub>DD</sub>  | V <sub>DD</sub> | Q9A   | Q9B   |
| M | D10    | NC    | GND              | GND             | Q10A  | Q10B  |
| N | D11    | NC    | V <sub>DD</sub>  | V <sub>DD</sub> | Q11A  | Q11B  |
| P | D12    | NC    | GND              | GND             | Q12A  | Q12B  |
| R | D13    | NC    | V <sub>DD</sub>  | V <sub>DD</sub> | Q13A  | Q13B  |
| T | D14    | NC    | V <sub>REF</sub> | V <sub>DD</sub> | Q14A  | Q14B  |

1 2 3 4 5 6  
**Register A (C0 = 0, C1 = 1)**

|   |        |       |                  |                 |       |       |
|---|--------|-------|------------------|-----------------|-------|-------|
| A | D1     | PPO   | V <sub>REF</sub> | V <sub>DD</sub> | Q1A   | Q1B   |
| B | D2     | NC    | GND              | GND             | Q2A   | Q2B   |
| C | D3     | NC    | V <sub>DD</sub>  | V <sub>DD</sub> | Q3A   | Q3B   |
| D | D4     | QERR# | GND              | GND             | Q4A   | Q4B   |
| E | D5     | NC    | V <sub>DD</sub>  | V <sub>DD</sub> | Q5A   | Q5B   |
| F | D6     | NC    | GND              | GND             | Q6A   | Q6B   |
| G | PAR_IN | RST#  | V <sub>DD</sub>  | V <sub>DD</sub> | C1    | C0    |
| H | CK     | DCS#  | GND              | GND             | QCSA# | QCSB# |
| J | CK#    | CSR#  | V <sub>DD</sub>  | V <sub>DD</sub> | ZOH   | ZOL   |
| K | D8     | NC    | GND              | GND             | Q8A   | Q8B   |
| L | D9     | NC    | V <sub>DD</sub>  | V <sub>DD</sub> | Q9A   | Q9B   |
| M | D10    | NC    | GND              | GND             | Q10A  | Q10B  |
| N | DODT   | NC    | V <sub>DD</sub>  | V <sub>DD</sub> | QODTA | QODTB |
| P | D12    | NC    | GND              | GND             | Q12A  | Q12B  |
| R | D13    | NC    | V <sub>DD</sub>  | V <sub>DD</sub> | Q13A  | Q13B  |
| T | DCKE   | NC    | V <sub>REF</sub> | V <sub>DD</sub> | QCKEA | QCKEB |

1 2 3 4 5 6  
**Register B (C0 = 1, C1 = 1)**



### General Description

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V VDD operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL\_18. The control inputs are LVCMOS. All outputs are 1.8-V CMOS drivers that have been optimized to drive the DDR-II DIMM load. **ICSSSTU32866** operates from a differential clock (CK and CK#). Data are registered at the crossing of CK going high, and CK# going low.

The C0 input controls the pinout configuration of the 1:2 pinout from A configuration (when low) to B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high).

#### A - Pair Configuration (CO<sub>1</sub> = 0, CI<sub>1</sub> = 1 and CO<sub>2</sub> = 0, CI<sub>2</sub> = 1)

Parity that arrives one cycle after the data input to which it applies is checked on the PAR\_IN of the first register. The second register produces to PPO and QERR# signals. The QERR# of the first register is left floating. The valid error information is latched on the QERR# output of the second register. If an error occurs QERR# is latched low for two cycles or until Reset# is low.

#### B - Single Configuration (CO = 0, C1 = 0)

The device supports low-power standby operation. When the reset input (RST#) is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (VREF) inputs are allowed. In addition, when RST# is low all registers are reset, and all outputs are forced low. The LVCMOS RST# and Cn inputs must always be held at a valid logic high or low level. To ensure defined outputs from the register before a stable clock has been supplied, RST# must be held in the low state during power up.

In the DDR-II RDIMM application, RST# is specified to be completely asynchronous with respect to CK and CK#. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of RST# until the input receivers are fully enabled, the design of the **ICSSSTU32866** must ensure that the outputs will remain low, thus ensuring no glitches on the output.

The device monitors both DCS# and CSR# inputs and will gate the Qn outputs from changing states when both DCS# and CSR# inputs are high. If either DCS# or CSR# input is low, the Qn outputs will function normally. The RST input has priority over the DCS# and CSR# control and will force the outputs low. If the DCS#-control functionality is not desired, then the CSR# input can be hardwired to ground, in which case, the setup-time requirement for DCS# would be the same as for the other D data inputs. Package options include 96-ball LFBGA (MO-205CC).

**Parity and Standby Functionality Truth Table**

| Inputs |                  |                  |                  |                  |                                 |                  | Outputs          |                     |
|--------|------------------|------------------|------------------|------------------|---------------------------------|------------------|------------------|---------------------|
| Reset# | DCS#             | CSR#             | CK               | CK#              | Sum of Inputs = H<br>(D1 - D25) | PAR_IN           | PPO              | QERR#               |
| H      | L                | X                | ↑                | ↓                | Even                            | L                | L                | H                   |
| H      | L                | X                | ↑                | ↓                | Odd                             | L                | H                | L                   |
| H      | L                | X                | ↑                | ↓                | Even                            | H                | H                | L                   |
| H      | L                | X                | ↑                | ↓                | Odd                             | H                | L                | H                   |
| H      | H                | L                | ↑                | ↓                | Even                            | L                | L                | H                   |
| H      | H                | L                | ↑                | ↓                | Odd                             | H                | H                | L                   |
| H      | H                | H                | ↑                | ↓                | X                               | X                | PPO <sub>0</sub> | QERR <sub>0</sub> # |
| H      | X                | X                | L or H           | L or H           | X                               | X                | PPO <sub>0</sub> | QERR <sub>0</sub> # |
| L      | X or<br>Floating | X or<br>Floating | X or<br>Floating | X or<br>Floating | X or Floating                   | X or<br>Floating | L                | H                   |

1. CO = 0 and CI = 0, Data inputs are D2, D3, D5, D6, D8 - D25.

CO = 0 and CI = 1, Data inputs are D2, D3, D5, D6, D8 - D14

CO = 1 and CI = 1, Data inputs are D1 - D6, D8 - D10, D12, D13

2. PAR\_IN arrives one clock cycle after the data to which it applies when CO = 0.

3. PAR\_IN arrives two clock cycles after the data to which it applies when CO = 1.

4. Assume QERR# is high at the CK↑ and CK#↓ crossing. If QERR# is low it stays latched low for two clock cycles on until Reset# is low.

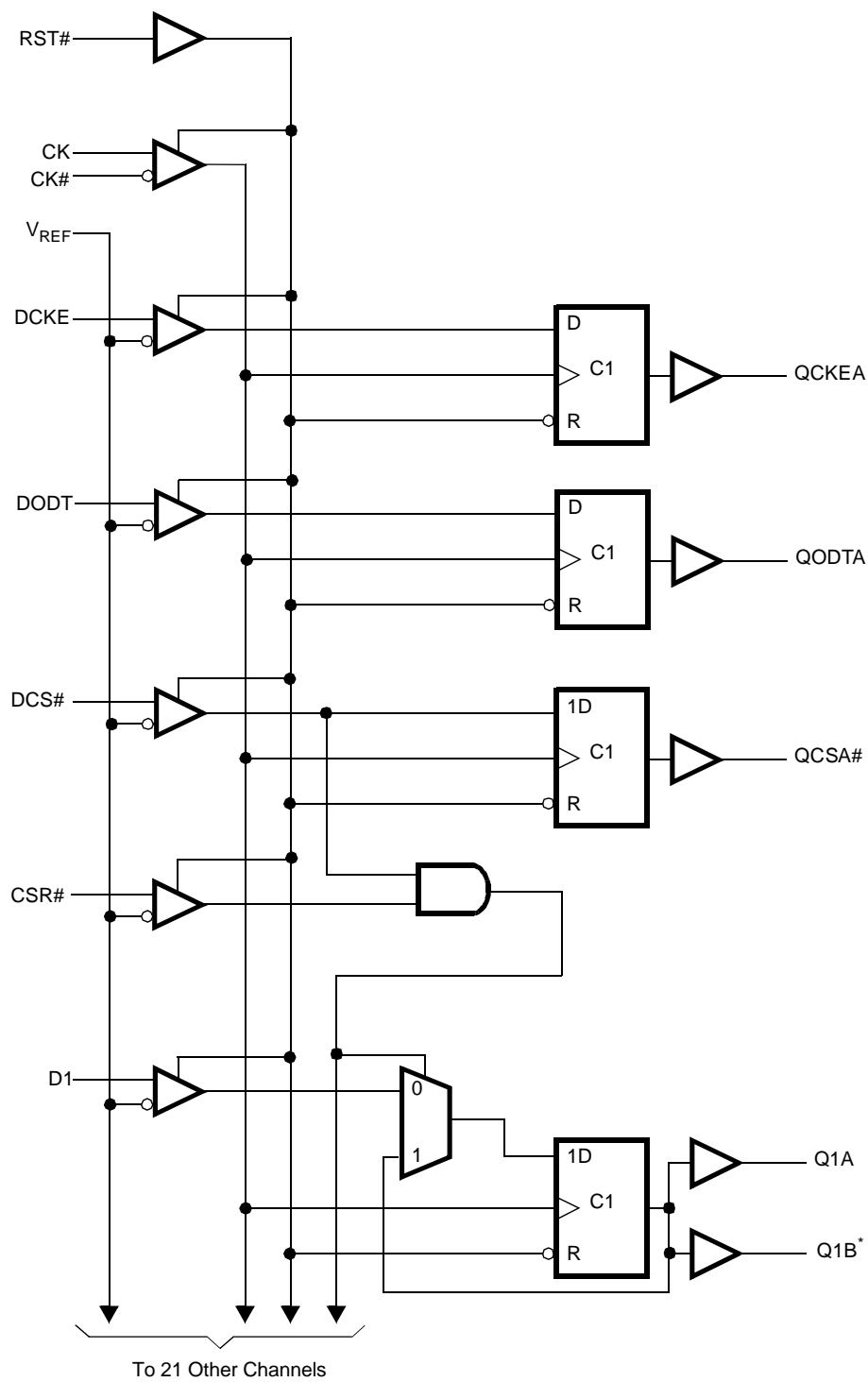


### Ball Assignment

| Terminal Name    | Description   | Electrical Characteristics |
|------------------|---|----------------------------|
| GND              | Ground  | Ground input               |
| V <sub>DD</sub>  | Power supply voltage  | 1.8V nominal               |
| V <sub>REF</sub> | Input reference voltage   | 0.9V nominal               |
| Z <sub>OH</sub>  | Reserved for future use   | Input                      |
| Z <sub>OL</sub>  | Reserved for future use   | Input                      |
| CK               | Positive master clock input   | Differential input         |
| CK               | Negative master clock input   | Differential input         |
| C0, C1           | Configuration control inputs  | LVC MOS inputs             |
| RST#             | Asynchronous reset input - resets registers and disables V <sub>REF</sub> data and clock differential-input receivers | LVC MOS input              |
| CSR#, DCS#       | Chip select inputs - disables D1 - D24 outputs switching when both inputs are high                                    | SSTL_18 input              |
| D1 - D25         | Data input - clock in on the crossing of the rising edge of CK and the falling edge of CK#                            | SSTL_18 input              |
| DODT             | The outputs of this register bit will not be suspended by the DCS# and CSR# control                                   | SSTL_18 input              |
| DCKE             | The outputs of this register bit will now be suspended by the DCS# and CSR# control                                   | SSTL_18 input              |
| Q1 - Q25         | Data outputs that are suspended by the DCS# and CSR# control  | 1.8V CMOS                  |
| QCS#             | Data output that will not be suspended by the DCS# and CSR# control   | 1.8V CMOS                  |
| QODT             | Data output that will not be suspended by the DCS# and CSR# control   | 1.8V CMOS                  |
| QCKE             | Data output that will not be suspended by the DCS# and CSR# control   | 1.8V CMOS                  |
| PPO              | Partial parity out indicates off parity of inputs D1 - D25.   | 1.8V CMOS                  |
| PAR_IN           | Parity input arrives one clock cycle after the corresponding data input   | SSTL_18 input              |
| QERR#            | Output error bit-generated one clock cycle after the corresponding data output  | Open drain output          |



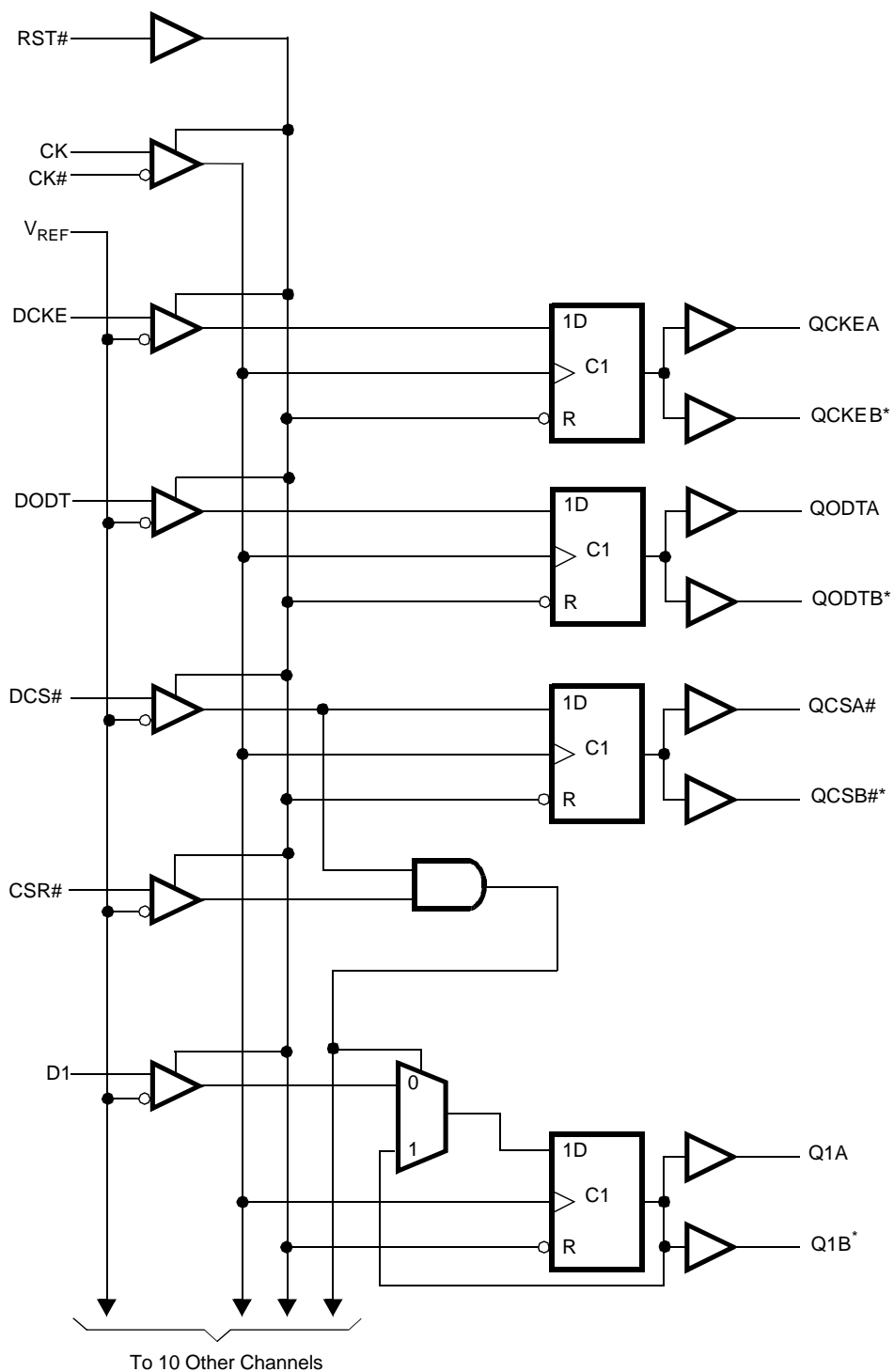
### Block Diagram for 1:1 mode (positive logic)



\*Note: Disabled in 1:1 configuration



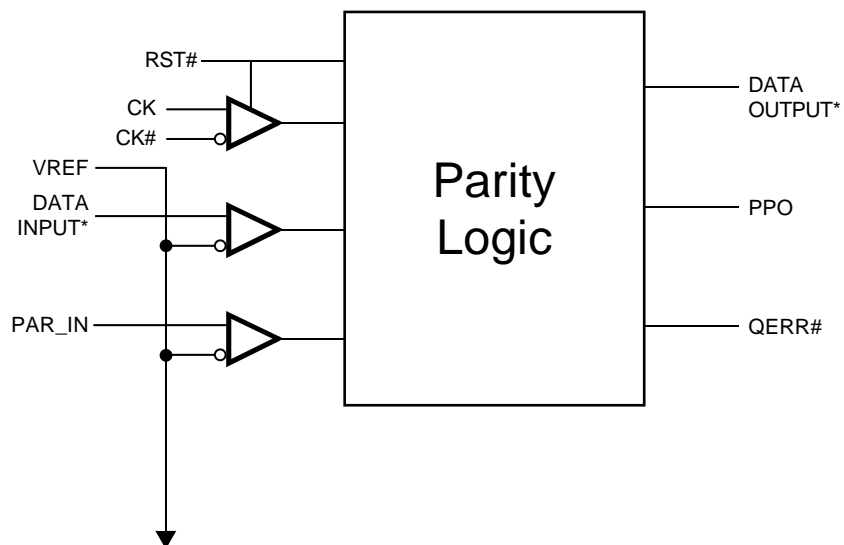
### Block Diagram for 1:2 mode (positive logic)



\*Note: Disabled in 1:1 configuration



## Parity Functionality Block Diagram



### \* Register Configurations

| DATA INPUT:                    | DATA OUTPUT:                   | CO | CI |
|--------------------------------|--------------------------------|----|----|
| D2, D3, D5, D6,<br>D8 - D25    | D2, D3, D5, D6,<br>D8 - D25    | 0  | 0  |
| D2, D3, D5, D6,<br>D8 - D14    | D2, D3, D5, D6,<br>D8 - D14    | 0  | 1  |
| D1 - D6, D8 -<br>D10, D12, D13 | D1 - D6, D8 -<br>D10, D12, D13 | 1  | 1  |



### Absolute Maximum Ratings

|  |                    |
|--|--------------------|
| Storage Temperature                    | -65°C to +150°C    |
| Supply Voltage                         | -0.5 to 2.5V       |
| Input Voltage <sup>1</sup>             | -0.5 to VDD + 2.5V |
| Output Voltage <sup>1,2</sup>          | -0.5 to VDDQ + 0.5 |
| Input Clamp Current                    | ±50 mA             |
| Output Clamp Current                   | ±50mA              |
| Continuous Output Current              | ±50mA              |
| VDDQ or GND Current/Pin                | ±100mA             |
| Package Thermal Impedance <sup>3</sup> | 36°C               |

#### Notes:

1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This current will flow only when the output is in the high state level  $V_O > V_{DDQ}$ .
3. The package thermal impedance is calculated in accordance with JESD 51.

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Recommended Operating Conditions

| PARAMETER            | DESCRIPTION                    |                   | MIN                      | TYP                   | MAX                      | UNITS |
|----------------------|--------------------------------|-------------------|--------------------------|-----------------------|--------------------------|-------|
| V <sub>DDQ</sub>     | I/O Supply Voltage             |                   | 1.7                      | 1.8                   | 1.9                      | V     |
| V <sub>REF</sub>     | Reference Voltage              |                   | 0.49 x V <sub>DD</sub>   | 0.5 x V <sub>DD</sub> | 0.51 x V <sub>DD</sub>   |       |
| V <sub>TT</sub>      | Termination Voltage            |                   | V <sub>REF</sub> - 0.04  | V <sub>REF</sub>      | V <sub>REF</sub> + 0.04  |       |
| V <sub>I</sub>       | Input Voltage                  |                   | 0                        |                       | V <sub>DDQ</sub>         |       |
| V <sub>IH</sub> (DC) | DC Input High Voltage          | Data Inputs       | V <sub>REF</sub> + 0.125 |                       |                          |       |
| V <sub>IH</sub> (AC) | AC Input High Voltage          |                   | V <sub>REF</sub> + 0.250 |                       |                          |       |
| V <sub>IL</sub> (DC) | DC Input Low Voltage           |                   |                          |                       | V <sub>REF</sub> - 0.125 |       |
| V <sub>IL</sub> (DC) | AC Input Low Voltage           |                   | V <sub>REF</sub> + 0.250 |                       |                          |       |
| V <sub>IH</sub>      | Input High Voltage Level       | RESET#,<br>C0, C1 | 0.65 x V <sub>DDQ</sub>  |                       |                          |       |
| V <sub>IL</sub>      | Input Low Voltage Level        |                   |                          |                       | 0.35 x V <sub>DDQ</sub>  |       |
| V <sub>ICR</sub>     | Common mode Input Range        | CLK, CLK#         | 0.675                    |                       | 1.125                    |       |
| V <sub>ID</sub>      | Differential Input Voltage     |                   | 0.600                    |                       |                          |       |
| I <sub>OH</sub>      | High-Level Output Current      |                   |                          |                       | -8                       | mA    |
| I <sub>OL</sub>      | Low-Level Output Current       |                   |                          |                       | 8                        |       |
| T <sub>A</sub>       | Operating Free-Air Temperature |                   | 0                        |                       | 70                       | °C    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

Note: Reset# and Cn inputs must be held at valid logic levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless Reset# is low.





## Electrical Characteristics - DC

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 2.5 \pm 0.2\text{V}$ ,  $V_{DDQ} = 2.5 \pm 0.2\text{V}$ ; (unless otherwise stated)

| SYMBOL     | PARAMETERS                                 | CONDITIONS   | $V_{DDQ}$   | MIN             | TYP | MAX     | UNITS                                  |
|------------|--|--|-------------|-----------------|-----|---------|--|
| $V_{IK}$   |  | $I_I = -18\text{mA}$   |             |                 |     | -1.2    | V                                      |
| $V_{OH}$   |  | $I_{OH} = -100\mu\text{A}$   | 1.7V - 1.9V | $V_{DDQ} - 0.2$ |     |         |  |
|            |  | $I_{OH} = -16\text{mA}$  | 1.7V        | 1.95            |     |         |  |
| $V_{OL}$   |  | $I_{OL} = 100\mu\text{A}$  | 1.7V - 1.9V |                 |     | 0.2     |  |
|            |  | $I_{OL} = 16\text{mA}$   | 1.7V        |                 |     | 0.35    |  |
| $I_I$      | All Inputs                                 | $V_I = V_{DD}$ or GND  | 1.9V        |                 |     | $\pm 5$ | $\mu\text{A}$                          |
| $I_{DD}$   | Standby (Static)                           | RESET# = GND   | 1.9V        |                 |     | 0.01    | $\mu\text{A}$                          |
|            | Operating (Static)                         | $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ ,<br>RESET# = $V_{DD}$  |             |                 | TBD |         | mA                                     |
| $I_{DDD}$  | Dynamic operating<br>(clock only)          | RESET# = $V_{DD}$ ,<br>$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ ,<br>CLK and CLK# switching<br>50% duty cycle.   | 1.8V        |                 | TBD |         | $\mu/\text{clock}$<br>MHz              |
|            | Dynamic Operating<br>(per each data input) | RESET# = $V_{DD}$ ,<br>$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ ,<br>CLK and CLK# switching<br>50% duty cycle. One data<br>input switching at half<br>clock frequency, 50%<br>duty cycle |             |                 | TBD |         | $\mu\text{A}/\text{clock}$<br>MHz/data |
| $r_{OH}$   | Output High                                | $I_{OH} = -20\text{mA}$  |             |                 |     |         | $\Omega$                               |
| $r_{OL}$   | Output Low                                 | $I_{OL} = 20\text{mA}$   |             |                 |     |         | $\Omega$                               |
| $r_{O(D)}$ | [ $r_{OH} - r_{OL}$ ] each<br>separate bit | $I_O = 20\text{mA}$ , $T_A = 25^\circ\text{C}$   |             |                 |     | 4       | $\Omega$                               |
| $C_i$      | Data Inputs                                | $V_I = V_{REF} \pm 350\text{mV}$   |             | 2.5             |     | 3.5     | pF                                     |
|            | CLK and CLK#                               | $V_{ICR} = 1.25\text{V}$ , $V_{I(PP)} = 360\text{mV}$  |             | 2               |     | 3       |  |
|            | RESET#                                     | $V_I = V_{DDQ}$ or GND   |             |                 | 2.5 |         |  |

Notes:

1 - Guaranteed by design, not 100% tested in production.

## Output Buffer Characteristics

Output edge rates over recommended operating free-air temperature range (See figure 7)

| PARAMETER          | $V_{DD} = 1.8\text{V} \pm 0.1\text{V}$ |     | UNIT |
|--------------------|--|-----|------|
|                    | MIN                                    | MAX |      |
| $dV/dt_r$          | 1                                      | 4   | V/ns |
| $dV/dt_f$          | 1                                      | 4   | V/ns |
| $dV/dt_{\Delta}^1$ |  | 1   | V/ns |

1. Difference between  $dV/dt_r$  (rising edge rate) and  $dV/dt_f$  (falling edge rate)



### Timing Requirements

(over recommended operating free-air temperature range, unless otherwise noted)

| SYMBOL             | PARAMETERS      |  | V <sub>DD</sub> = 1.8V ±0.1V |     | UNITS |
|--------------------|-----------------|--|------------------------------|-----|-------|
|                    |                 |  | MIN                          | MAX |       |
| f <sub>clock</sub> | Clock frequency |  |                              | 300 | MHz   |
| t <sub>s</sub>     | Setup time      | Data before CLK↑, CLK#↓                | 0.75                         |     | ns    |
|                    |                 |  | 0.9                          |     |       |
|                    |                 | DCS# before CK↑, CK#↓, CSR# high       | 0.7                          |     |       |
|                    |                 | CSR# before CK↑, CK#↓, DCS# high       | 0.7                          |     |       |
|                    |                 | DCS# before CK↑, CK#↓, CSR# low        | 0.5                          |     |       |
|                    |                 | DODT, DCKE and Q before CK↑, CK#↓      | 0.5                          |     |       |
| t <sub>H</sub>     | Hold time       | DCS#, DODT, DCKE and Q after CK↑, CK#↓ | 0.50                         |     | ns    |
|                    | Hold time       | PAR_IN after CK↑, CK#↓                 | 0.50                         |     | ns    |

- Notes:**
- 1 - Guaranteed by design, not 100% tested in production.
  - 2 - For data signal input slew rate of 1V/ns.
  - 3 - For data signal input slew rate of 0.5V/ns and < 1V/ns.
  - 4 - CLK/CLK# signal input slew rate of 1V/ns.

### Switching Characteristics

(over recommended operating free-air temperature range, unless otherwise noted)

| Symbol             | Parameter                                | Measurement Conditions | MIN  | MAX  | Units |
|--------------------|--|------------------------|------|------|-------|
| f <sub>max</sub>   | Max input clock frequency                |                        | 270  |      | MHz   |
| t <sub>PDM</sub>   | Propagation delay, single bit switching  | CK↑ to CK#↓ QN         | 1.41 | 215  | ns    |
| t <sub>PD</sub>    | Propagation delay                        | CK↑ to CK#↓ to PPO     | 0.5  | 1.8  | ns    |
| t <sub>LH</sub>    | Low to High propagation delay            | CK↑ to CK#↓ to QERR#   | 1.2  | 3    | ns    |
| t <sub>HL</sub>    | High to low propagation delay            | CK↑ to CK#↓ to QERR#   | 1    | 2.4  | ns    |
| t <sub>PDMSS</sub> | Propagation delay simultaneous switching | CK↑ to CK#↓ QN         |      | 2.35 | ns    |
| t <sub>PHL</sub>   | High to low propagation delay            | Reset# ↓ to QN↓        |      | 3    | ns    |
| t <sub>PHL</sub>   | High to low propagation delay            | Reset# ↓ to PPO↓       |      | 3    | ns    |
| t <sub>PLH</sub>   | Low to High propagation delay            | Reset# ↓ to QERR#↑     |      | 3    | ns    |

2. Guaranteed by design, not 100% tested in production.

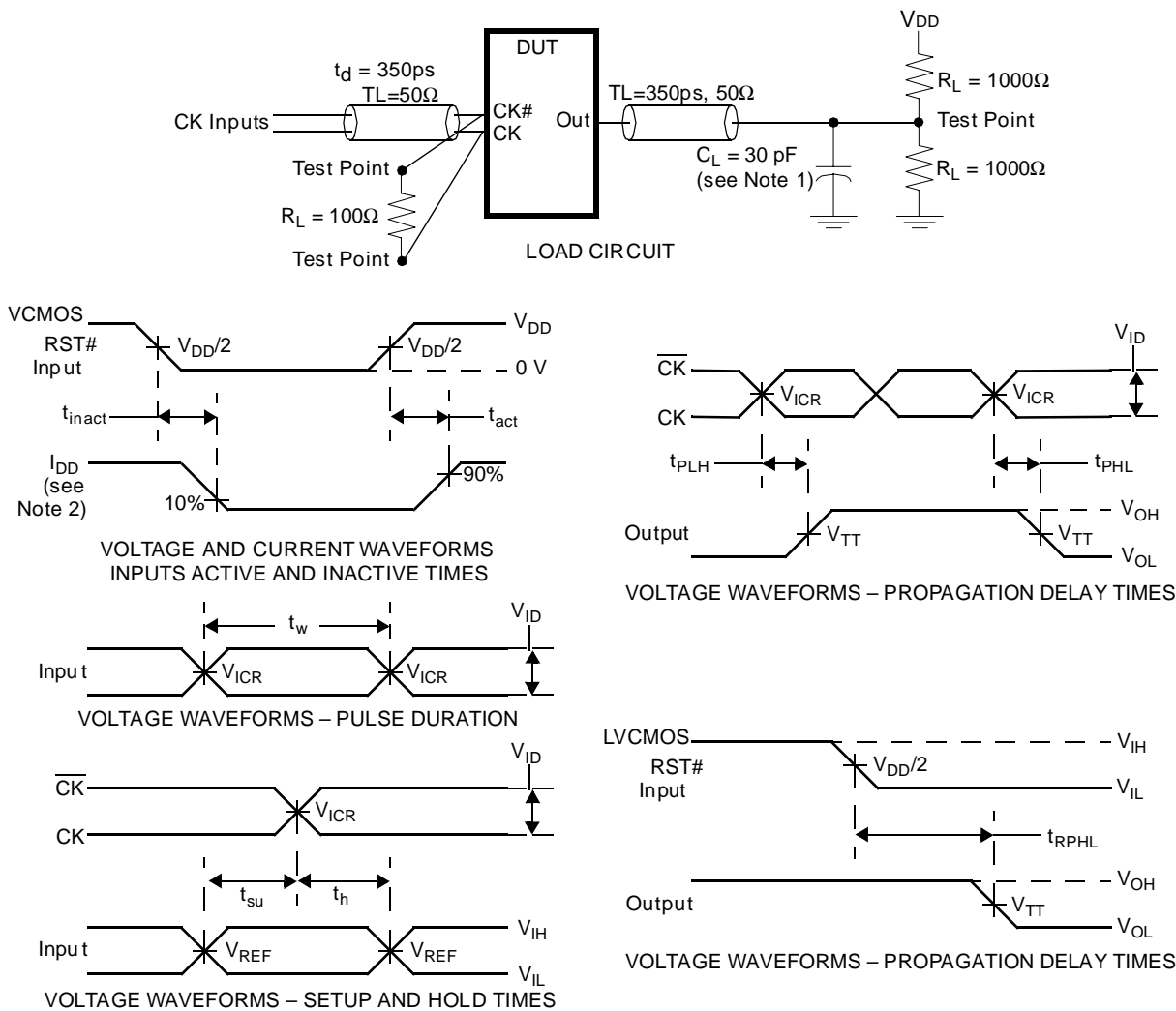
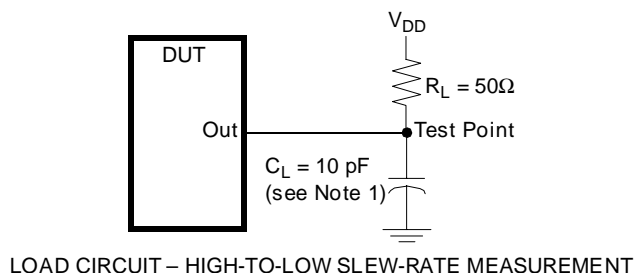
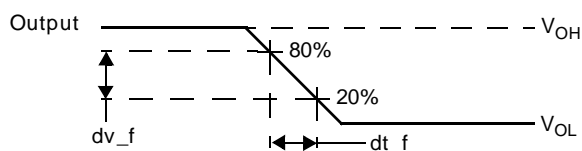


Figure 6— Parameter Measurement Information ( $V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$ )

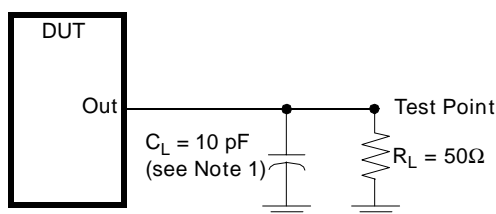
- Notes:
1.  $C_L$  includes probe and jig capacitance.
  2.  $I_{DD}$  tested with clock and data inputs held at  $V_{DD}$  or GND, and  $I_o = 0\text{mA}$ .
  3. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_o = 50\Omega$ , input slew rate =  $1\text{ V/ns} \pm 20\%$  (unless otherwise specified).
  4. The outputs are measured one at a time with one transition per measurement.
  5.  $V_{REF} = V_{DD}/2$
  6.  $V_{IH} = V_{REF} + 250\text{ mV}$  (ac voltage levels) for differential inputs.  $V_{IH} = V_{DD}$  for LVCMOS input.
  7.  $V_{IL} = V_{REF} - 250\text{ mV}$  (ac voltage levels) for differential inputs.  $V_{IL} = \text{GND}$  for LVCMOS input.
  8.  $V_{ID} = 600\text{ mV}$
  9.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PDM}$ .



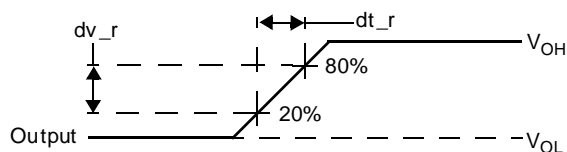
LOAD CIRCUIT – HIGH-TO-LOW SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS – HIGH-TO-LOW SLEW-RATE MEASUREMENT



LOAD CIRCUIT – LOW-TO-HIGH SLEW-RATE MEASUREMENT

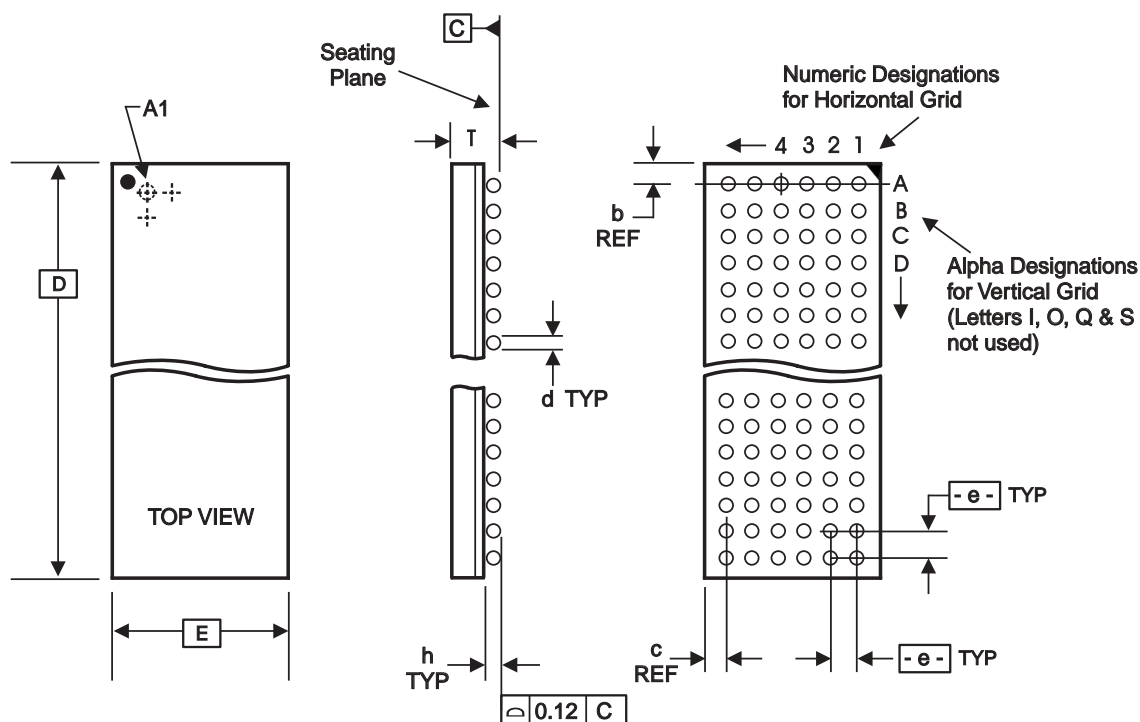


VOLTAGE WAVEFORMS – LOW-TO-HIGH SLEW-RATE MEASUREMENT

Figure 7 — Output Slew-Rate Measurement Information ( $V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$ )

Notes: 1.  $C_L$  includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{MHz}$ ,  $Z_O = 50\Omega$ , input slew rate =  $1 \text{ V/ns} \pm 20\%$  (unless otherwise specified).



ALL DIMENSIONS IN MILLIMETERS

| D         | E        | T         | e        | ----- BALL GRID ----- |      | Max.<br>TOTAL | d         | h         | REF. DIMENSIONS |       |
|-----------|----------|-----------|----------|-----------------------|------|---------------|-----------|-----------|-----------------|-------|
|           |          |           |          | HORIZ                 | VERT |               |           |           | b               | c     |
|           |          | Min/Max   |          |                       |      |               | Min/Max   | Min/Max   |                 |       |
| 16.00 Bsc | 5.50 Bsc | 1.30/1.50 | 0.80 Bsc | 6                     | 19   | 114           | 0.40/0.50 | 0.31/0.41 | 0.80            | 0.75  |
| 13.50 Bsc | 5.50 Bsc | 1.30/1.50 | 0.80 Bsc | 6                     | 16   | 96            | 0.40/0.50 | 0.25/0.41 | 0.75            | 0.75  |
| 7.00 Bsc  | 4.50 Bsc | 0.86/1.00 | 0.65 Bsc | 6                     | 10   | 60            | 0.35/0.45 | 0.15/0.21 | 0.575           | 0.625 |

Note: Ball grid total indicates maximum ball count for package. Lesser quantity may be used.

\* Source Ref.: JEDEC Publication 95, MO-205

10-0055C

## Ordering Information

ICSSSTU32866yHT

Example:

ICS XXXX y H - T

Designation for tape and reel packaging

Package Type

H = BGA

Revision Designator (will not correlate with datasheet revision)

Device Type

Prefix

ICS = Standard Device