



# MK3754

## LOW COST 54 MHz 3.3 VOLT VCXO

### Description

The MK3754D and MK3754B are drop-in replacements for the MK3754S device. Compared to these earlier devices the MK3754D and MK3754B offer a wider operating frequency range and improved power supply noise rejection.

The MK3754 is ICS' lowest cost, low jitter, high performance 3.3 Volt VCXO and PLL clock synthesizer designed to replace expensive 54 MHz VCXOs. The on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3.3 V input voltage to vary the output clocks by  $\pm 100$  ppm. Using ICS' patented VCXO and analog/digital Phase-Locked Loop (PLL) techniques, the device uses an inexpensive external 13.5 MHz pullable crystal input to produce a 54 MHz output clock.

The MK3754D exhibits a moderate VCXO gain of 120ppm/V typical, when used with a high quality external pullable quartz crystal. The MK3754B offers a higher VCXO gain of 150ppm/V. The higher intrinsic VCXO gain of the MK3754B may help compensate for the reduced pullability of a low quality crystal used in some applications. However, higher VCXO gain may also increase clock output phase noise.

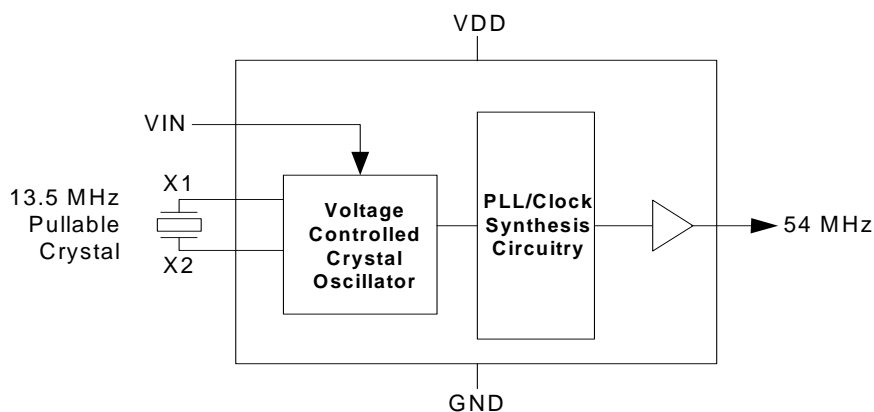
The frequency of the on-chip VCXO is adjusted by an external control voltage input into pin VIN. Because VIN is a high impedance input, it can be driven directly from an PWM RC integrator circuit. Frequency output increases with VIN voltage input. The usable range of VIN is 0 to 3V.

### Features

- MK3754D and MK3754B are drop-in upgrades to the earlier MK3754S device
- Packaged in 8 pin SOIC
- Operating voltage of 3.3 V
- Uses an inexpensive 13.500 MHz external crystal
- On-chip VCXO (patented) with pull range of 200ppm (minimum)
- VCXO turning voltage of 0 to 3.3V
- 12mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process

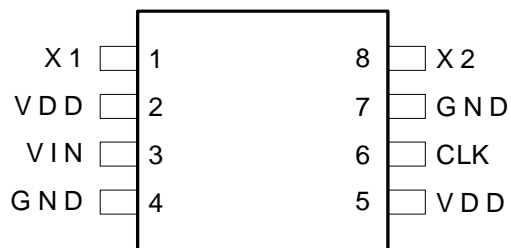
**MK3754D is Recommended for New Designs.**

### Block Diagram





## Pin Assignment



**MK3754S**  
**MK3754B**  
**MK3754D**

**8 Pin (150 mil) SOIC**

## Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	XI	Input	Crystal connection. Connect to the external pullable crystal.
2	VDD	Power	Connect to +3.3 V (0.01uf decoupling capacitor recommended).
3	VIN	Input	Voltage input to VCXO -- 0 to 3.3 V analog input which controls the oscillation frequency of the VCXO.
4	GND	Power	Connect to ground.
5	VDD	Power	Connect to +3.3 V (0.01uf decoupling capacitor recommended).
6	CLK	Output	54 MHz clock output.
7	GND	Power	Connect to ground.
8	X2	Input	Crystal connection. Connect to the external pullable crystal.



## External Component Selection

The MK3754 requires a minimum number of external components for proper operation.

### Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD (pin 2) and GND (pin 4), as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

### Series Termination Resistor

When the PCB trace between the clock output (CLK, pin 5) and the load is over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

### Quartz Crystal

The MK3754 VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the following section shown must be followed.

The frequency of oscillation of a quartz crystal is determined by its “cut” and by the load capacitors connected to it. The MK3754 incorporates on-chip variable load capacitors that “pull” (change) the frequency of the crystal. The crystal specified for use with the MK3754 is designed to have zero frequency error when the total of on-chip + stray capacitance is 14pF.

#### Recommended Crystal Parameters:

Initial Accuracy at 25°C	±20 ppm
Temperature Stability	±30 ppm
Aging	±20 ppm
Load Capacitance	14 pF
Shunt Capacitance, C0	7 pF Max
C0/C1 Ratio	250 Max
Equivalent Series Resistance	35 Ω Max

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the MK3754. There should be no via's between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal.

### Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. Stuffing of these capacitors on the PCB is optional. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

To determine the need for and value of the crystal adjustment capacitors, you will need a PC board of your final layout, a frequency counter capable of about 1 ppm resolution and accuracy, two power supplies, and some samples of the crystals which you plan to use in production, along with measured initial accuracy for each crystal at the specified crystal load capacitance, CL.

To determine the value of the crystal capacitors:

1. Connect VDD of the MK3754 to 3.3V. Connect pin 3 of the MK3754 to the second power supply. Adjust the voltage on pin 3 to 0V. Measure and record the frequency of the CLK output.
2. Adjust the voltage on pin 3 to 3.3V. Measure and record the frequency of the same output.

To calculate the centering error:

$$\text{Error} = 10^6 \times \left[ \frac{(f_{3.0V} - f_{\text{target}}) + (f_{0V} - f_{\text{target}})}{f_{\text{target}}} \right] - \text{error}_{\text{xtal}}$$

Where:

$f_{\text{target}}$  = nominal crystal frequency

$\text{error}_{\text{xtal}}$  = actual initial accuracy (in ppm) of the crystal being measured

If the centering error is less than ±25 ppm, no adjustment is needed. If the centering error is more than 25ppm negative, the PC board has excessive stray capacitance and a new PCB layout should be



considered to reduce stray capacitance. (Alternately, the crystal may be re-specified to a higher load capacitance. Contact ICS MicroClock for details.) If the centering error is more than 25ppm positive, add identical fixed centering capacitors from each crystal pin to ground. The value for each of these caps (in pF) is given by:

External Capacitor =

$$2 \times (\text{centering error}) / (\text{trim sensitivity})$$

Trim sensitivity is a parameter which can be supplied by your crystal vendor. If you do not know the value, assume it is 30 ppm/pF. After any changes, repeat the measurement to verify that the remaining error is acceptably low (typically less than  $\pm 25$ ppm).

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK3754. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7V
All Inputs and Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Soldering Temperature	260°C

## Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0	–	+70	°C
Power Supply Voltage (measured in respect to GND)	+3.15		+3.45	V
Reference crystal parameters	Refer to page 3			



## DC Electrical Characteristics

**VDD=3.3V  $\pm$ 5%** , Ambient temperature 0 to +70°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -12 mA	2.4			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 12 mA			0.4	V
Output High Voltage (CMOS Level)	V <sub>OH</sub>	I <sub>OH</sub> = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	No load		9		mA
Short Circuit Current	I <sub>OS</sub>			$\pm$ 50		mA
VIN, VCXO Control Voltage	V <sub>IA</sub>		0		3.3	V

## AC Electrical Characteristics

**VDD = 3.3V  $\pm$ 5%**, Ambient Temperature 0 to +70° C, unless stated otherwise

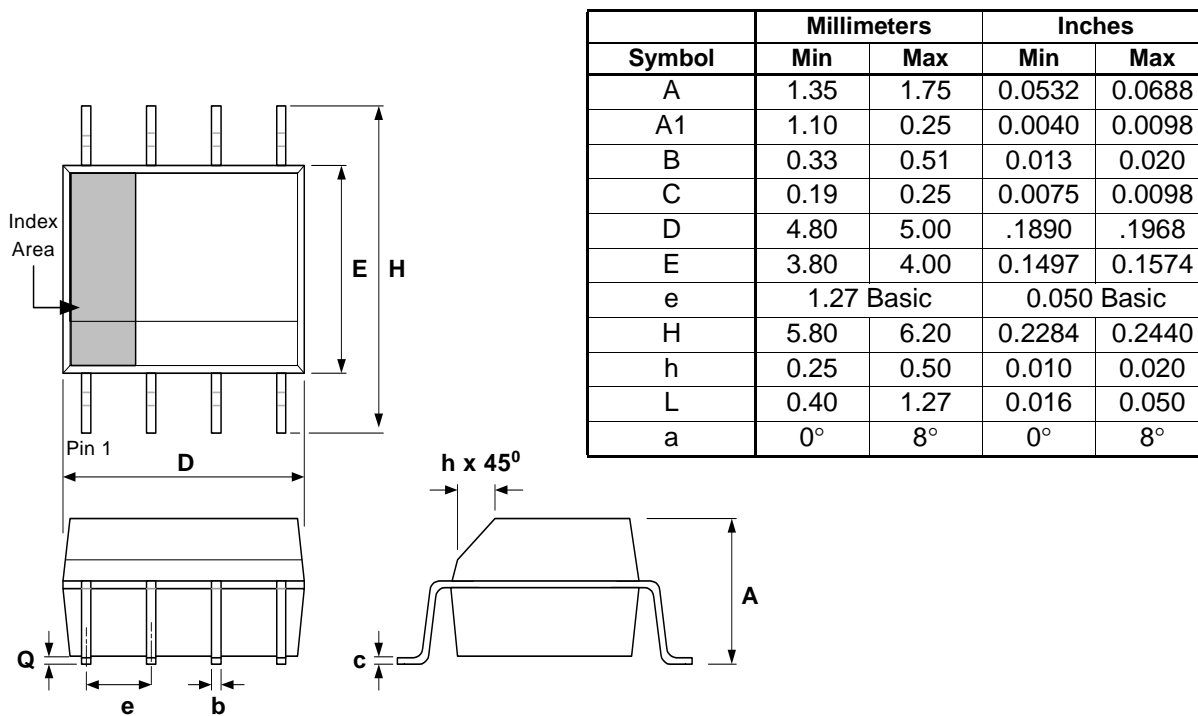
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Crystal Pullability						
MK3754D and MK3754B	F <sub>P</sub>	0V $\leq$ VIN $\leq$ 3.3V, Note 1	$\pm$ 115			ppm
MK3754S	F <sub>P</sub>	0V $\leq$ VIN $\leq$ 3.3V, Note 1	$\pm$ 100			ppm
VCXO Gain						
MK3754D		VIN = VDD/2 $\pm$ 1V, Note 1		120		ppm/V
MK3754B		VIN = VDD/2 $\pm$ 1V, Note 1		150		ppm/V
MK3754S		VIN = VDD/2 $\pm$ 1V, Note 1		100		ppm/V
Output Rise Time	t <sub>OR</sub>	0.8 to 2.0V, C <sub>L</sub> =15pF			1.5	ns
Output Fall Time	t <sub>OF</sub>	2.0 to 0.8V, C <sub>L</sub> =15pF			1.5	ns
Output Clock Duty Cycle	t <sub>D</sub>	Measured at 1.4V, C <sub>L</sub> =15pF	45	50	55	%
Maximum Output Jitter, short term	t <sub>J</sub>	C <sub>L</sub> =15pF		100		ps

Note 1: External crystal device must conform with Pullable Crystal Specifications listed on page 3.



## Package Outline and Package Dimensions (8 pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



## Ordering Information

Part / Order Number (Note 1)	Marking	Shipping packaging	Package	Temperature
MK3754D	MK3754D	Tubes	8 pin SOIC	0 to +70° C
MK3754DTR	MK3754D	Tape and Reel	8 pin SOIC	0 to +70° C
MK3754B	MK3754B	Tubes	8 pin SOIC	0 to +70° C
MK3754BTR	MK3754B	Tape and Reel	8 pin SOIC	0 to +70° C
MK3754S	MK3754S	Tubes	8 pin SOIC	0 to +70° C
MK3754STR	MK3754S	Tape and Reel	8 pin SOIC	0 to +70° C

**Note 1: MK3754D is recommended for new designs. Call factory for information on MK3754S.**

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