



## 3.3V CMOS 18-BIT UNIVERSAL *IDT74ALVCHR16501* BUS TRANSCEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

### FEATURES:

- 0.5 MICRON CMOS Technology
- Typical  $t_{SK(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels ( $0.4\mu W$  typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SSOP, TSSOP, and TVSOP packages

### DRIVE FEATURES:

- Balanced Output Drivers:  $\pm 12mA$
- Low Switching Noise

### APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

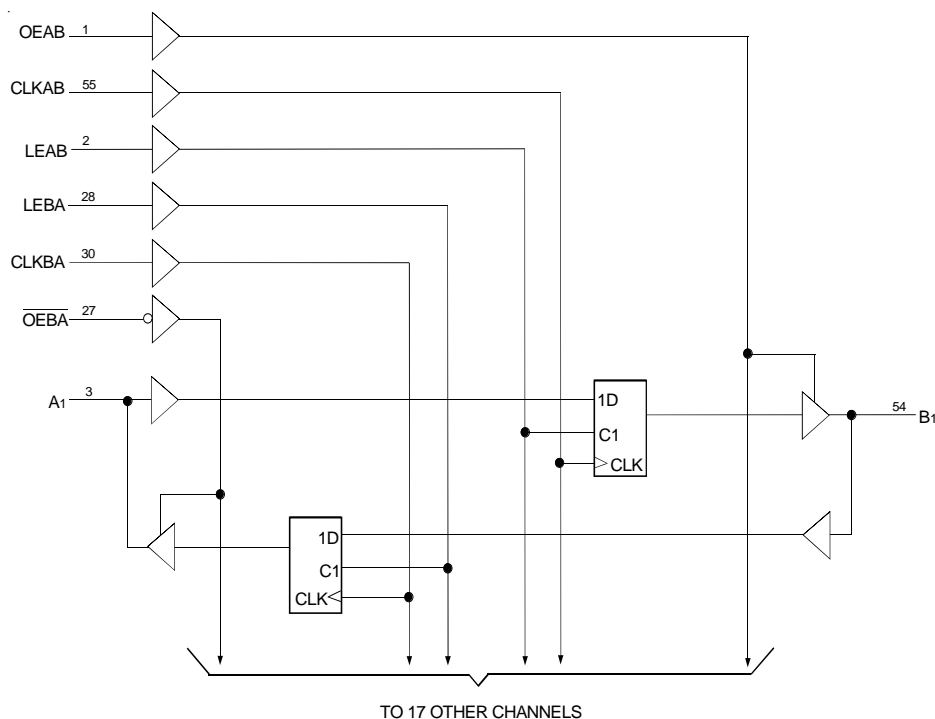
### DESCRIPTION:

This 18-bit universal bus transceiver is built using advanced dual metal CMOS technology. Data flow in each direction is controlled by output-enable ( $OEAB$  and  $\overline{OEBA}$ ), latch enable ( $LEAB$  and  $LEBA$ ) and clock ( $CLKAB$  and  $CLKBA$ ) inputs. For A-to-B data flow, the device operates in the transparent mode when  $LEAB$  is high. When  $LEAB$  is low, the A data is latched if  $CLKAB$  is held at a high or low logic level. If  $LEAB$  is low, the A data is stored in the latch/flip-flop on the low-to-high transition of  $CLKAB$ . When  $OEAB$  is high, the outputs are active. When  $OEAB$  is low, the outputs are in the high-impedance state. Data flow from B to A is similar to that of A to B but uses  $\overline{OEBA}$ ,  $LEBA$ , and  $CLKBA$ . The output enables are complementary ( $OEAB$  is active high and  $\overline{OEBA}$  is active low).

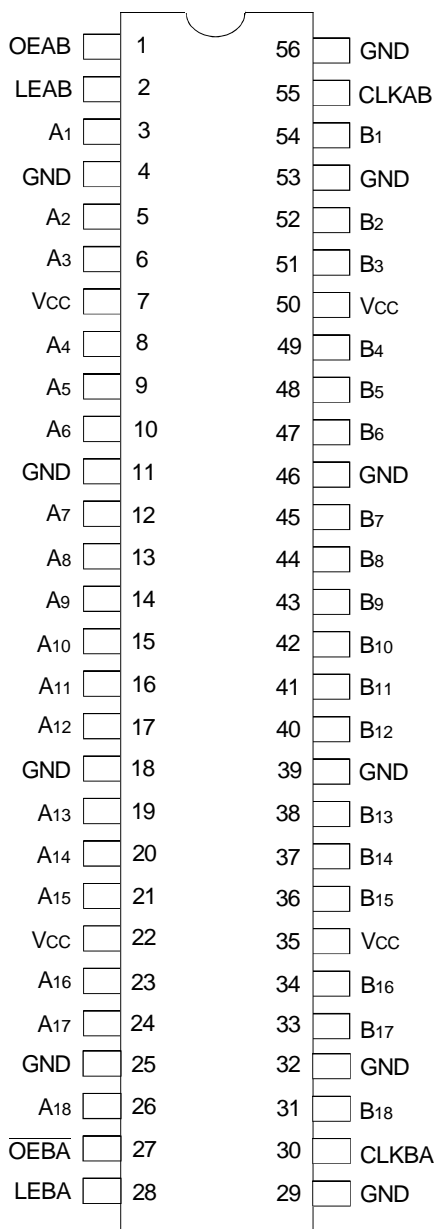
The ALVCHR16501 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive  $\pm 12mA$  at the designated threshold levels.

The ALVCHR16501 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
I <sub>IK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>I</sub> > Vcc	±50	mA
I <sub>OK</sub>	Continuous Clamp Current, V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each Vcc or GND	±100	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- All terminals except Vcc.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	9	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	7	9	pF

### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{\text{OEBA}}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A <sub>x</sub>	A-to-B Data Inputs or B-to-A 3-State Outputs <sup>(1)</sup>
B <sub>x</sub>	B-to-A Data Inputs or A-to-B 3-State Outputs <sup>(1)</sup>

### NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE<sup>(1,2)</sup>

Inputs				Output
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B <sup>(3)</sup>
H	L	H	X	B <sup>(4)</sup>

### NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar, but uses  $\overline{\text{OEBA}}$ , LEBA, and CLKBA.
2. H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance  
↑ = LOW-to-HIGH Transition
3. Output level before the indicated steady-state input conditions were established
4. Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IiH	Input HIGH Current	VCC = 3.6V	Vi = VCC	—	—	±5	μA
IiL	Input LOW Current	VCC = 3.6V	Vi = GND	—	—	±5	μA
IoZH IoZL	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	Vo = VCC	—	—	±10	μA
			Vo = GND	—	—	±10	
VIK	Clamp Diode Voltage	VCC = 2.3V, IIN = -18mA		—	-0.7	-1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL ICCH ICCZ	Quiescent Power Supply Current	VCC = 3.6V VIN = GND or VCC		—	0.1	40	μA
ΔICC	Quiescent Power Supply Current Variation	One input at VCC - 0.6V, other inputs at VCC or GND		—	—	750	μA

### NOTE:

1. Typical values are at VCC = 3.3V, +25°C ambient.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 3V	V <sub>I</sub> = 2V	-75	—	—	μA
			V <sub>I</sub> = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 2.3V	V <sub>I</sub> = 1.7V	-45	—	—	μA
			V <sub>I</sub> = 0.7V	45	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 3.6V	—	—	±500	μA

### NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> - 0.2	—	V
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -4mA	1.9	—	
			I <sub>OH</sub> = -6mA	1.7	—	
		V <sub>CC</sub> = 2.7V	I <sub>OH</sub> = -4mA	2.2	—	
			I <sub>OH</sub> = -8mA	2	—	
		V <sub>CC</sub> = 3V	I <sub>OH</sub> = -6mA	2.4	—	
			I <sub>OH</sub> = -12mA	2	—	
VOL	Output LOW Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
		V <sub>CC</sub> = 2.3V	I <sub>OL</sub> = 4mA	—	0.4	
			I <sub>OL</sub> = 6mA	—	0.55	
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 4mA	—	0.4	
			I <sub>OL</sub> = 8mA	—	0.6	
		V <sub>CC</sub> = 3V	I <sub>OL</sub> = 6mA	—	0.55	
			I <sub>OL</sub> = 12mA	—	0.8	

### NOTE:

1. V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range.  
T<sub>A</sub> = -40°C to +85°C.

## OPERATING CHARACTERISTICS, T<sub>A</sub> = 25°C

Symbol	Parameter	Test Conditions	V <sub>CC</sub> = 2.5V ± 0.2V	V <sub>CC</sub> = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	C <sub>L</sub> = 0pF, f = 10Mhz	—	—	pF
CPD	Power Dissipation Capacitance Outputs disabled		—	—	

## SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ax to Bx or Bx to Ax	1.2	5.9	—	5.2	1	4.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEBA to Ax or LEAB to Bx	1.6	6.8	—	6	1.3	5.2	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLKBA to Ax or CLKAB to Bx	1.7	7.2	—	6.3	1.4	5.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{\text{OEBA}}$ to Ax	1.4	7.3	—	6.7	1.1	5.6	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEAB to Bx	1.1	6.8	—	6	1	5.2	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{\text{OEBA}}$ to Ax	2	6	—	5.1	1.3	4.7	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEAB to Bx	2.2	6.9	—	6.2	1.4	5.5	ns
t <sub>SU</sub>	Set-up Time, data before CLK↑	2.2	—	2.1	—	1.7	—	ns
t <sub>H</sub>	Hold Time, data after CLK↑	0.6	—	0.6	—	0.7	—	ns
t <sub>SU</sub>	Set-up Time, data before LE↓	CLK LOW	1.9	—	1.6	—	1.5	ns
		CLK HIGH	1.3	—	1.1	—	1	
t <sub>H</sub>	Hold Time, data after LE↓, CLK HIGH or LOW	1.4	—	1.7	—	1.4	—	ns
t <sub>w</sub>	Pulse Width, LE HIGH	3.3	—	3.3	—	3.3	—	ns
t <sub>w</sub>	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t <sub>sk(0)</sub>	Output Skew <sup>(2)</sup>	—	—	—	—	—	500	ps

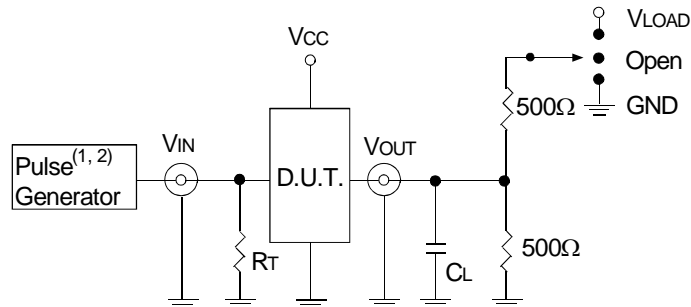
### NOTES:

- See TEST CIRCUITS AND WAVEFORMS. T<sub>A</sub> = – 40°C to + 85°C.
- Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
$V_{LOAD}$	6	6	$2 \times V_{CC}$	V
$V_{IH}$	2.7	2.7	$V_{CC}$	V
$V_T$	1.5	1.5	$V_{CC} / 2$	V
$V_{LZ}$	300	300	150	mV
$V_{HZ}$	300	300	150	mV
$C_L$	50	50	30	pF



Test Circuit for All Outputs

#### DEFINITIONS:

$C_L$  = Load capacitance: includes jig and probe capacitance.

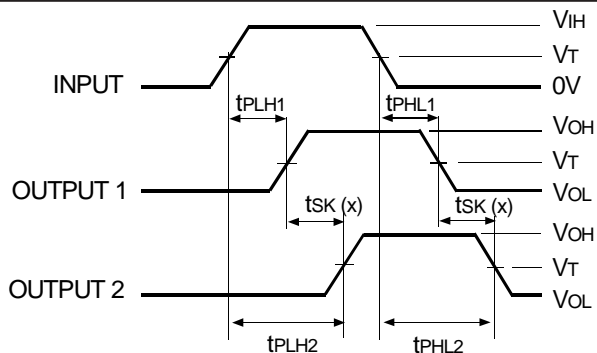
$R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2\text{ns}$ ;  $t_f \leq 2\text{ns}$ .

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	$V_{LOAD}$
Disable High Enable High	GND
All Other Tests	Open

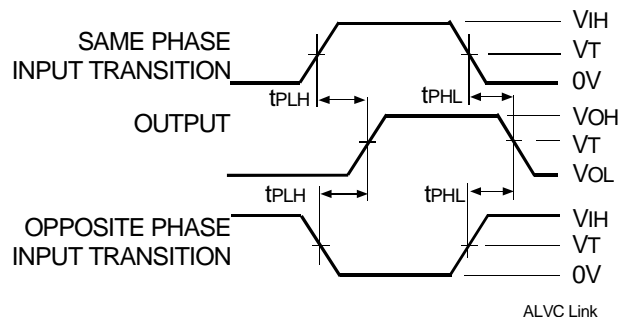


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

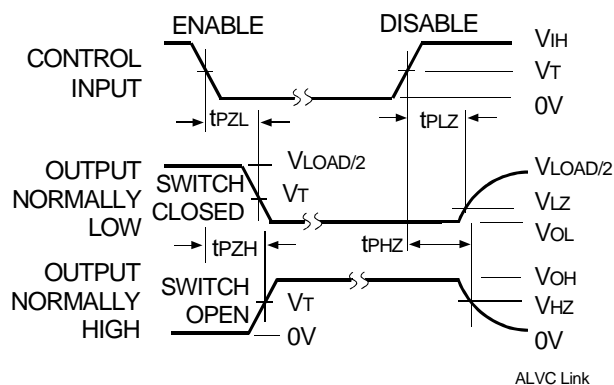
Output Skew -  $tsk(x)$

#### NOTES:

1. For  $tsk(o)$  OUTPUT1 and OUTPUT2 are any two outputs.
2. For  $tsk(b)$  OUTPUT1 and OUTPUT2 are in the same bank.



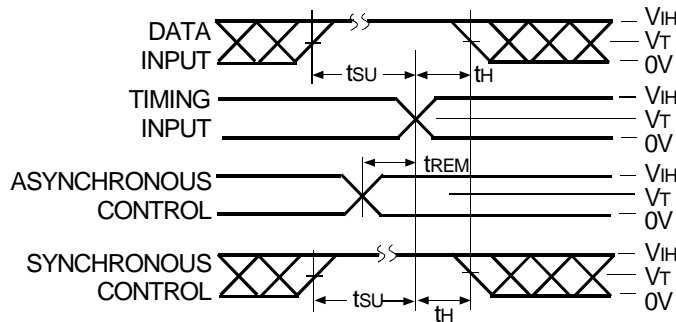
Propagation Delay



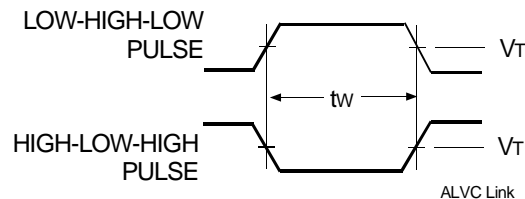
Enable and Disable Times

#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

## ORDERING INFORMATION

IDT	XX	ALVC	X	XXX	XXX	XX		
Temp. Range			Bus-Hold	Family	Device Type	Package		
						PV		Shrink Small Outline Package
						PA		Thin Shrink Small Outline Package
						PF		Thin Very Small Outline Package
						501		18-Bit Universal Bus Transceiver with 3-State Outputs
						R16		Double-Density, $\pm 12\text{mA}$
						H		Bus-Hold
						74		$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$



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