



## 3.3V CMOS 16-BIT BUS REGISTERED TRANSCEIVER, 5 VOLT TOLERANT I/O

**IDT74LVC16652A**

### FEATURES:

- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- CMOS power levels ( $0.4\mu W$  typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SSOP, TSSOP, and TVSOP packages

### DRIVE FEATURES:

- High Output Drivers:  $\pm 24mA$
- Reduced system switching noise

### APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

### DESCRIPTION:

The LVC16652A 16-bit registered transceiver is built using advanced dual metal CMOS technology. This high-speed, low power device is organized as two independent 8-bit bus transceivers with 3-state D-type registers. For example, the OEAB and  $\overline{OEBA}$  signals control the transceiver functions.

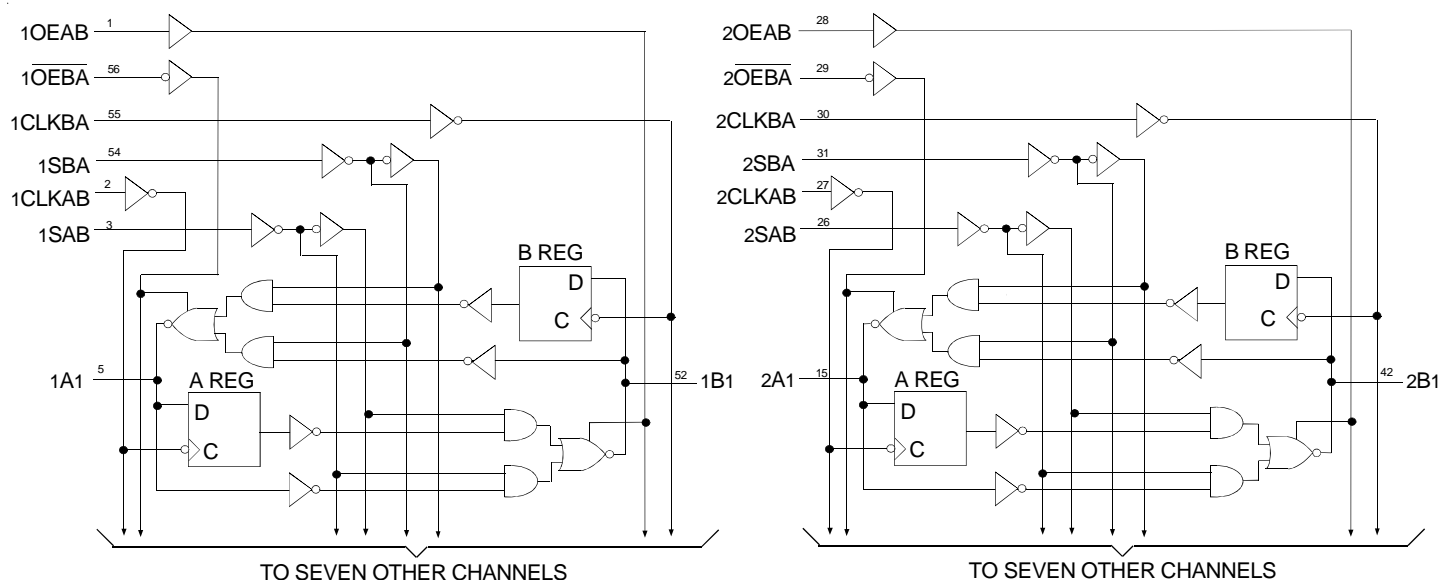
The SAB and the SBA control pins are provided to select either real time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real time data. A Low input level selects real-time data and a High level selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D-flip-flops by the Low-to-High transitions at the appropriate clock pins (CLKAB or CLKBA), regardless of the select or enable control pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

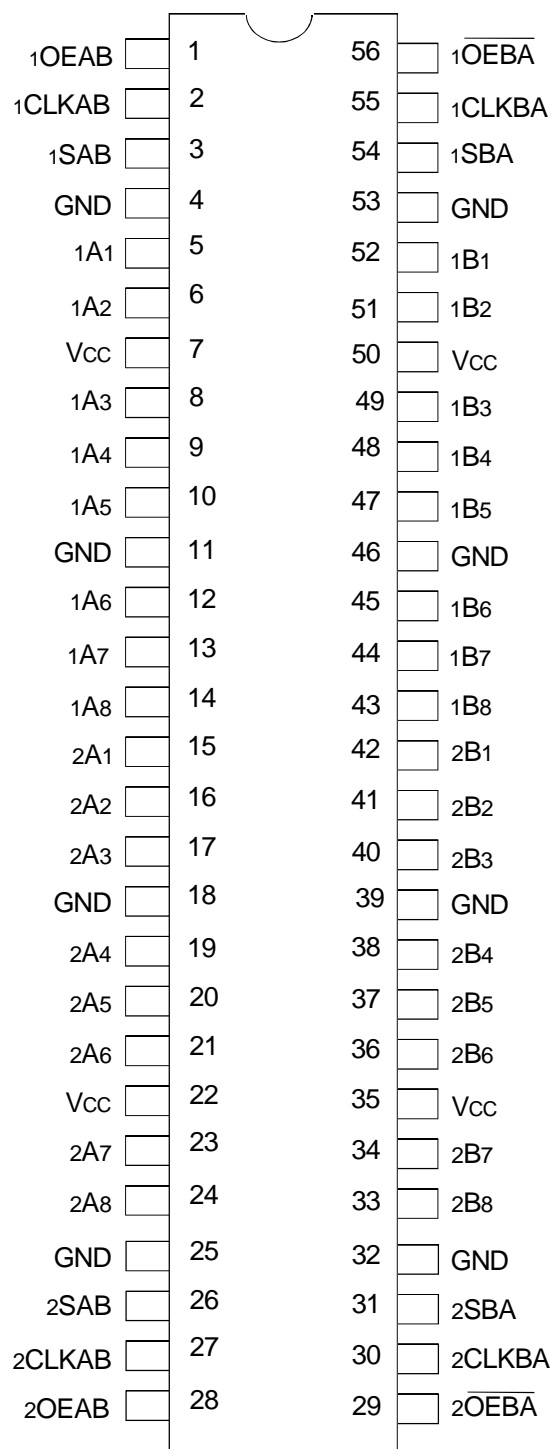
The LVC16652A is ideally suited for driving high capacitance loads and low-impedance backplanes.

All pins can be driven from either a 3.3V or 5V device. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-50 to +50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	6.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xOEAB, xOEBA	Output Enable Inputs

## FUNCTION TABLE<sup>(1,2)</sup>

Inputs						Data I/O <sup>(3)</sup>		Operation or Function
xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified <sup>(3)</sup>	Store A, Hold B
H	H	↑	↑	X <sup>(2)</sup>	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified <sup>(3)</sup>	Input	Store B, Hold A
L	L	↑	↑	X	X <sup>(2)</sup>	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real time B data to A bus
L	L	X	H or L	X	H			Store B data to A bus
H	H	X	X	L	X	Input	Output	Real time A data to B bus
H	H	H or L	X	H	X			Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Store A data to B bus and Store B data to A bus

### NOTES:

1. H = HIGH Voltage Level  
X = Don't Care  
L = LOW Voltage Level  
↑ = LOW-to-HIGH transition
2. Select Control = L: clocks can occur simultaneously.  
Select Control = H: clocks can be staggered to load both registers.
3. The data output functions may be enabled or disabled by various signals at the xOEAB or xOEBA inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

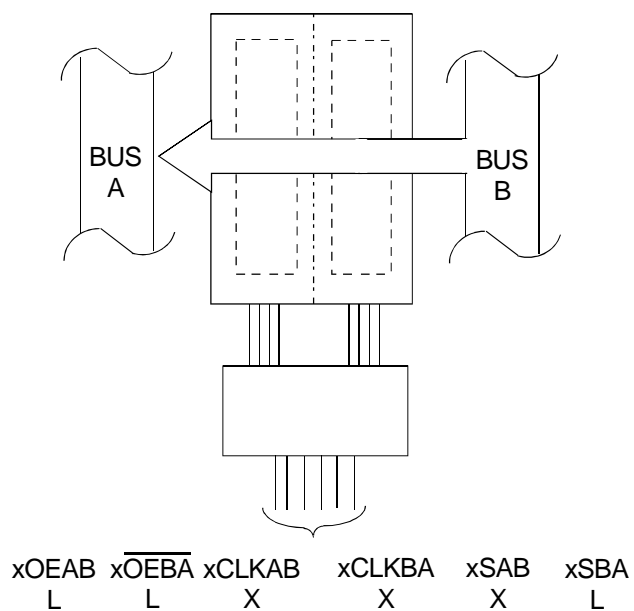
Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

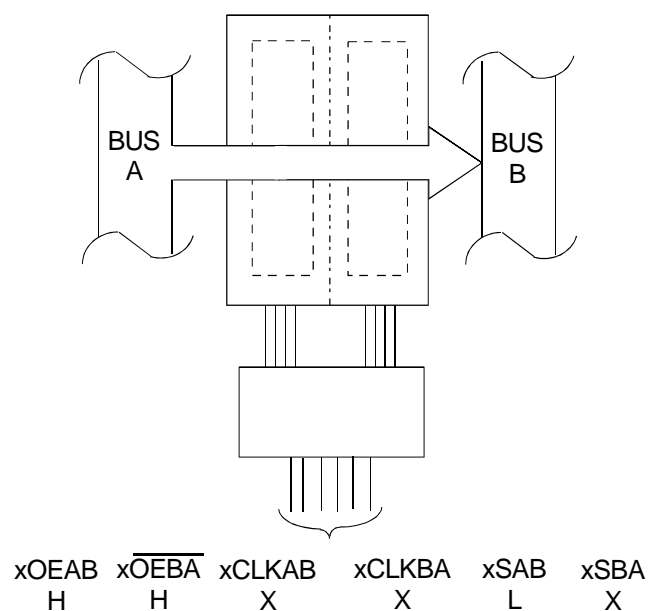
Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		1.7	—	—	V
		V <sub>CC</sub> = 2.7V to 3.6V		2	—	—	
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		—	—	0.7	V
		V <sub>CC</sub> = 2.7V to 3.6V		—	—	0.8	
I <sub>IH</sub> I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 5.5V	—	—	±5	μA
I <sub>OZH</sub> I <sub>OZL</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = 3.6V	V <sub>O</sub> = 0 to 5.5V	—	—	±10	μA
I <sub>OFF</sub>	Input/Output Power Off Leakage	V <sub>CC</sub> = 0V, V <sub>IN</sub> or V <sub>O</sub> ≤ 5.5V		—	—	±50	μA
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = -18mA		—	-0.7	-1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	—	mV
I <sub>CC1</sub> I <sub>CC2</sub> I <sub>CC3</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V	V <sub>IN</sub> = GND or V <sub>CC</sub>	—	—	10	μA
			3.6 ≤ V <sub>IN</sub> ≤ 5.5V <sup>(2)</sup>	—	—	10	
ΔI <sub>CC</sub>	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND		—	—	500	μA

### NOTES:

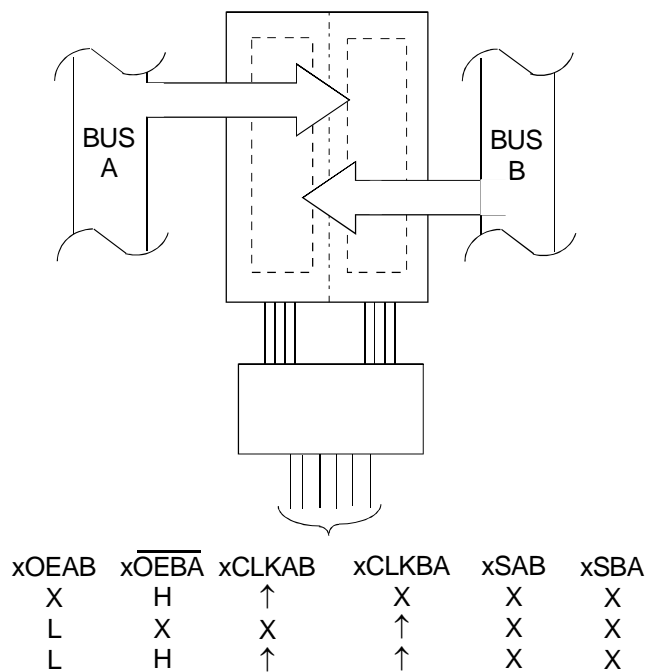
1. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
2. This applies in the disabled state only.



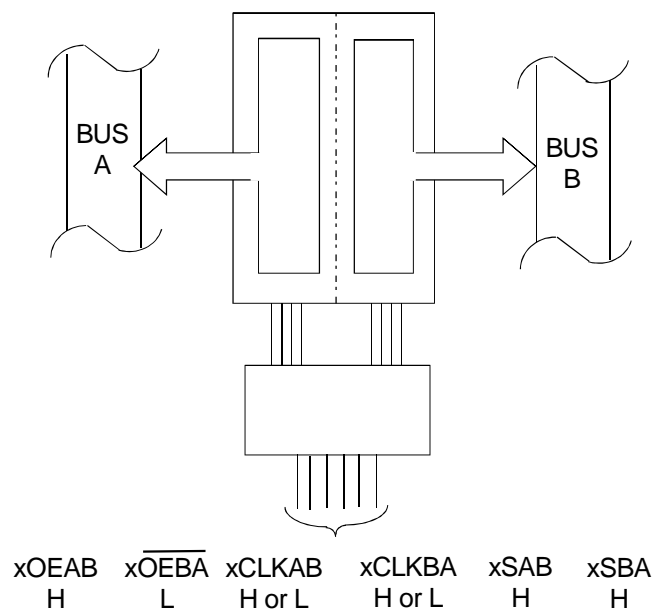
REAL-TIME TRANSFER  
BUS B TO A



REAL-TIME TRANSFER  
BUS A TO B



STORAGE FROM  
A, B, OR A AND B



TRANSFER STORED  
DATA TO A AND/OR B

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 6mA	2	—	
		VCC = 2.3V	IOH = - 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3V		2.4	—	
		VCC = 3V	IOH = - 24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IoL = 0.1mA	—	0.2	V
		VCC = 2.3V	IoL = 6mA	—	0.4	
			IoL = 12mA	—	0.7	
		VCC = 2.7V	IoL = 12mA	—	0.4	
		VCC = 3V	IoL = 24mA	—	0.55	

**NOTE:**

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range.  
TA = - 40°C to + 85°C.

## OPERATING CHARACTERISTICS, VCC = 3.3V ± 0.3V, TA = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	CL = 0pF, f = 10Mhz	55	pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled		12	

## SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
f <sub>MAX</sub>		150	—	150	—	MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay xAx to xBx or xBx to xAx	—	6.4	1.4	6.3	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay xCLKAB or CLKBA to xAx or xBx	—	7.3	2.4	6.4	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay xSBA or xSAB to xAx or xBx	—	8.8	1.9	7.4	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time xOEAB or $\overline{\text{xOEBA}}$ to xAx or Bx	—	6.6	1.6	6.3	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time xOEAB or $\overline{\text{xOEBA}}$ to xAx or Bx	—	6.6	1.2	6.2	ns
t <sub>SU</sub>	Set-up Time HIGH or LOW xAx or xBx before xCLKAB↑ or xCLKBA↑	3.4	—	3	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW xAx or xBx after xCLKAB↑ or xCLKBA↑	0	—	0.2	—	ns
t <sub>w</sub>	Clock Pulse Width HIGH or LOW	3.3	—	3.3	—	ns
t <sub>sk(o)</sub>	Output Skew <sup>(2)</sup>	—	—	—	500	ps

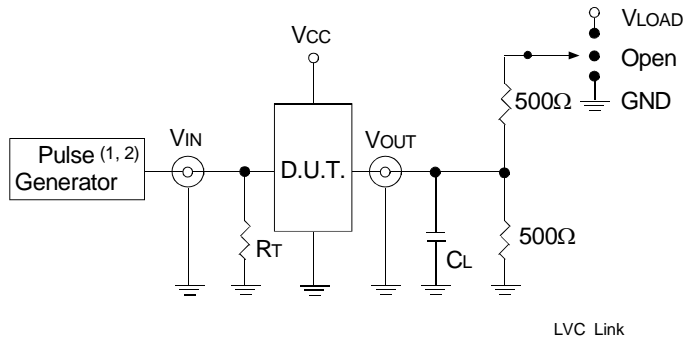
### NOTES:

- See TEST CIRCUITS AND WAVEFORMS. T<sub>A</sub> = – 40°C to + 85°C.
- Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
$V_{LOAD}$	6	6	$2 \times V_{CC}$	V
$V_{IH}$	2.7	2.7	$V_{CC}$	V
$V_T$	1.5	1.5	$V_{CC} / 2$	V
$V_{LZ}$	300	300	150	mV
$V_{HZ}$	300	300	150	mV
$C_L$	50	50	30	pF



Test Circuit for All Outputs

#### DEFINITIONS:

$C_L$  = Load capacitance: includes jig and probe capacitance.

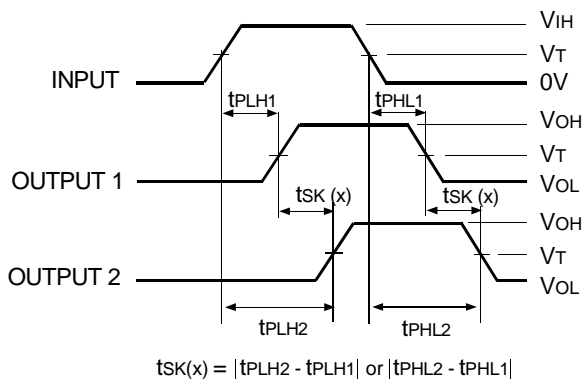
$R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate  $\leq 10\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .
2. Pulse Generator for All Pulses: Rate  $\leq 10\text{MHz}$ ;  $t_r \leq 2\text{ns}$ ;  $t_f \leq 2\text{ns}$ .

## SWITCH POSITION

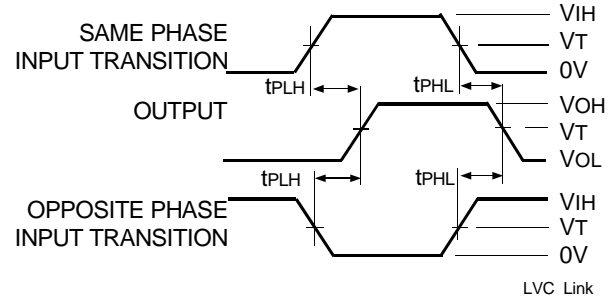
Test	Switch
Open Drain Disable Low Enable Low	$V_{LOAD}$
Disable High Enable High	GND
All Other Tests	Open



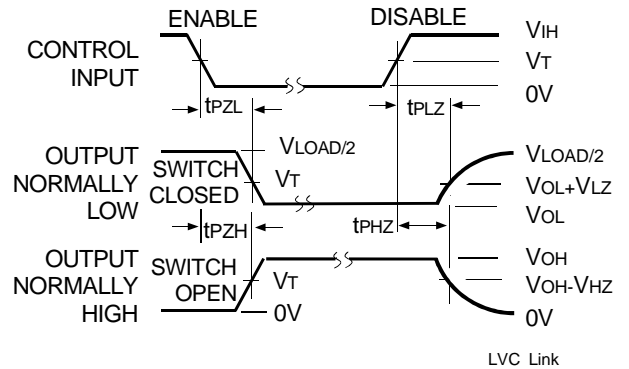
Output Skew -  $tsK(x)$

#### NOTES:

1. For  $tsK(o)$  OUTPUT1 and OUTPUT2 are any two outputs.
2. For  $tsK(b)$  OUTPUT1 and OUTPUT2 are in the same bank.



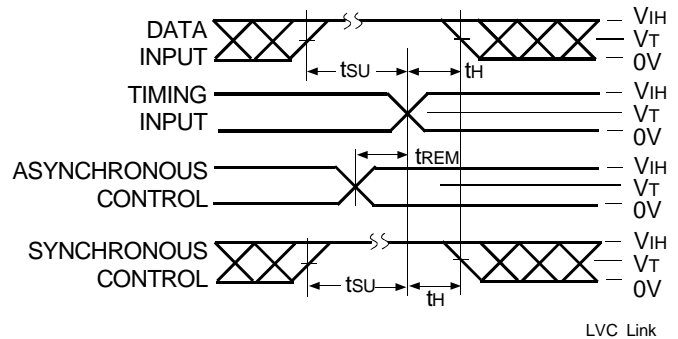
Propagation Delay



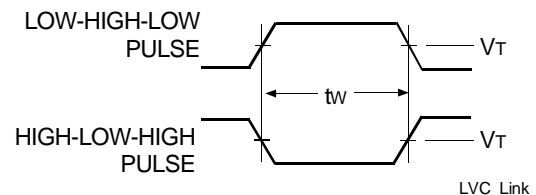
Enable and Disable Times

#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

## ORDERING INFORMATION

IDT	XX	LVC	X	XX	XXXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package
						PA	Thin Shrink Small Outline Package
						PF	Thin Very Small Outline Package
					652A		16-Bit Bus Registered Transceiver with 5 Volt Tolerant I/O
					16		Double-Density, $\pm 24\text{mA}$
					Blank		No Bus-hold
					74		$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$



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