FAST CMOS
BUFFER/CLOCK DRIVER

IDT49FCT805BT/CT
IDT49FCT806BT/CT

Integrated Device Technology, Inc.

FEATURES:
- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 500ps (max.)
- Very low duty cycle distortion < 600ps (max.)
- Low CMOS power levels
- TTL compatible inputs and outputs
- TTL level output voltage swings
- High drive: -32mA I_{OH}, 48mA I_{OL}
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- 'Heartbeat' monitor output
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in DIP, SOIC, SSOP, QSOP, Cerpack and LCC packages

- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:
The IDT49FCT805BT/CT and IDT49FCT806BT/CT are clock drivers built using advanced dual metal CMOS technology. The IDT49FCT805BT/CT is a non-inverting clock driver and the IDT49FCT806BT/CT is an inverting clock driver. Each device consists of two banks of drivers. Each bank drives five output buffers from a standard TTL compatible input. The 805BT/CT and 806BT/CT have extremely low output skew, pulse skew, and package skew. The devices has a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The 805BT/CT and 806BT/CT offer low capacitance inputs with hysteresis.
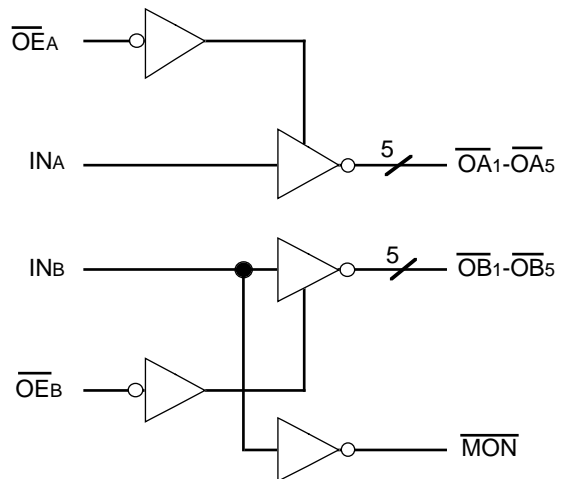
FUNCTIONAL BLOCK DIAGRAMS

IDT49FCT805T
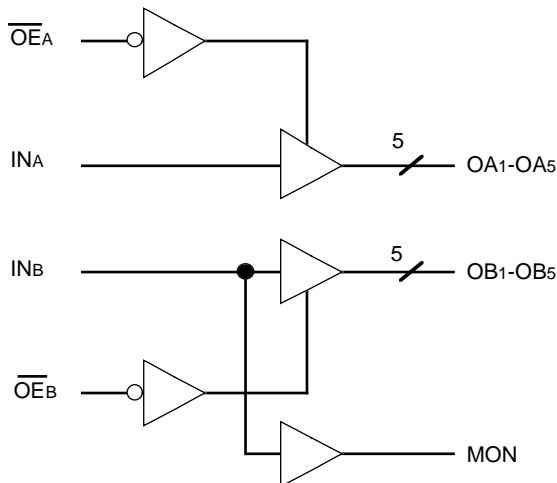
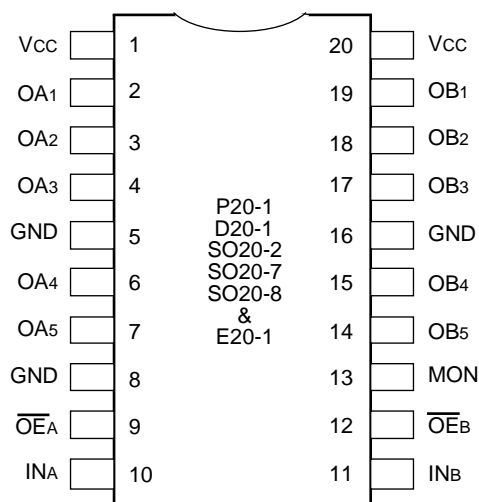
2920 drw 01

IDT49FCT806T

2920 drw 02

MILITARY AND COMMERCIAL TEMPERATURE RANGES

OCTOBER 1995

DSC-2920/5

PIN CONFIGURATIONS

IDT49FCT805T

P20-1
D20-1
SO20-2
SO20-7
SO20-8
&
E20-1

**DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW**

2920 drw 03

L20-2
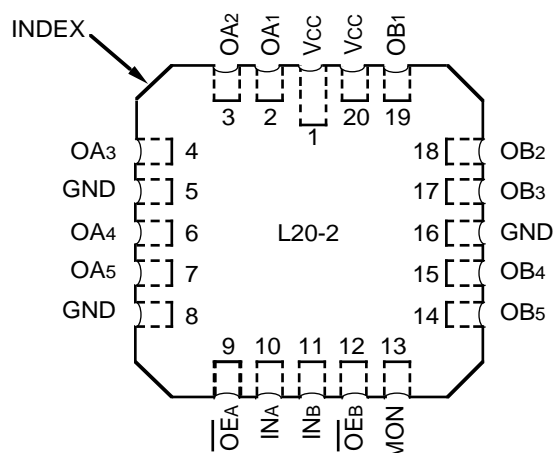
**LCC
TOP VIEW**

2920 drw 04

IDT49FCT806T

P20-1
D20-1
SO20-2
SO20-7
SO20-8
&
E20-1
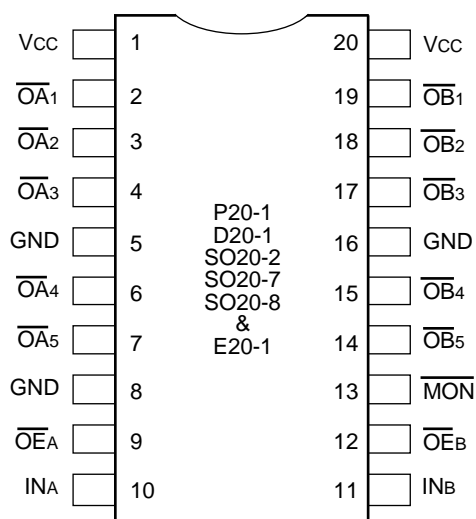
**DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW**

2920 drw 05

L20-2
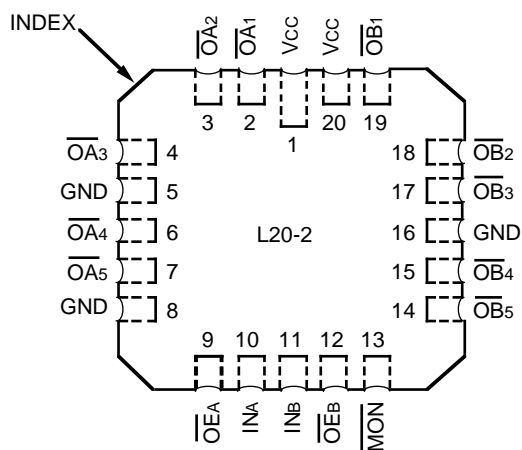
**LCC
TOP VIEW**

2920 drw 06

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OA_n, OB_n	Clock Outputs (FCT805T)
$\overline{OA}_n$, $\overline{OB}_n$	Clock Outputs (FCT806T)
MON	Monitor Output (FCT805T)
$\overline{MON}$	Monitor Output (FCT806T)

2920 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs			
		49FCT805T		49FCT806T	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	OA_n, OB_n	MON	$\overline{OA}_n$, $\overline{OB}_n$	$\overline{MON}$
L	L	L	L	H	H
L	H	H	H	L	L
H	L	Z	L	Z	H
H	H	Z	H	Z	L

2920 tbl 02

NOTE:
1. H = HIGH, L = LOW, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
VTERM[3]	Terminal Voltage with Respect to GND	−0.5 to VCC +0.5	−0.5 to VCC +0.5	V
TA	Operating Temperature	0 to +70	−55 to +125	°C
TBIAS	Temperature Under Bias	−55 to +125	−65 to +135	°C
TSTG	Storage Temperature	−55 to +125	−65 to +150	°C
IOUT	DC Output Current	−60 to +120	−60 to +120	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RAT-INGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.
2. Input and VCC terminals.
3. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
COUT	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2920 lnk 04
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
VIH	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
VIL	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
IIH	Input HIGH Current[5]	VCC = Max.	VI = 2.7V	—	—	±1	µA
IIL	Input LOW Current[5]	VCC = Max.	VI = 0.5V	—	—	±1	µA
IOZH	High Impedance Output Current	VCC = Max.	VO = 2.7V	—	—	±1	µA
IOZL	(3-State Output pins)[5]		VO = 0.5V	—	—	±1	µA
II	Input HIGH Current[5]	VCC = Max., VI = VCC (Max.)		—	—	±1	µA
VIK	Clamp Diode Voltage	VCC = Min., IIN= −18mA		—	−0.7	−1.2	V
IOS	Short Circuit Current	VCC = Max.[3], VO = GND		−60	−120	−225	mA
VOH	Output HIGH Voltage	VCC = Min. VIN = VIH or VIL	IOH = −12mA MIL. IOH = −15mA COM'L.	2.4	3.3	—	V
			IOH = −24mA MIL. IOH = −32mA COM'L.[4]	2.0	3.0	—	
VOL	Output LOW Voltage	VCC = Min. VIN = VIH or VIL	IOL = 32mA MIL. IOL = 48mA COM'L.	—	0.3	0.55	V
IOFF	Input/Output Power Off Leakage[5]	VCC = 0V, VIN or VO ≤ 4.5V		—	—	±1	µA
VH	Input Hysteresis for all inputs	—		—	150	—	mV
ICCL ICCH ICCZ	Quiescent Power Supply Current	VCC = Max., VIN = GND or VCC		—	5	500	µA

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NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = −55°C.

POWER SUPPLY CHARACTERISTICS

	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔIcc	Quiescent Power Supply Current TTL Inputs HIGH	Vcc = Max. Vin = 3.4V[3]		—	0.5	2.0	mA
Iccd	Dynamic Power Supply Current[4]	Vcc = Max. Outputs Open $\overline{OE}_A = \overline{OE}_B$ = GND 50% Duty Cycle	Vin = Vcc Vin = GND	—	60	100	µA/ MHz/bit
Ic	Total Power Supply Current[6]	Vcc = Max. Outputs Open fo = 25MHz	Vin = Vcc Vin = GND	—	1.5	3.0	mA
		50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ =Vcc Mon. Output Toggling	Vin = 3.4V Vin = GND	—	1.8	4.0	
		Vcc = Max. Outputs Open fo = 50MHz	Vin = Vcc Vin = GND	—	33	55.5[5]	
		50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND Eleven Outputs Toggling	Vin = 3.4V Vin = GND	—	33.5	57.5[5]	

2920 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input; (Vin = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula.   These limits are guaranteed but not tested.
6. Ic = Iquiescent + Iinputs + Idynamic
   Ic = Icc + ΔIcc DHNT + Iccd (foNo)
   Icc = Quiescent Current (Iccl, Icch and Iccz)
   ΔIcc = Power Supply Current for a TTL High Input (Vin = 3.4V)
   DH = Duty Cycle for TTL Inputs High
   NT = Number of TTL Inputs at DH
   Iccd = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   fo= Output Frequency
   No= Number of Outputs at fo
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3,4]

| Symbol | Parameter | Condition[1] | IDT49FCT805BT/806BT | | | | IDT49FCT805CT/806CT | | | | Unit |
| | | | Com'l. | | Mil. | | Com'l. | | Mil. | | |
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_n, IN_B to OB_n	C_L = 50pF R_L = 500Ω	1.5	5.0	1.5	5.7	1.5	4.5	1.5	5.2	ns
t_R	Output Rise Time		—	1.5	—	2.0	—	1.5	—	2.0	ns
t_F	Output Fall Time		—	1.5	—	1.5	—	1.5	—	1.5	ns
$t_{SK(o)}$	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.7	—	0.9	—	0.5	—	0.7	ns
$t_{SK(p)}$	Pulse skew: skew between opposite transitions of same output ($|t_{PHL}-t_{PLH}|$)		—	0.7	—	0.9	—	0.6	—	0.8	ns
$t_{SK(t)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.2	—	1.5	—	1.0	—	1.2	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	6.0	1.5	6.5	1.5	5.0	1.5	6.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	6.0	1.5	6.5	1.5	5.0	1.5	6.0	ns

2920 tbl 07

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, $t_{SK(t)}$ are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR ALL OUTPUTS

VCC

7.0V

500Ω

Pulse Generator

VIN

D.U.T.

V OUT

R T

50pF

C L

500Ω

2920 drw 07
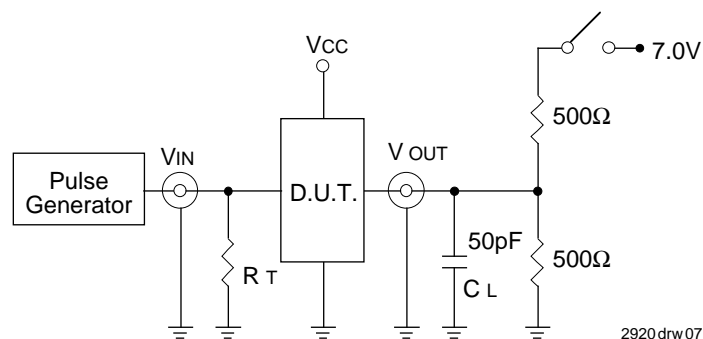
ENABLE AND DISABLE TIME
SWITCH POSITION

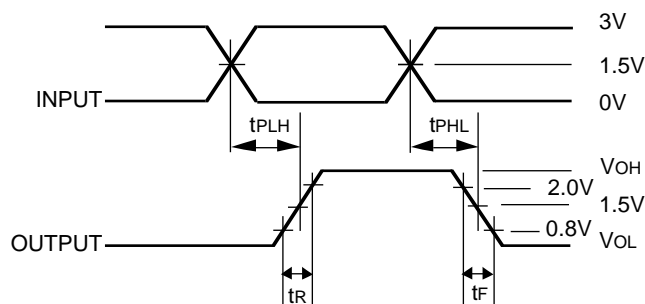| Test	Switch
Disable LOW Enable LOW	Closed
Disable HIGH Enable HIGH	Open

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DEFINITIONS:
C_L= Load capacitance: includes jig and probe capacitance.
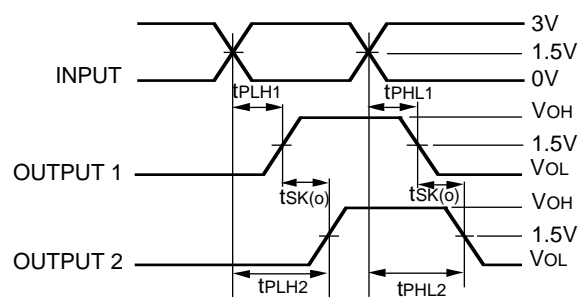R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
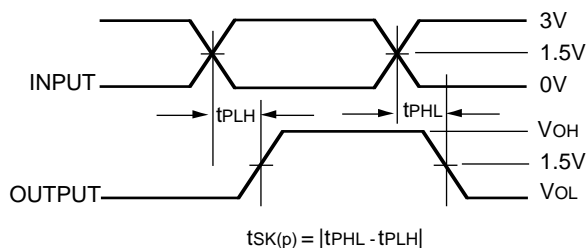
PACKAGE DELAY

3V
1.5V
0V
INPUT
tPLH
tPHL
VOH
2.0V
1.5V
0.8V VOL
OUTPUT
tR
tF

2920 drw 08

OUTPUT SKEW- tSK(o)

3V
1.5V
0V
INPUT
tPLH1
tPHL1
VOH
1.5V
VOL
OUTPUT 1
tSK(o)
tSK(o)
VOH
1.5V
VOL
OUTPUT 2
tPLH2
tPHL2

$t_{SK(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$
2920 drw 09

PULSE SKEW - tSK(p)

3V
1.5V
0V
INPUT
tPLH
tPHL
VOH
1.5V
VOL
OUTPUT

$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

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PACKAGE SKEW - tSK(t)

3V
1.5V
0V
INPUT
tPLH1
tPHL1
VOH
1.5V
VOL
PACKAGE 1 OUTPUT
tSK(t)
tSK(t)
VOH
1.5V
VOL
PACKAGE 2 OUTPUT
tPLH2
tPHL2
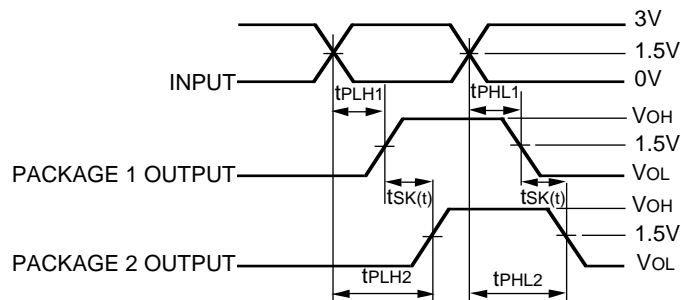
$t_{SK(t)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$
Package 1 and Package 2 are same device type and speed grade

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ENABLE AND DISABLE TIMES

ENABLE
DISABLE
3V
1.5V
0V
CONTROL INPUT
t PZL
t PLZ
OUTPUT NORMALLY LOW
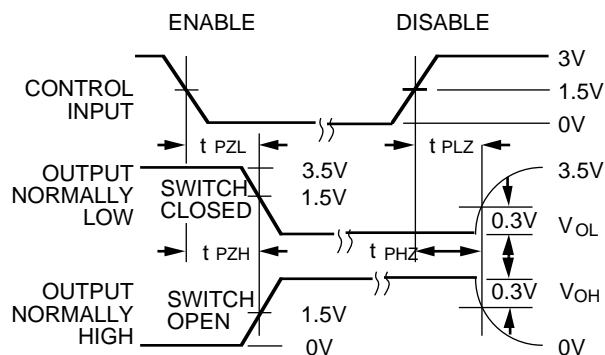SWITCH CLOSED
3.5V
1.5V
0.3V VOL
t PZH
t PHZ
OUTPUT NORMALLY HIGH
SWITCH OPEN
0.3V VOH
1.5V
0V

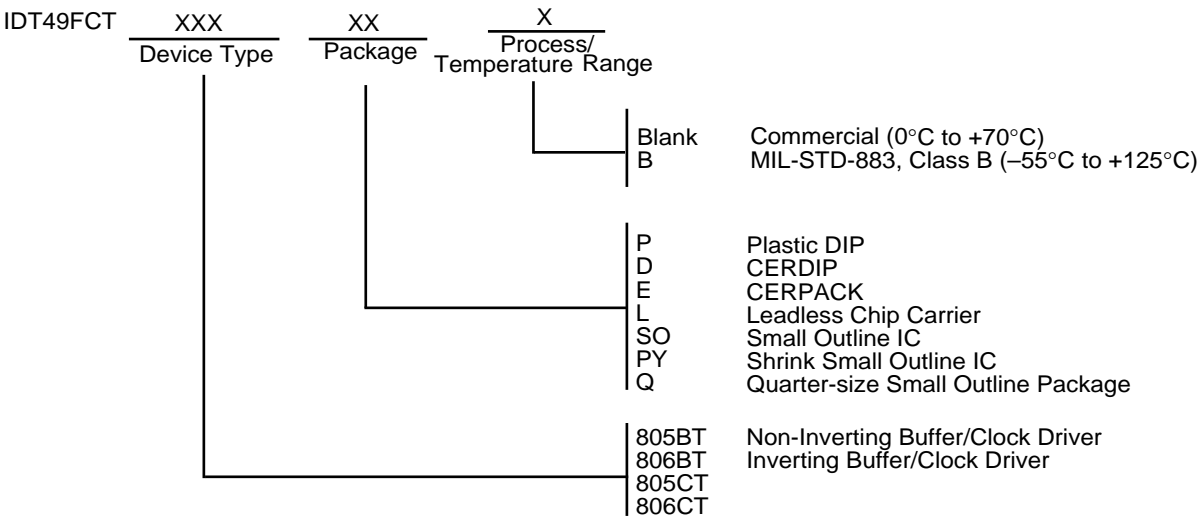2920 drw 12

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: $f \leq 1.0$MHz; $t_F \leq 2.5$ns; $t_R \leq 2.5$ns

ORDERING INFORMATION

```
IDT49FCT    XXX          XX           X
         Device Type   Package     Process/
                              Temperature Range
```

Blank	Commercial (0°C to +70°C)	
B	MIL-STD-883, Class B (–55°C to +125°C)	

P	Plastic DIP
D	CERDIP
E	CERPACK
L	Leadless Chip Carrier
SO	Small Outline IC
PY	Shrink Small Outline IC
Q	Quarter-size Small Outline Package

805BT	Non-Inverting Buffer/Clock Driver
806BT	Inverting Buffer/Clock Driver
805CT	
806CT	

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