



Integrated Device Technology, Inc.

FAST CMOS ADDRESS/ CLOCK DRIVER

IDT54/74FCT162344AT/CT/ET

FEATURES:

- 0.5 MICRON CMOS Technology
- Ideal for address line driving and clock distribution
- 8 banks with 1:4 fanout and 3-state
- Typical tsk(o) (Output Skew) < 500ps
- Balanced Output Drivers: $\pm 24\text{mA}$ (commercial), $\pm 16\text{mA}$ (military)
- Reduced system switching noise
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)

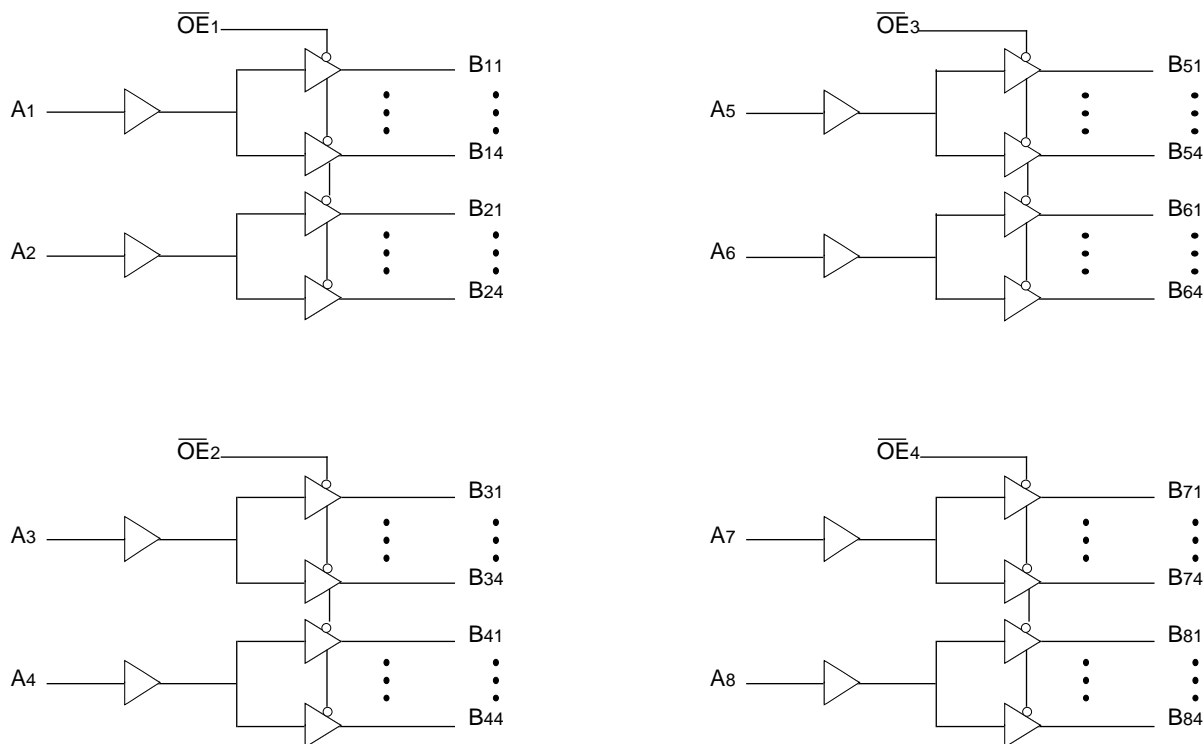
DESCRIPTION:

The FCT162344AT/CT/ET is a 1:4 address line driver built using advanced dual metal CMOS technology. This high-speed, low power device provides the ability to fanout to memory arrays. Eight banks, each with a fanout of 4, and 3-state control provide efficient address distribution. One or more banks may be used for clock distribution.

The FCT162344AT/CT/ET has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times reducing the need for external series terminating resistors.

A large number of power and ground pins and TTL output swings also ensure reduced noise levels. All inputs are designed with hysteresis for improved noise margins.

FUNCTIONAL BLOCK DIAGRAM



3069 drw 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AUGUST 1996

SSOP/TSSOP/TVSOP TOP VIEW				CERPACK TOP VIEW			
OE1	1	56	OE4	1	56	OE4	
B11	2	55	B81	2	55	B81	
B12	3	54	B82	3	54	B82	
GND	4	53	GND	4	53	GND	
B13	5	52	B83	5	52	B83	
B14	6	51	B84	6	51	B84	
VCC	7	50	VCC	7	50	VCC	
A1	8	49	A8	8	49	A8	
B21	9	48	B71	9	48	B71	
B22	10	47	B72	10	47	B72	
GND	11	46	GND	11	46	GND	
B23	12	45	B73	12	45	B73	
B24	13	44	B74	13	44	B74	
A2	14	43	A7	14	43	A7	
A3	15	42	A6	15	42	A6	
B31	16	41	B61	16	41	B61	
B32	17	40	B62	17	40	B62	
GND	18	39	GND	18	39	GND	
B33	19	38	B63	19	38	B63	
B34	20	37	B64	20	37	B64	
A4	21	36	A5	21	36	A5	
VCC	22	35	VCC	22	35	VCC	
B41	23	34	B51	23	34	B51	
B42	24	33	B52	24	33	B52	
GND	25	32	GND	25	32	GND	
B43	26	31	B53	26	31	B53	
B44	27	30	B54	27	30	B54	
OE2	28	29	OE3	28	29	OE3	

PIN DESCRIPTION

Pin Names	Description
$\overline{\text{OEx}}$	3-State Output Enable Inputs (Active LOW)
Ax	Inputs
Bxx	3-State Outputs

3069 tbl 01

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} (2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
V _{TERM} (3)	Terminal Voltage with Respect to GND	−0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	DC Output Current	−60 to +120	mA

NOTES:

3069 Ink 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT.

FUNCTION TABLE⁽¹⁾

Inputs		Outputs
$\overline{\text{OEx}}$	Ax	Bxx
L	L	L
L	H	H
H	X	Z

3069 tbl 02

NOTE:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High Impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	3.5	8.0	pF

3069 Ink 04

NOTE:

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-80	-140	-225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$		—	5	500	μA

3069 Ink 05

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		60	115	200	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		-60	-115	-200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -16\text{mA MIL.}$ $I_{OH} = -24\text{mA COM'L.}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 16\text{mA MIL.}$ $I_{OL} = 24\text{mA COM'L.}$	—	0.3	0.55	V

NOTES:

3069 Ink 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE}_x = \text{GND}$ One Input Bit Toggling Four Output Bits Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	170	220	μA / MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{OE}_x = \text{GND}$ One Input Bit Toggling Four Output Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.7	2.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2.0	3.5	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{OE}_x = \text{GND}$ Eight Input Bits Toggling Thirty Two Output Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.4	4.9 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	5.4	10.9 ⁽⁵⁾	

NOTES:

3069 tbl 07

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT162344AT				FCT162344CT				FCT162344ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Ax to Bxx	CL = 50pF RL = 500Ω	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.6	1.5	3.8	—	—	ns
tPZH tPZL	Output Enable Time OEx to Bx		1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	1.5	5.0	—	—	ns
tPHZ tPLZ	Output Disable Time OEx to Bx		1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	1.5	4.6	—	—	ns
tsk1(o)	Skew between outputs of same bank and same package (same transition) ⁽³⁾		—	0.5	—	0.5	—	0.35	—	0.35	—	0.25	—	—	ns
tsk2(o)	Skew between outputs of all banks of same package (A1 thru A8 tied together) ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

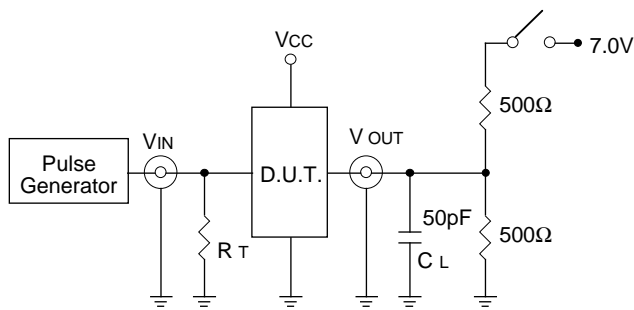
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

3069 tbl 08

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3069 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

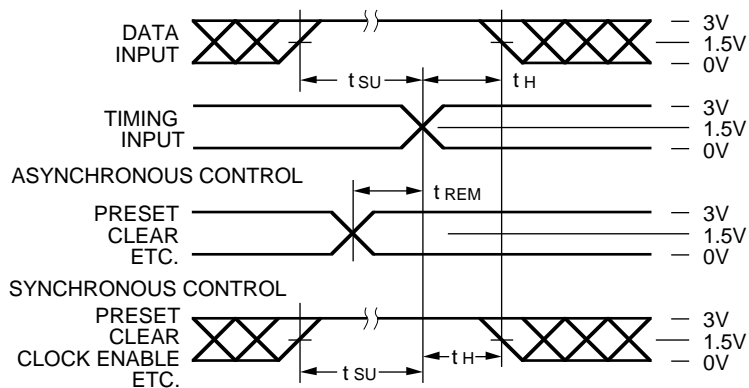
DEFINITIONS:

3069 Ink 09

CL = Load capacitance: includes jig and probe capacitance.

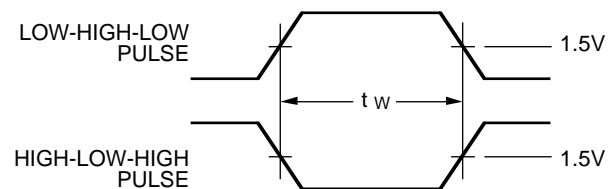
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



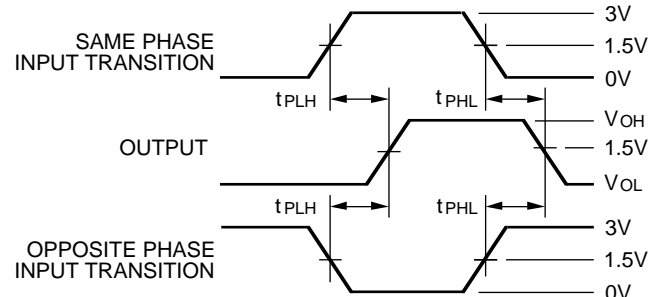
3069 drw 05

PULSE WIDTH



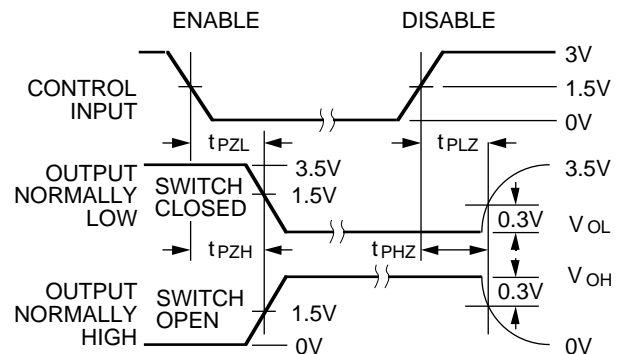
3069 drw 06

PROPAGATION DELAY



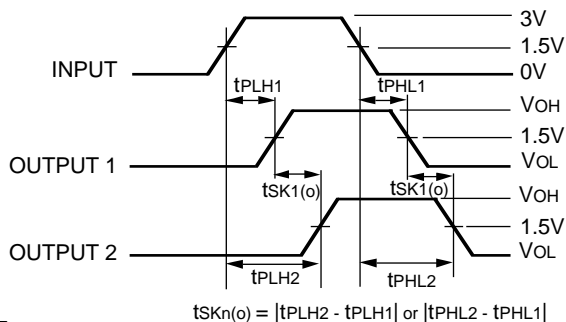
3069 drw 07

ENABLE AND DISABLE TIMES



3069 drw 08

OUTPUT SKEW - tSKn(o)



$$tSKn(o) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$

NOTE:

- For tsk1(o) OUTPUT1 and OUTPUT 2 are in the same bank,
For tsk2(o) OUTPUT1 and OUTPUT 2 are in different banks on the same part.

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$

ORDERING INFORMATION

IDT	XX	FCT	XXXX	X	X		
Temp. Range		Device Type		Package	Process		
					Blank	Commercial	
					B	MIL-STD-883, Class B	
					PV	Shrink Small Outline Package (SO56-1)	
					PA	Thin Shrink Small Outline Package (SO56-2)	
					PF	Thin Very Small Outline Package (SO56-3)	
						E	CERPACK (E56-1)
						162344AT	Address Line Driver
						162344CT	
162344ET							
			54	−55°C to +125°C			
			74	−40°C to +85°C			

3069 drw 09