



Integrated Device Technology, Inc.

# FAST CMOS 16-BIT REGISTERED/LATCHED TRANSCIVER WITH PARITY

IDT54/74FCT162511AT/CT

## FEATURES:

- 0.5 MICRON CMOS Technology
- Typical tsk(o) (Output Skew) < 250ps, clocked mode
- Low input and output leakage  $\leq 1\mu\text{A}$  (max)
- ESD > 2000V per MIL-STD-883, Method 3015;  
> 200V using machine model (C = 200pF, R = 0)
- Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP,  
15.7 mil pitch TVSOP and 25 mil pitch Cerpack
- Extended commercial range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- $V_{CC} = 5V \pm 10\%$
- Balanced Output Drivers:  $\pm 24\text{mA}$  (commercial)  
 $\pm 16\text{mA}$  (military)
- Series current limiting resistors
- Generate/Check, Check/Check modes
- Open drain parity error allows wire-OR

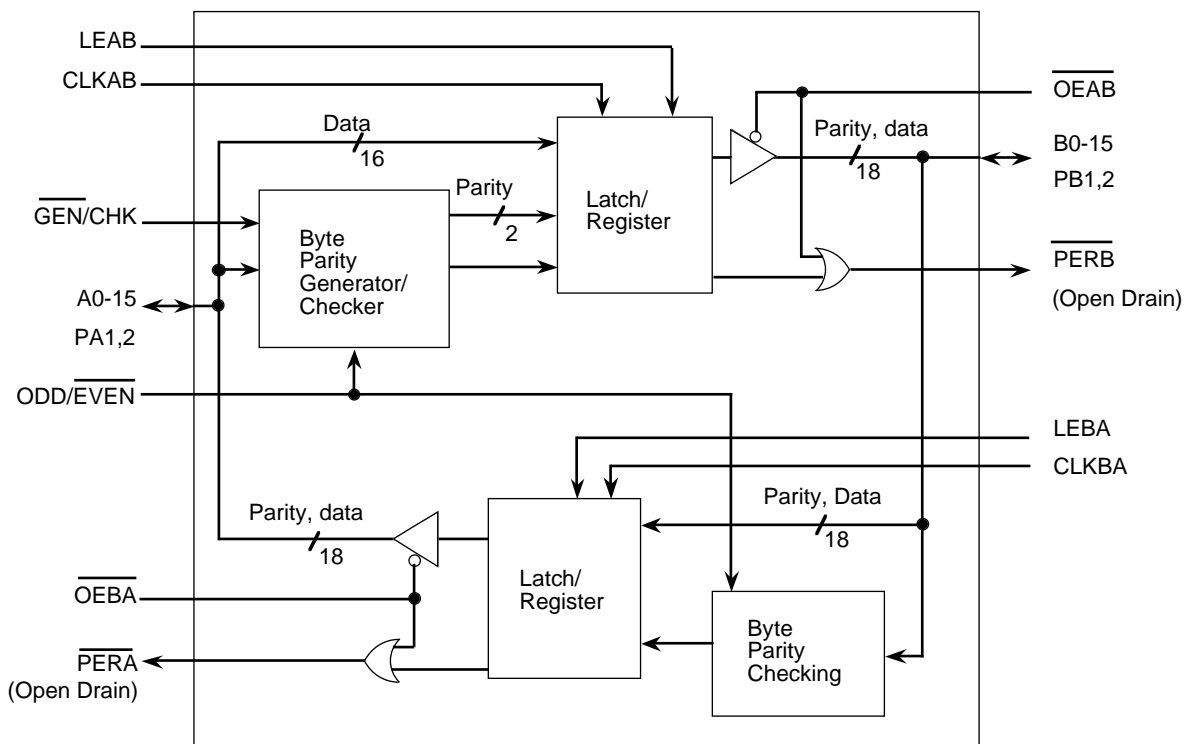
## DESCRIPTION:

The FCT162511AT/CT 16-bit registered/latched transceiver with parity is built using advanced dual metal CMOS technology. This high-speed, low-power transceiver combines D-

type latches and D-type flip-flops to allow data flow in transparent, latched or clocked modes. The device has a parity generator/checker in the A-to-B direction and a parity checker in the B-to-A direction. Error checking is done at the byte level with separate parity bits for each byte. Separate error flags exits for each direction with a single error flag indicating an error for either byte in the A-to-B direction and a second error flag indicating an error for either byte in the B-to-A direction. The parity error flags are open drain outputs which can be tied together and/or tied with flags from other devices to form a single error flag or interrupt. The parity error flags are enabled by the  $\overline{\text{OE}}_{xx}$  control pins allowing the designer to disable the error flag during combinational transitions.

The control pins LEAB, CLKAB and  $\overline{\text{OE}}_{AB}$  control operation in the A-to-B direction while LEBA, CLKBA and  $\overline{\text{OE}}_{BA}$  control the B-to-A direction.  $\overline{\text{GEN}}/\overline{\text{CHK}}$  is only for the selection of A-to-B operation, the B-to-A direction is always in checking mode. The ODD/EVEN select is common between the two directions. Except for the ODD/EVEN control, independent operation can be achieved between the two directions by using the corresponding control lines.

## SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM:



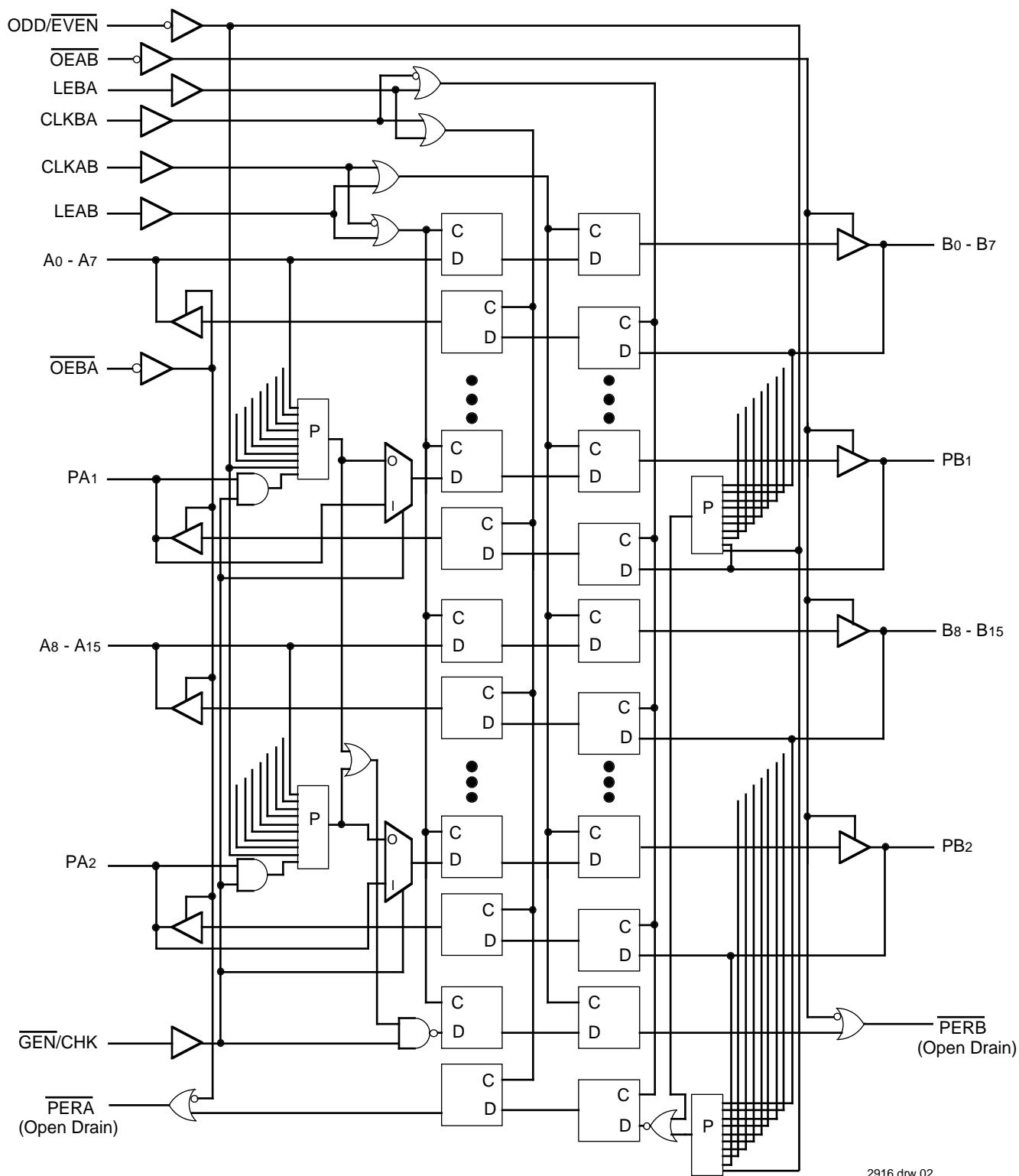
2916 drw 01

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

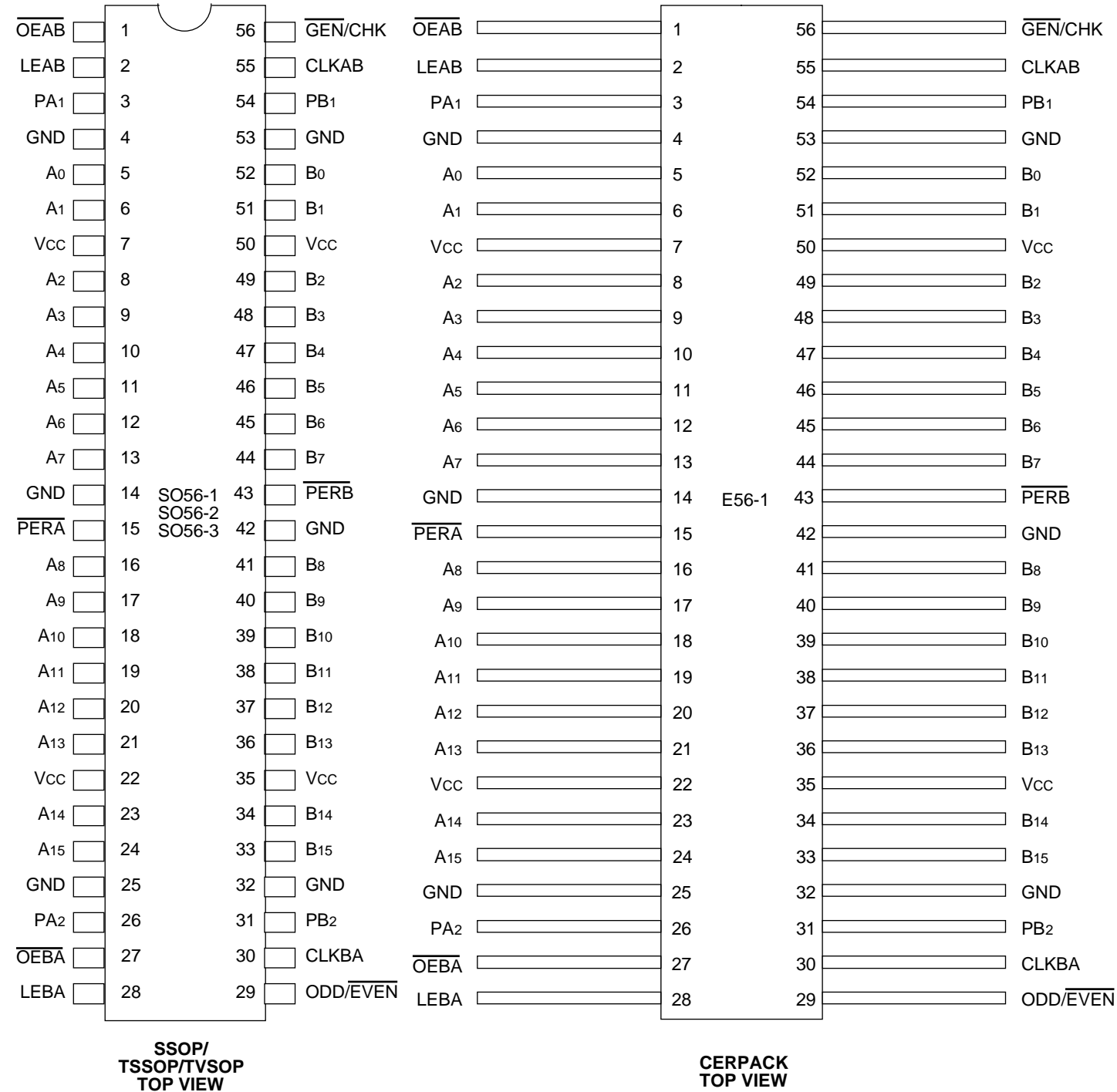
AUGUST 1996

## FUNCTIONAL BLOCK DIAGRAM



2916 drw 02

PIN CONFIGURATIONS



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max.	Unit
V <sub>TERM</sub> (2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
V <sub>TERM</sub> (3)	Terminal Voltage with Respect to GND	−0.5 to V <sub>CC</sub> +0.5	V
T <sub>STG</sub>	Storage Temperature	−65 to +150	°C
I <sub>OUT</sub>	DC Output Current	−60 to +120	mA

### NOTES:

2916 Ink 01

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Open drain and all device terminals except FCT162XXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT.

## FUNCTION TABLE<sup>(1,4)</sup>

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L	X	B <sup>(2)</sup>
L	L	H	X	B <sup>(3)</sup>

### NOTES:

2916 tbl 02

- A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High Impedance  
↑ = LOW-to-HIGH Transition

## PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input (Active LOW)
OEBA	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs
PERA	Parity Error (Open Drain) on A Outputs
PERB	Parity Error (Open Drain) on B Outputs
PAx <sup>(1)</sup>	A-to-B Parity Input, B-to-A Parity Output
PBx	B-to-A Parity Input, A-to-B Parity Output
ODD/EVEN	Parity Mode Selection Input
GEN/CHK	A to B Port Generate or Check Mode Input

### NOTES:

2916 tbl 03

- The PAx pin input is internally disabled during parity generation. This means that when generating parity in the A to B direction there is no need to add a pull up resistor to guarantee state. The pin will still function properly as the parity output for the B to A direction.

## CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	3.5	6.0	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 0V	3.5	8.0	pF
C <sub>O</sub>	Open Drain Capacitance	V <sub>OUT</sub> = 0V	3.5	6.0	pF

### NOTE:

1. This parameter is measured at characterization but not tested.

2916 lmk 04

## FUNCTION TABLE (PARITY CHECKING)<sup>(1, 2, 3, 4)</sup>

A <sub>0</sub> - A <sub>7</sub> and PA <sub>1</sub> <sup>(5)</sup> , Total Number of inputs that are high	ODD/ <u>EVEN</u>	<u>PERB</u>
1, 3, 5, 7 or 9	L	L
1, 3, 5, 7 or 9	H	H <sup>(6)</sup>
0, 2, 4, 6 or 8	L	H <sup>(6)</sup>
0, 2, 4, 6 or 8	H	L

### NOTES:

- Conditions shown are for  $\overline{\text{GEN}}/\text{CHK} = \text{H}$ ,  $\overline{\text{OEAB}} = \text{L}$ ,  $\overline{\text{OEBA}} = \text{H}$ .
- A-to-B parity checking is shown. B-to-A parity checking is similar but uses  $\overline{\text{OEBA}} = \text{L}$ ,  $\overline{\text{OEAB}} = \text{H}$  and errors will be indicated on  $\overline{\text{PERA}}$ .
- In parity checking mode the parity bits will be transmitted unchanged along with the corresponding data regardless of parity errors. (PB<sub>1</sub> = PA<sub>1</sub>).
- The response shown is for LEAB = H. If LEAB = L then CLKAB will control as an edge triggered clock.
- Conditions shown are for the byte A<sub>0</sub>-A<sub>7</sub> and PA<sub>1</sub>. The byte A<sub>8</sub>-A<sub>15</sub> and PA<sub>2</sub> is similar.
- The parity error flag  $\overline{\text{PERB}}$  is a combined flag for both bytes A<sub>0</sub>-A<sub>7</sub> and A<sub>8</sub>-A<sub>15</sub>. If a parity error occurs on either byte  $\overline{\text{PERB}}$  will go low.  $\overline{\text{PERB}}$  is an open drain output which must be externally pulled up to achieve a logic HIGH.

2916 tbl 05

## FUNCTION TABLE (PARITY GENERATION)<sup>(1, 2, 3, 4, 5)</sup>

A <sub>0</sub> - A <sub>7</sub> , Total Number of inputs that are high	ODD/ <u>EVEN</u>	PB <sub>1</sub>
1, 3, 5 or 7	L	H
1, 3, 5 or 7	H	L
0, 2, 4, 6 or 8	L	L
0, 2, 4, 6 or 8	H	H

### NOTES:

- Conditions shown are for  $\overline{\text{GEN}}/\text{CHK} = \text{L}$ ,  $\overline{\text{OEAB}} = \text{L}$ ,  $\overline{\text{OEBA}} = \text{H}$ .
- A-to-B parity checking is shown. B-to-A is capable of parity checking while A-to-B is performing generation. B-to-A will not generate parity.
- The response shown is for LEAB = H. If LEAB = L then CLKAB will control as an edge triggered clock.
- Conditions shown are for the byte A<sub>0</sub>-A<sub>7</sub>. The byte A<sub>8</sub>-A<sub>15</sub> is similar but will output the parity on PB<sub>2</sub>.
- The error flag  $\overline{\text{PERB}}$  will remain in a high state during parity generation.

2916 tbl 06

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$ ; Military:  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$ 

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current (Input pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
	Input HIGH Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{IL}$	Input LOW Current (Input pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_I = \text{GND}$	—	—	$\pm 1$	
	Input LOW Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{OZH}$	High Impedance Output Current (3-State Output pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_O = 0.5\text{V}$	—	—	$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-80	-140	-225	mA
$V_H$	Input Hysteresis	—		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$		—	5	500	$\mu\text{A}$

2916 Ink 07

**OUTPUT DRIVE CHARACTERISTICS FOR FCT162511T**

Symbol	Parameter		Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_{ODL}$	Output LOW Current	(I/O pins)	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		60	115	200	mA
		(Open Drain)			—	250	—	mA
$I_{ODH}$	Output HIGH Current (I/O pins)		$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		-60	-115	-200	mA
$I_{OFF}$	Output Power Off Leakage Current (Open Drain) <sup>(5)</sup>		$V_{CC} = 0, V_O \leq 5.5\text{V}$		—	—	$\pm 1$	$\mu\text{A}$
$V_{OH}$	Output HIGH Voltage (I/O pins)		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -16\text{mA MIL.}$ $I_{OH} = -24\text{mA COM'L.}$	2.4	3.3	—	V
$V_{OL}$	Output LOW Voltage	(I/O pins)	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 16\text{mA MIL.}$ $I_{OL} = 24\text{mA COM'L.}$	—	0.3	0.55	V
		(Open Drain)		$I_{OL} = 48\text{mA MIL.}$ $I_{OL} = 64\text{mA COM'L.}$	—	0.3	0.55	V

**NOTES:**

2916 tbl 08

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .

**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$	All other Input Pins	—	0.5	1.5	mA
			Parity Input Pins (PAx, PBx)	—	1.0	2.5	
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $\overline{OEAB} = \text{GND}$ , $\overline{OEBA} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	75	120	$\mu\text{A}/\text{MHz}$
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $f_{CP} = 10\text{MHz}$ (CLKAB) 50% Duty Cycle $\overline{OEAB} = \text{GND}$ , $\overline{OEBA} = V_{CC}$ LEAB = GND One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.3	3.2	
		$V_{CC} = \text{Max.}$ , Outputs Open $f_{CP} = 10\text{MHz}$ (CLKAB) 50% Duty Cycle $\overline{OEAB} = \text{GND}$ , $\overline{OEBA} = V_{CC}$ LEAB = GND Eighteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	6.5 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	9.0	21.8 <sup>(5)</sup>	

**NOTES:**

2916 tbl 09

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (PROPAGATION DELAYS)

TYPICAL CHARACTERISTICS OVER OPERATING RANGE (PROPAGATION DELAYS)												
Symbol	Parameter	Condition <sup>(1)</sup>	FCT162511AT				FCT162511CT				Unit	
			Com'l.		Mil.		Com'l.		Mil.			
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.		
tPLH	Propagation Delay, PAx to PBx	CL = 50pF RL = 500Ω	1.5	5.0	1.5	5.3	1.5	4.2	1.5	4.5	ns	
tPHL	Ax to Bx or Bx to Ax, PBx to PAx											
tPLH	Propagation Delay		GEN/CHK LOW Ax to PBx	1.5	7.5	1.5	8.0	1.5	6.5	1.5	6.8	ns
tPHL	Ax to PBx											
tPLH <sup>(3)</sup>	Propagation Delay		Ax to $\overline{\text{PERB}}$ , PAx to $\overline{\text{PERB}}$	1.5	9.0	1.5	9.0	1.5	7.5	1.5	7.8	ns
tPHL	Ax to $\overline{\text{PERB}}$ , PAx to $\overline{\text{PERB}}$			1.5	8.0	1.5	8.0	1.5	6.5	1.5	6.8	
tPLH <sup>(3)</sup>	Propagation Delay		Bx to $\overline{\text{PERA}}$ , PBx to $\overline{\text{PERA}}$	1.5	9.0	1.5	9.0	1.5	7.5	1.5	7.8	ns
tPHL	Bx to $\overline{\text{PERA}}$ , PBx to $\overline{\text{PERA}}$			1.5	8.0	1.5	8.0	1.5	6.5	1.5	6.8	
tPLH	Propagation Delay		LEBA to Ax and PAx LEAB to Bx and PBx	1.5	5.6	1.5	6.0	1.5	5.3	1.5	5.5	ns
tPHL	LEBA to Ax and PAx LEAB to Bx and PBx											
tPLH <sup>(3)</sup>	Propagation Delay		LEBA to $\overline{\text{PERA}}$ , LEAB to $\overline{\text{PERB}}$	1.5	7.0	1.5	7.0	1.5	6.0	1.5	6.3	ns
tPHL	LEBA to $\overline{\text{PERA}}$ , LEAB to $\overline{\text{PERB}}$			1.5	6.0	1.5	6.0	1.5	5.0	1.5	5.3	
tPLH	Propagation Delay		CLKBA to Ax and PAx CLKAB to Bx and PBx	1.5	5.6	1.5	6.0	1.5	5.3	1.5	5.5	ns
tPHL	CLKBA to Ax and PAx CLKAB to Bx and PBx											
tPLH <sup>(3)</sup>	Propagation Delay		CLKBA to $\overline{\text{PERA}}$ CLKAB to $\overline{\text{PERB}}$	1.5	7.0	1.5	7.0	1.5	6.0	1.5	6.3	ns
tPHL	CLKBA to $\overline{\text{PERA}}$ CLKAB to $\overline{\text{PERB}}$			1.5	6.0	1.5	6.0	1.5	5.0	1.5	5.3	
tPZH	Output Enable Time		$\overline{\text{OEBA}}$ to Ax and PAx $\overline{\text{OEAB}}$ to Bx and PBx	1.5	6.0	1.5	6.5	1.5	5.6	1.5	5.8	ns
tPZL	$\overline{\text{OEBA}}$ to Ax and PAx $\overline{\text{OEAB}}$ to Bx and PBx											
tPHZ	Output Disable Time		$\overline{\text{OEBA}}$ to Ax and PAx $\overline{\text{OEAB}}$ to Bx and PBx	1.5	5.6	1.5	6.0	1.5	5.2	1.5	5.5	ns
tPLZ	$\overline{\text{OEBA}}$ to Ax and PAx $\overline{\text{OEAB}}$ to Bx and PBx											
tPLZ <sup>(3)</sup>	Parity ERROR Enable		$\overline{\text{OEBA}}$ to $\overline{\text{PERA}}$ , $\overline{\text{OEAB}}$ to $\overline{\text{PERB}}$	1.5	6.0	1.5	6.3	1.5	6.0	1.5	6.3	ns
tPZL	$\overline{\text{OEBA}}$ to $\overline{\text{PERA}}$ , $\overline{\text{OEAB}}$ to $\overline{\text{PERB}}$			1.5	6.0	1.5	6.3	1.5	6.0	1.5	6.3	
tPLH <sup>(3)</sup>	ODD/ $\overline{\text{EVEN}}$ to $\overline{\text{PERx}}$			1.5	10.0	1.5	10.0	1.5	10.0	1.5	10.0	ns
tPHL				1.5	10.0	1.5	10.0	1.5	10.0	1.5	10.0	
tPLH	ODD/ $\overline{\text{EVEN}}$ to PBx			1.5	10.0	1.5	10.0	1.5	10.0	1.5	10.0	ns
tPHL												

### NOTES:

- See test circuits and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- On Open Drain Outputs tPLH is measured at  $V_{\text{OUT}} = V_{\text{OL}} + 0.3V$ .

2916 tbl 10



## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (SET UP TIMES)

Symbol	Parameter	Test Conditions <sup>(1,3)</sup>			FCT162511AT				FCT162511CT				Unit
					Com'l.		Mil.		Com'l.		Mil.		
					Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tsu	Set-up Time HIGH or LOW Ax to CLKAB	$\overline{\text{GEN}}/\text{CHK}$ LOW	PBx valid	CL = 50pF RL = 500Ω	4	—	4	—	3	—	3.5	—	ns
			PBx not valid		3	—	3	—	3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK}$ HIGH	$\overline{\text{PERB}}$ valid		4	—	4	—	3	—	3	—	ns
			$\overline{\text{PERB}}$ not valid		3	—	3	—	3	—	3	—	ns
tsu	Set-up Time PAx to CLKAB	$\overline{\text{GEN}}/\text{CHK}$ HIGH	$\overline{\text{PERB}}$ valid		4	—	4	—	3	—	3	—	ns
			$\overline{\text{PERB}}$ not valid		3	—	3	—	3	—	3	—	ns
tsu	Set-up Time Bx to CLKBA, PBx to CLKBA		$\overline{\text{PERA}}$ valid		4	—	4	—	3	—	3	—	ns
			$\overline{\text{PERA}}$ not valid		3	—	4	—	3	—	3	—	ns
tsu	Set-up Time Ax to LEAB	CLKAB LOW	PBx valid		3.5	—	3.5	—	3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK}$ LOW	PBx not valid		3	—	3	—	3	—	3	—	ns
		CLKAB LOW	$\overline{\text{PERB}}$ valid		3.5	—	3.5	—	3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK}$ HIGH	$\overline{\text{PERB}}$ not valid		3	—	3	—	3	—	3	—	ns
		CLKAB HIGH	PBx valid		3.5	—	3.5	—	3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK}$ LOW	PBx not valid		3	—	3	—	3	—	3	—	ns
		CLKAB HIGH	$\overline{\text{PERB}}$ valid		3.5	—	3.5	—	3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK}$ HIGH	$\overline{\text{PERB}}$ not valid		3	—	3	—	3	—	3	—	ns
tsu	Set-up Time PAx to LEAB	CLKAB LOW	$\overline{\text{PERB}}$ valid		3.5	—	3.5	—	3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK}$ HIGH	$\overline{\text{PERB}}$ not valid		3	—	3	—	3	—	3	—	ns
		CLKAB HIGH	$\overline{\text{PERB}}$ valid		3.5	—	3.5	—	3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK}$ HIGH	$\overline{\text{PERB}}$ not valid		3	—	3	—	3	—	3	—	ns
tsu	Set-up Time Bx to LEBA PBx to LEBA	CLKBA LOW	$\overline{\text{PERA}}$ valid		3.5	—	3.5	—	3	—	3	—	ns
			$\overline{\text{PERA}}$ not valid		3	—	3	—	3	—	3	—	ns
		CLKBA HIGH	$\overline{\text{PERA}}$ valid		3.5	—	3.5	—	3	—	3	—	ns
			$\overline{\text{PERA}}$ not valid		3	—	3	—	3	—	3	—	ns
tsk(O)	Output Skew <sup>(4)</sup>				—	0.5	—	0.5	—	0.5	—	0.5	ns

2916 tbl 11

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (HOLD TIMES)

Symbol	Parameter	Condition <sup>(1)</sup>	FCT162511AT				FCT162511CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
th	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA	CL = 50pF RL = 500Ω	1	—	1	—	1	—	1	—	ns
th	Hold Time HIGH or LOW PAx to LEAB		1	—	1	—	1	—	1	—	ns
th	Hold Time HIGH or LOW PBx to LEBA		1	—	1	—	1	—	1	—	ns
th	Hold Time Ax to CLKAB, PAx to CLKAB		1	—	1	—	0	—	0	—	ns
th	Hold Time Bx to CLKBA, PBx to CLKBA		1	—	1	—	0	—	0	—	ns
tw	LEAB or LEBA Pulse Width HIGH <sup>(2)</sup>		3	—	3	—	3	—	3	—	ns
tw	CLKAB or CLKBA Pulse Width HIGH or LOW <sup>(2)</sup>		3	—	3	—	3	—	3	—	ns

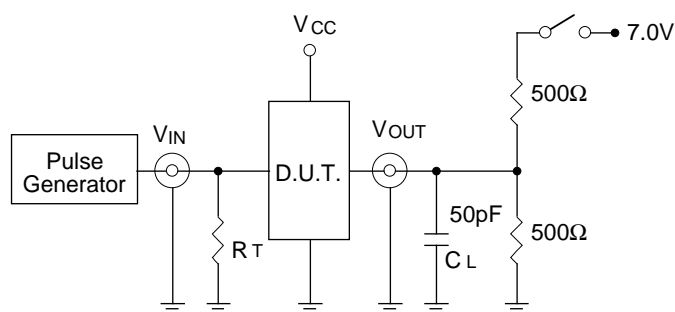
### NOTES:

2916 tbl 12

- See test circuits and waveforms.
- This parameter is guaranteed but not tested.
- "Not valid" means the set-up time indicated is not sufficient to assure proper functioning of this output; however, the set-up time indicated will assure proper functioning of the A to B or B to A port respective to the indicated direction.
- Skew between any two outputs of the same package, switching in the same direction, excluding  $\overline{\text{PERx}}$  in clocked mode, and Pxx (parity bits) and  $\overline{\text{PERx}}$  in transparent/latched mode. This parameter is guaranteed by design.

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



2916 drw 05

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

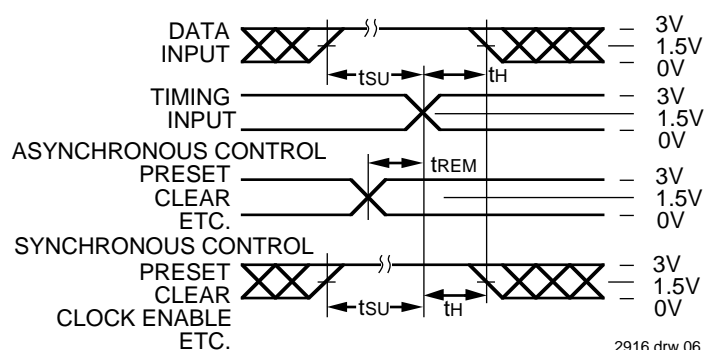
#### DEFINITIONS:

$C_L$  = Load capacitance: includes jig and probe capacitance.

$R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

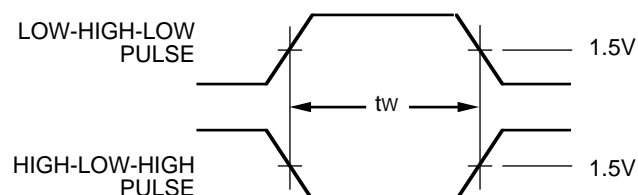
2916 lmk 13

### SET-UP, HOLD AND RELEASE TIMES



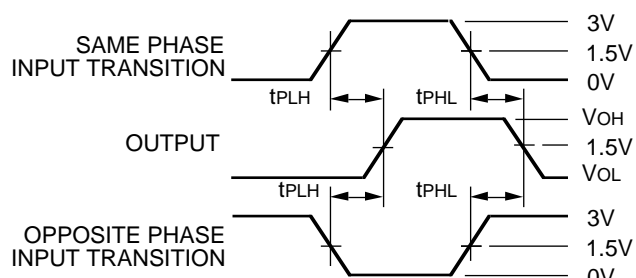
2916 drw 06

### PULSE WIDTH



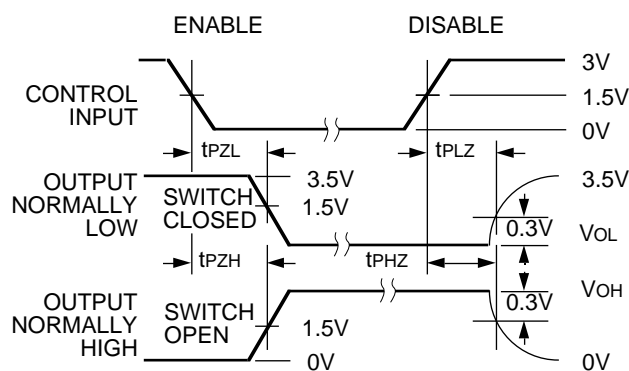
2916 drw 07

### PROPAGATION DELAY



2916 drw 08

### ENABLE AND DISABLE TIMES



2916 drw 09

#### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$

ORDERING INFORMATION

IDT	X	FCT	XXXX	X	X		
	Temperature Range		Device Type	Package	Process		
						Blank	Commercial
						B	MIL-STD-883, Class B
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
						E	CERPACK (E56-1)
						162511AT	16-Bit Registered Transceiver with Parity
						162511CT	
						54	−55°C to +125°C
						74	−40°C to +85°C

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