



Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTERS (3-STATE)

IDT54/74FCT374/A/C
IDT54/74FCT534/A/C
IDT54/74FCT574/A/C

FEATURES:

- IDT54/74FCT374/534/574 equivalent to FAST™ speed and drive
- **IDT54/74FCT374A/534A/574A up to 30% faster than FAST**
- **IDT54/74FCT374C/534C/574C up to 50% faster than FAST**
- IOL = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Edge triggered master/slave, D-type flip-flops
- Buffered common clock and buffered common three-state control
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meets or exceeds JEDEC Standard 18 specifications

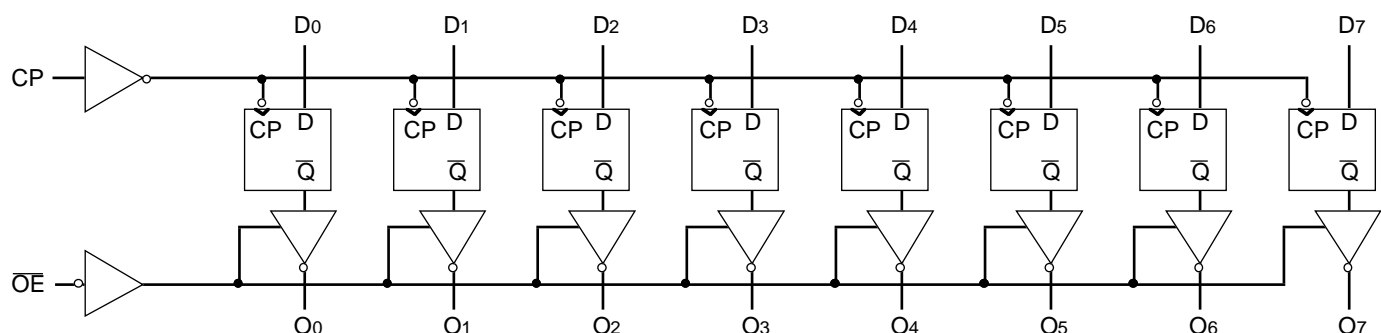
DESCRIPTION:

The IDT54/74FCT374/A/C, IDT54/74FCT534/A/C and IDT54/74FCT574/A/C are 8-bit registers built using an advanced dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output enable (OE) is LOW, the eight outputs are enabled. When the OE input is HIGH, the outputs are in the high-impedance state.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

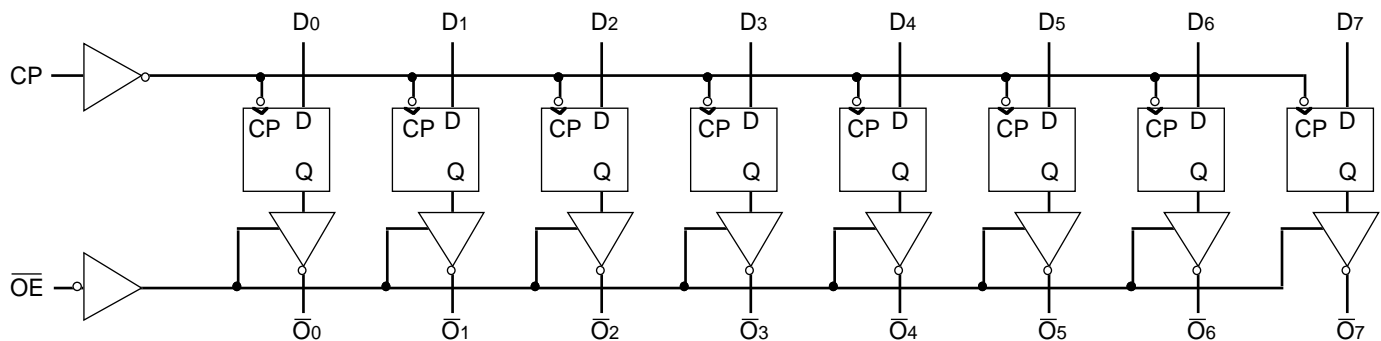
The IDT54/74FCT374/A/C and IDT54/74FCT574/A/C have non-inverting outputs with respect to the data at the D inputs. The IDT54/74FCT534/A/C have inverting outputs.

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT374 AND IDT54/74FCT574



2603 cnv* 01

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT534



2603 cnv* 02

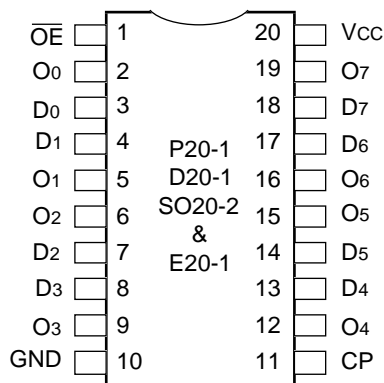
The IDT logo is a registered trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1992

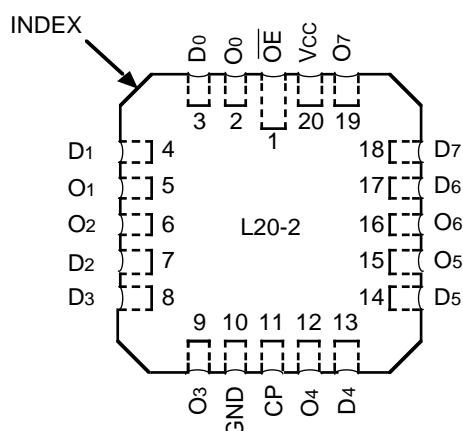
PIN CONFIGURATIONS

IDT54/74FCT374



DIP/SOIC/CERPACK
TOP VIEW

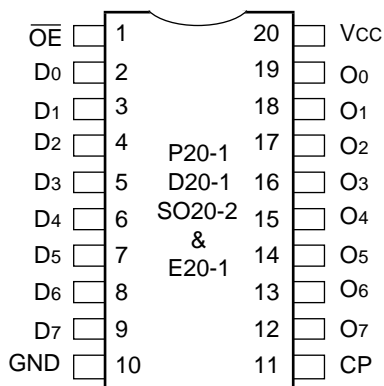
2603 cnv* 03



LCC
TOP VIEW

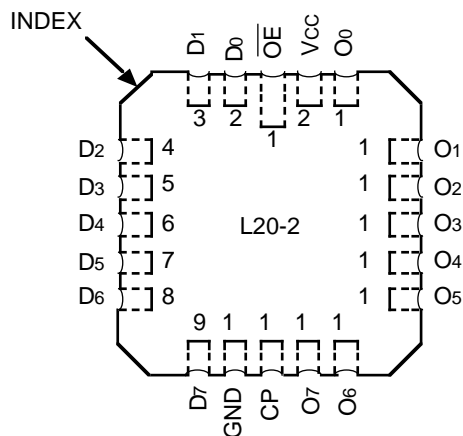
2603 cnv* 04

IDT54/74FCT574



DIP/SOIC/CERPACK
TOP VIEW

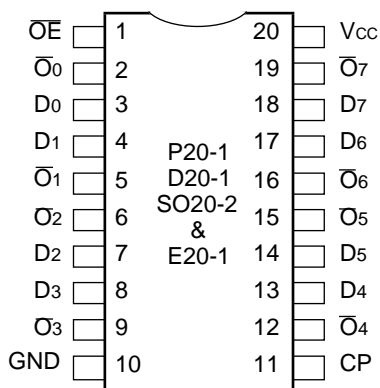
2603 cnv* 05



LCC
TOP VIEW

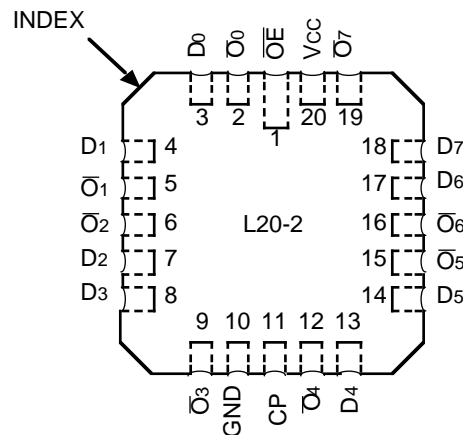
2603 cnv* 06

IDT54/74FCT534



DIP/SOIC/CERPACK
TOP VIEW

2603 cnv* 07



LCC
TOP VIEW

2603 cnv* 08

PIN DESCRIPTION

Pin Names	Description
DN	D flip-flop data inputs.
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition.
ON	3-state outputs, (true).
$\overline{\text{ON}}$	3-state outputs, (inverted).
$\overline{\text{OE}}$	Active LOW 3-state Output Enable input.

2603 tbl 06

FUNCTION TABLE⁽¹⁾

Function	Inputs			FCT534		FCT374/574	
				Outputs	Internal	Outputs	Internal
	$\overline{\text{OE}}$	CP	DN	$\overline{\text{ON}}$	QN	ON	$\overline{\text{QN}}$
Hi-Z	H	L	X	Z	NC	Z	NC
	H	H	X	Z	NC	Z	NC
Load Register	L	\nearrow	L	H	L	L	H
	L	\nearrow	H	L	H	H	L
	H	\nearrow	L	Z	L	Z	H
	H	\nearrow	H	Z	H	Z	L

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Z = High Impedance
NC = No Change
 \nearrow = LOW-to-HIGH transition

2603 tbl 05

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
TA	Operating Temperature	0 to +70	−55 to +125	°C
TBIAS	Temperature Under Bias	−55 to +125	−65 to +135	°C
TSTG	Storage Temperature	−55 to +125	−65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES:

2603 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

NOTE:

2603 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55^{\circ}C$ to $+125^{\circ}C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	5	μA
			$V_I = 2.7V$	—	—	5 ⁽⁴⁾	
I_{IL}	Input LOW Current		$V_I = 0.5V$	—	—	-5 ⁽⁴⁾	
			$V_I = GND$	—	—	-5	
I_{OZH}	Off State (High Impedance) Output Current	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	10	μA
			$V_O = 2.7V$	—	—	10 ⁽⁴⁾	
I_{OZL}			$V_O = 0.5V$	—	—	-10 ⁽⁴⁾	
			$V_O = GND$	—	—	-10	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_N = -18mA$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$ ⁽³⁾ , $V_O = GND$		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V$, $V_{IN} = V_{LC}$ or V_{HC} , $I_{OH} = -32\mu A$		V_{HC}	V_{CC}	—	V
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}	—	
			$I_{OH} = -12mA \text{ MIL.}$	2.4	4.3	—	
			$I_{OH} = -15mA \text{ COM'L.}$	2.4	4.3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 3V$, $V_{IN} = V_{LC}$ or V_{HC} , $I_{OL} = 300\mu A$		—	GND	V_{LC}	V
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 300\mu A$	—	GND	V_{LC} ⁽⁴⁾	
			$I_{OL} = 32mA \text{ MIL.}$	—	0.3	0.5	
			$I_{OL} = 48mA \text{ COM'L.}$	—	0.3	0.5	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^{\circ}C$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

2603 tbl 03

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ $f_i = 5\text{MHz}$ 50% Duty Cycle One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2.2	6.0	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ Eight Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.2	16.8 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
All currents are in milliamps and all frequencies are in megahertz.

2603 tbl 04

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions ⁽¹⁾	FCT374/534/574				FCT374A/534A/574A				FCT374C/534C/574C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay CP to ON ⁽³⁾	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	2.0	5.2	2.0	6.2	ns
tPZH tPZL	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.2	ns
tpHZ tPLZ	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.7	ns
tsU	Set-up Time HIGH or LOW, DN to CP		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, DN to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

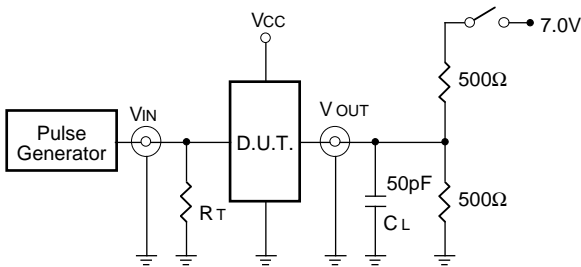
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. ON for FCT374 and FCT574, ON for FCT534.

2603 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



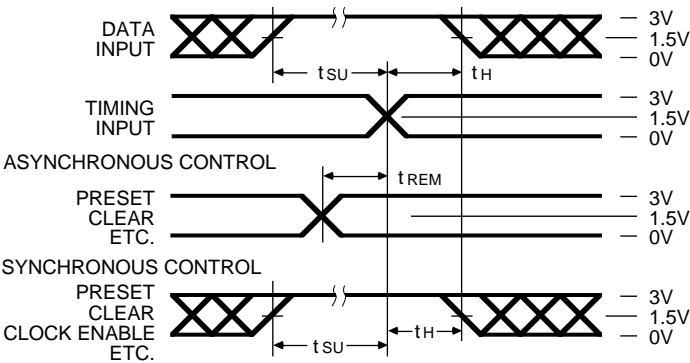
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

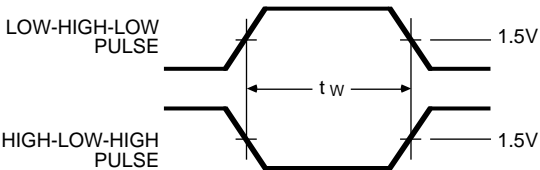
DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

2603 tbl 08

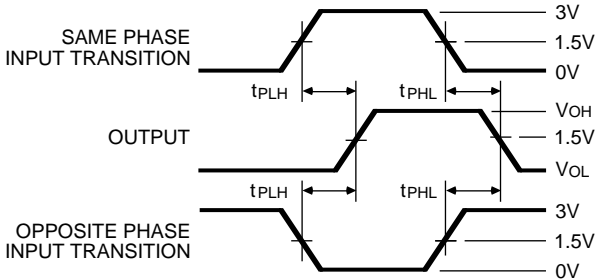
SET-UP, HOLD AND RELEASE TIMES



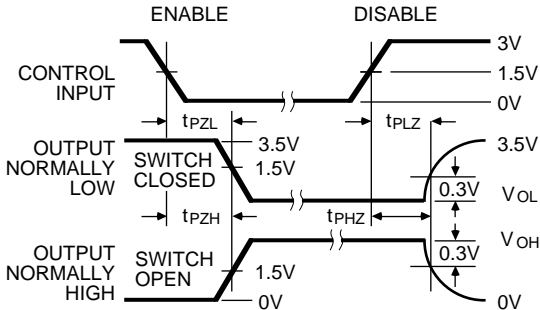
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



- NOTES**
- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
 - Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; tr ≤ 2.5ns; tr ≤ 2.5ns.

2603 drw 15

ORDERING INFORMATION

IDT	XX	FCT	XXXX	X	X	
	Temp. Range		Device Type	Package	Process	
						Blank
						B
						P
						D
						SO
						L
						E
						374
						574
						534
						374A
						574A
						534A
						374C
						574C
						534C
						54
						74

2603 cnv* 14