



## LOW SKEW PLL CLOCK DRIVER TURBOCLOCK™ JR.

**IDT59920A**

### FEATURES:

- Eight zero delay outputs
- Selectable positive or negative edge synchronization
- Synchronous output enable
- Output frequency: 15MHz to 100MHz
- CMOS outputs
- 3 skew grades:
  - IDT59920A-2:  $t_{\text{SKEW0}} < 250\text{ps}$
  - IDT59920A-5:  $t_{\text{SKEW0}} < 500\text{ps}$
  - IDT59920A-7:  $t_{\text{SKEW0}} < 750\text{ps}$
- 3-level inputs for PLL range control
- PLL bypass for DC testing
- External feedback, internal loop filter
- 46mA IoL high drive outputs
- Low Jitter:  $< 200\text{ps}$  peak-to-peak
- Outputs drive  $50\Omega$  terminated lines
- Pin-compatible with Cypress CY7B9920
- Available in SOIC package

### DESCRIPTION:

The IDT59920A is a high fanout phase lock loop clock driver intended for high performance computing and data-communications applications. The IDT59920A has CMOS outputs.

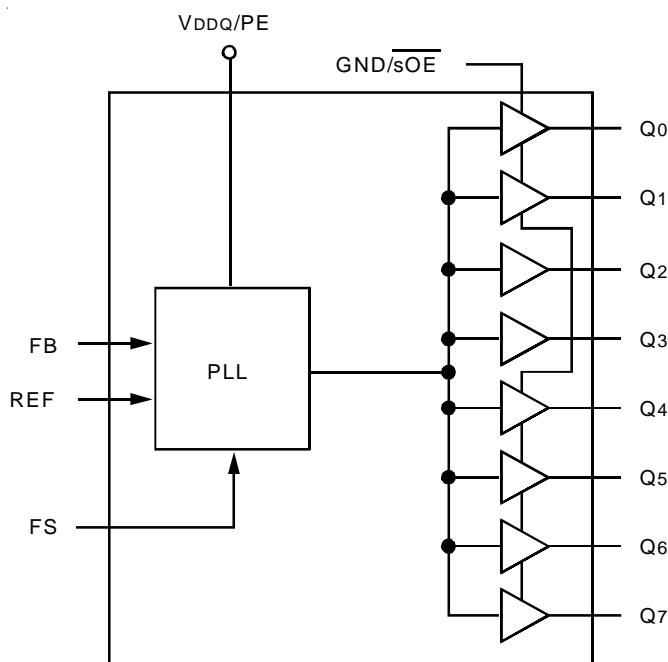
The IDT59920A maintains Cypress CY7B9920 compatibility while providing two additional features: Synchronous Output Enable ( $\text{GND}/\overline{\text{sOE}}$ ), and Positive/Negative Edge Synchronization ( $\text{VDDQ}/\text{PE}$ ). When the  $\text{GND}/\overline{\text{sOE}}$  pin is held low, all outputs are synchronously enabled (CY7B9920 compatibility). However, if  $\text{GND}/\overline{\text{sOE}}$  is held high, all outputs except Q2 and Q3 are synchronously disabled.

Furthermore, when the  $\text{VDDQ}/\text{PE}$  is held high, all outputs are synchronized with the positive edge of the REF clock input (CY7B9920 compatibility). When  $\text{VDDQ}/\text{PE}$  is held low, all outputs are synchronized with the negative edge of REF.

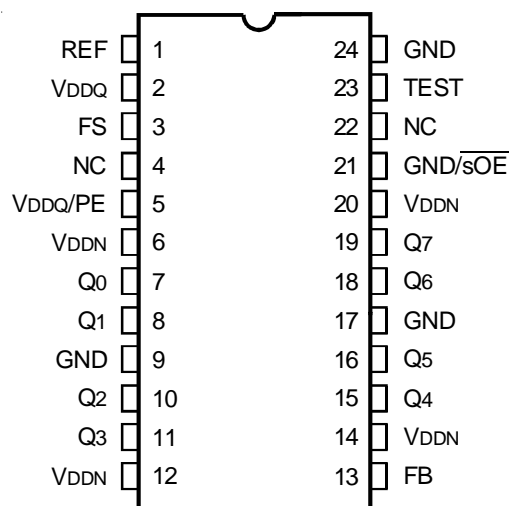
The FB signal is compared with the input REF signal at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly.

An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SOIC  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
	Supply Voltage to Ground	-0.5 to +7	V
V <sub>I</sub>	DC Input Voltage	-0.5 to +7	V
	Maximum Power Dissipation (T <sub>A</sub> = 85°C)	530	mW
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C

### NOTE:

- Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1MHz, V<sub>IN</sub> = 0V)

Parameter	Description	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	5	7	pF

### NOTE:

- Capacitance applies to all inputs except TEST and FS. It is characterized but not production tested.

## PIN DESCRIPTION

Pin Name	Type	Description
REF	IN	Reference Clock Input
FB	IN	Feedback Input
TEST <sup>(1)</sup>	IN	When MID or HIGH, disables PLL (except for conditions of Note 1). REF goes to all outputs. Set LOW for normal operation.
GND/ $\overline{\text{sOE}}$ <sup>(1)</sup>	IN	Synchronous Output Enable. When HIGH, it stops clock outputs (except Q2 and Q3) in a LOW state - Q2 and Q3 may be used as the feedback signal to maintain phase lock. Set GND/ $\overline{\text{sOE}}$ LOW for normal operation.
VDDQ/PE	IN	Selectable positive or negative edge control. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock.
FS <sup>(2)</sup>	IN	Frequency range select. 3 level input. FS = GND: 15 to 35MHz FS = MID (or open): 25 to 60MHz FS = VDD: 40 to 100MHz
Q0 - Q7	OUT	Eight clock output
VDDN	PWR	Power supply for output buffers
VDDQ	PWR	Power supply for phase locked loop and other internal circuitry
GND	PWR	Ground

### NOTES:

- When TEST = MID and GND/ $\overline{\text{sOE}}$  = HIGH, PLL remains active.
- This input is wired to VDD, GND, or unconnected. Default is MID level. If it is switched in the real time mode, the outputs may glitch, and the PLL may require an additional lock time before all data sheet limits are achieved.

## RECOMMENDED OPERATING RANGE

Symbol	Description	IDT59920A-5, -7 (Industrial)		IDT59920A-2 (Commercial)		Unit
		Min.	Max.	Min.	Max.	
V <sub>DD</sub>	Power Supply Voltage	4.5	5.5	4.75	5.25	V
T <sub>A</sub>	Ambient Operating Temperature	-40	+85	0	+70	°C

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions	Min.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Logic HIGH (REF, FB Inputs Only)	V <sub>DD</sub> −1.35	—	V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Logic LOW (REF, FB Inputs Only)	—	1.35	V
V <sub>IHH</sub>	Input HIGH Voltage <sup>(1)</sup>	3-Level Inputs Only	V <sub>DD</sub> −1	—	V
V <sub>IMM</sub>	Input MID Voltage <sup>(1)</sup>	3-Level Inputs Only	V <sub>DD</sub> /2−0.5	V <sub>DD</sub> /2+0.5	V
V <sub>ILL</sub>	Input LOW Voltage <sup>(1)</sup>	3-Level Inputs Only	—	1	V
I <sub>IN</sub>	Input Leakage Current (REF, FB Inputs Only)	V <sub>IN</sub> = V <sub>DD</sub> or GND V <sub>DD</sub> = Max.	—	±5	μA
I <sub>3</sub>	3-Level Input DC Current (TEST, FS)	V <sub>IN</sub> = V <sub>DD</sub> HIGH Level	—	±200	μA
		V <sub>IN</sub> = V <sub>DD</sub> /2      MID Level	—	±50	
		V <sub>IN</sub> = GND      LOW Level	—	±200	
I <sub>PU</sub>	Input Pull-Up Current (V <sub>DDO</sub> /PE)	V <sub>DD</sub> = Max., V <sub>IN</sub> = GND	—	±100	μA
I <sub>PD</sub>	Input Pull-Down Current (GND/sO <sub>E</sub> )	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>DD</sub>	—	±100	μA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = −16mA	—	—	V
		V <sub>DD</sub> = Min., I <sub>OH</sub> = −40mA	V <sub>DD</sub> −0.75	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 46mA	—	0.45	V
I <sub>OS</sub>	Output Short Circuit Current <sup>(2)</sup>	V <sub>DD</sub> = Max., V <sub>O</sub> = GND	—	N/A	mA

### NOTES:

- These inputs are normally wired to V<sub>DD</sub>, GND, or unconnected. Internal termination resistors bias unconnected inputs to V<sub>DD</sub>/2. If these inputs are switched, the function and timing of the outputs may be glitched, and the PLL may require an additional lock time before all datasheet limits are achieved.
- Outputs are not to be shorted.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Typ.	Max.	Unit
I <sub>DDQ</sub>	Quiescent Power Supply Current	V <sub>DD</sub> = Max., TEST = MID, REF = LOW, GND/sO <sub>E</sub> = LOW, All outputs unloaded	10	40	mA
ΔI <sub>DD</sub>	Power Supply Current per Input HIGH	V <sub>DD</sub> = Max., V <sub>IN</sub> = 3.4V	0.4	1.5	mA
I <sub>DDO</sub>	Dynamic Power Supply Current per Output	V <sub>DD</sub> = Max., C <sub>L</sub> = 0pF	100	160	μA/MHz
I <sub>TOT</sub>	Total Power Supply Current	V <sub>DD</sub> = 5V, F <sub>REF</sub> = 25MHz, C <sub>L</sub> = 240pF <sup>(1)</sup>	53	—	mA
		V <sub>DD</sub> = 5V, F <sub>REF</sub> = 33MHz, C <sub>L</sub> = 240pF <sup>(1)</sup>	63	—	
		V <sub>DD</sub> = 5V, F <sub>REF</sub> = 66MHz, C <sub>L</sub> = 240pF <sup>(1)</sup>	117	—	

### NOTE:

- For eight outputs, each loaded with 30pF.

## INPUT TIMING REQUIREMENTS

Symbol	Description <sup>(1)</sup>	Min.	Max.	Unit
t <sub>R</sub> , t <sub>F</sub>	Maximum input rise and fall times, 0.8V to 2V	—	10	ns/V
t <sub>PWC</sub>	Input clock pulse, HIGH or LOW	3	—	ns
D <sub>H</sub>	Input duty cycle	10	90	%
REF	Reference Clock Input	15	100	MHz

### NOTE:

- Where pulse width implied by D<sub>H</sub> is less than t<sub>PWC</sub> limit, t<sub>PWC</sub> limit applies.

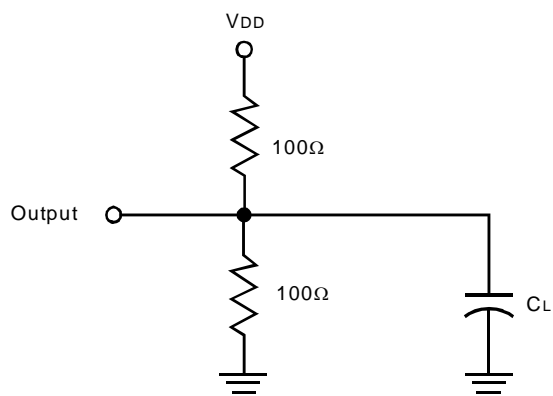
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter		IDT59920A-2			IDT59920A-5			IDT59920A-7			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
F <sub>REF</sub>	REF Frequency Range	FS = LOW	15	—	35	15	—	35	15	—	35	MHz
		FS = MED	25	—	60	25	—	60	25	—	60	
		FS = HIGH	40	—	100	40	—	100	40	—	100	
t <sub>RPWH</sub>	REF Pulse Width HIGH <sup>(1,8)</sup>		3	—	—	3	—	—	3	—	—	ns
t <sub>RPWL</sub>	REF Pulse Width LOW <sup>(1,8)</sup>		3	—	—	3	—	—	3	—	—	ns
t <sub>SKEW0</sub>	Zero Output Skew (All Outputs) <sup>(1,3,4)</sup>		—	0.1	0.25	—	0.25	0.5	—	0.3	0.75	ns
t <sub>DEV</sub>	Device-to-Device Skew <sup>(1,2,5)</sup>		—	—	0.75	—	—	1.25	—	—	1.65	ns
t <sub>PD</sub>	REF Input to FB Propagation Delay <sup>(1,7)</sup>		−0.25	0	0.25	−0.5	0	0.5	−0.7	0	0.7	ns
t <sub>ODCV</sub>	Output Duty Cycle Variation from 50% <sup>(1)</sup>		−0.5	0	0.5	−1.2	0	1.2	−1.5	0	1.5	ns
t <sub>ORISE</sub>	Output Rise Time <sup>(1)</sup>		0.5	2	2.5	0.5	2	3.5	0.5	3	5	ns
t <sub>OFALL</sub>	Output Fall Time <sup>(1)</sup>		0.5	2	2.5	0.5	2	3.5	0.5	3	5	ns
t <sub>LOCK</sub>	PLL Lock Time <sup>(1,6)</sup>		—	—	0.5	—	—	0.5	—	—	0.5	ms
t <sub>JR</sub>	Cycle-to-Cycle Output Jitter <sup>(1)</sup>	RMS	—	—	25	—	—	25	—	—	25	ps
		Peak-to-Peak	—	—	200	—	—	200	—	—	200	

### NOTES:

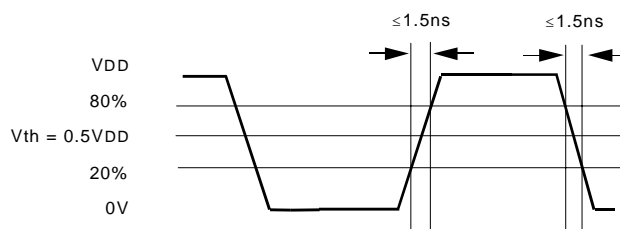
- All timing and jitter tolerances apply for F<sub>NOM</sub> ≥ 25MHz. Guaranteed by design and characterization, not subject to production testing.
- Skew is the time between the earliest and the latest output transition among all outputs with the specified load.
- t<sub>SKEW</sub> is the skew between all outlets. See AC TEST LOADS.
- For IDT59920A-2 t<sub>SKEW0</sub> is measured with C<sub>L</sub> = 0pF; for C<sub>L</sub> = 30pF, t<sub>SKEW0</sub> = 0.45ns Max.
- t<sub>DEV</sub> is the output-to-output skew between any two devices operating under the same conditions (V<sub>DD</sub>, ambient temperature, air flow, etc.)
- t<sub>LOCK</sub> is the time that is required before synchronization is achieved. This specification is valid only after V<sub>DD</sub> is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t<sub>PD</sub> is within specified limits.
- t<sub>PD</sub> is measured with REF input rise and fall times (from 0.2V<sub>DD</sub> to 0.8V<sub>DD</sub>) of 1.5ns.
- Refer to INPUT TIMING REQUIREMENTS for more detail.

## AC TEST LOADS AND WAVEFORMS

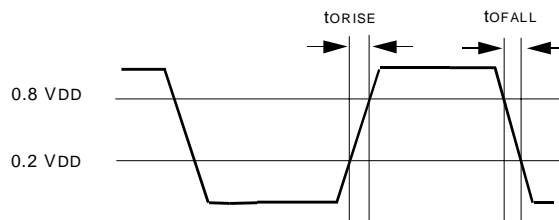


$C_L = 50\text{pF}$  ( $C_L = 30\text{pF}$  for -2 and -5 devices)

*Test Load*

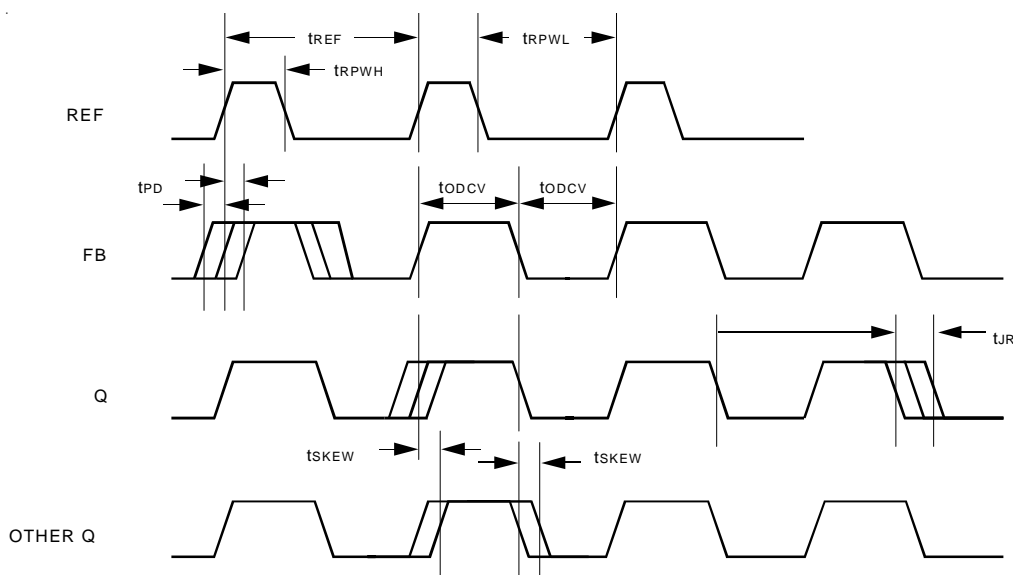


*CMOS Input Test Waveform*



*CMOS Output Waveform*

## AC TIMING DIAGRAM



### NOTES:

- Skew: The time between the earliest and the latest output transition among all outputs when all are loaded with 50pF (30pF for -2 and -5) and terminated with  $V_{DD}/2$ .
- tsKEW: The skew between all outputs.
- tDEV: The output-to-output skew between any two devices operating under the same conditions ( $V_{DD}$ , ambient temperature, air flow, etc.)
- tODCV: The deviation of the output from a 50% duty cycle.
- tORISE and tOFALL are measured between  $0.2V_{DD}$  and  $0.8V_{DD}$ .
- tLOCK: The time that is required before synchronization is achieved. This specification is valid only after  $V_{DD}$  is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until tPD is within specified limits.

## ORDERING INFORMATION

IDT	XXXXX	XX	X		
Device Type	Package	Process			
			Blank	Commercial (0°C to +70°C)	
			I	Industrial (-40°C to +85°C)	
			SO	Small Outline IC (300-mil)	
			59920A-2	Low Skew PLL Clock Driver TurboClock Jr.	
			59920A-5		
			59920A-7		



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