



PRECISION CLOCK GENERATOR OC-48 APPLICATIONS

IDT5T929

FEATURES:

- **Input frequency:**
 - For SONET non-FEC: 19.44MHz, 38.88MHz, 77.76MHz, 155.52MHz, 311.04MHz, or 622.08MHz
 - For SONET FEC: 20.83MHz, 41.66MHz, 83.31MHz, 166.63MHz, 333.26MHz, or 666.52MHz
 - For 10GE copper: 19.53MHz, 39.06MHz, 78.125MHz, 156.25MHz, 312.5MHz, or 625MHz
 - For 10GE optical: 20.14MHz, 40.28MHz, 80.56MHz, 161.13MHz, 322.26MHz, or 644.53MHz
- **Output frequency range selection**
- **1x, 2x, 4x, 8x, 16x, and 32x outputs on Q_{OUT}**
- **Regenerated input clock on Q_{REG}**
- **Lock indicator**
- **Power-down mode**
- **LVPECL or LVDS outputs**
- **Two modes of output frequency range**
 - Mode 0: Q_{OUT} range 155.5 - 166.6MHz. Q_{REG} is a regenerated version of the input clock.
 - Mode 1: Q_{OUT} range 622 - 666.5MHz. Q_{REG} is a regenerated version of the input clock frequency.
- **Hitless switchover**
- **Differential LVPECL, LVDS, or single-ended LVTTTL input interface**
- **2.375 - 3.465V core and I/O**
- **Available in VFQFPN package**

DESCRIPTION:

The IDT5T929 generates a high precision FEC (Forward Error Correction) or non-FEC source clock for SONET/SDH systems as well as a source clock for Gigabit Ethernet systems. This device also has clock regeneration capability: it creates a "clean" version of the clock input by using the internal oscillator to square the input clock's rising and falling edges and remove jitter. In the event that the main clock input fails, the device automatically locks to a backup reference clock using a hitless switchover mechanism.

This device detects loss of valid CLKIN and leaves the VCO of the PLL at the last valid frequency while an alternate input REFIN is selected. If CLKIN and REFIN are different frequencies, the multiplication factor will be adjusted to retain the same output frequency.

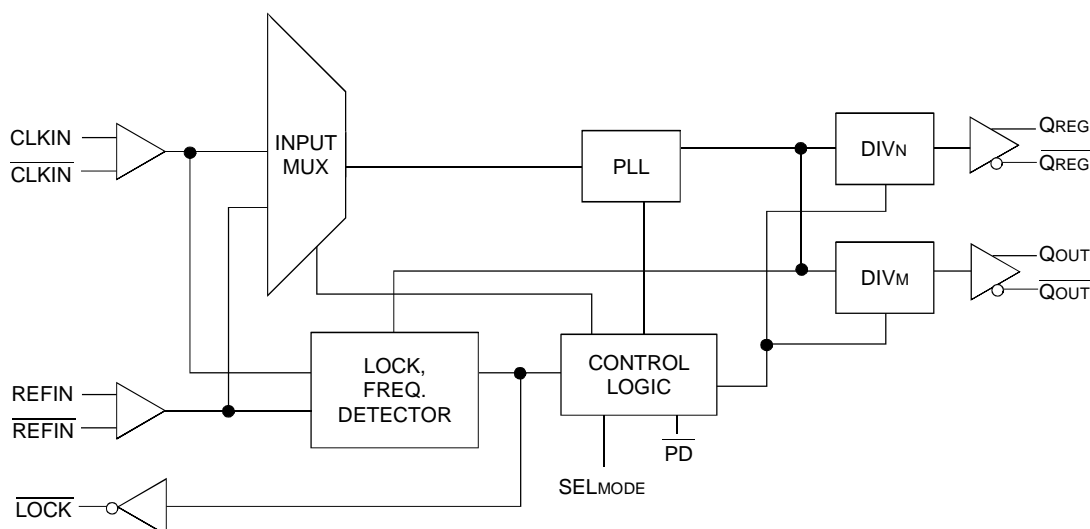
The IDT5T929 can act as a translator from a differential LVPECL, LVDS, or single-ended LVTTTL input to LVPECL or LVDS outputs. The IDT5T929-10 has LVDS outputs and the IDT5T929-30 has LVPECL outputs.

The two modes of output frequency range are controlled by the SELmode. When SELmode is high or low, the Q_{OUT} is a multiplied version of the input clock while Q_{REG} is a regenerated version of the input clock.

APPLICATIONS:

- Terabit routers
- Gigabit ethernet systems
- SONET / SDH systems
- Digital cross connects
- Optical transceiver modules

FUNCTIONAL BLOCK DIAGRAM

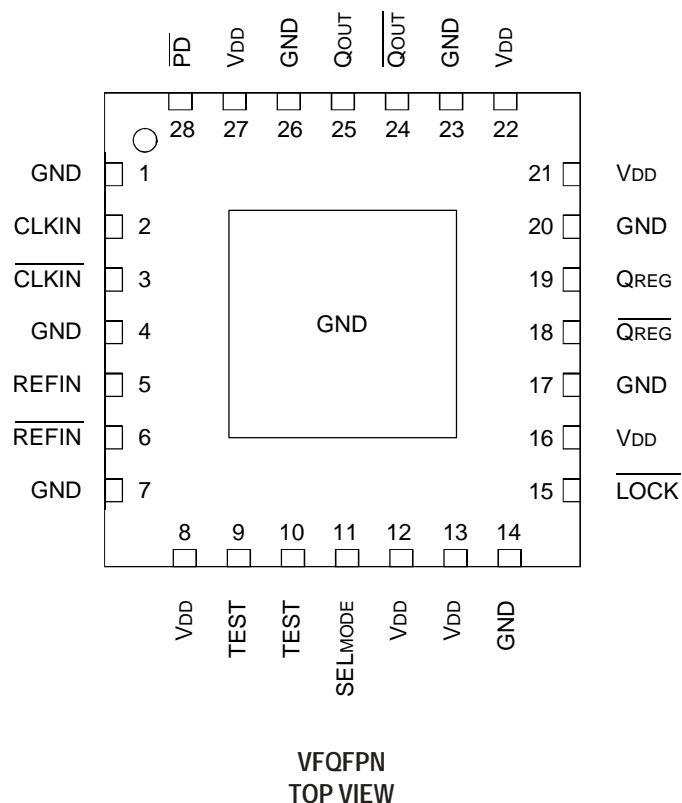


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INDUSTRIAL TEMPERATURE RANGE

JANUARY 2004

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|------------------|----------------------|------------------------------|------|
| V _{DD} | Power Supply Voltage | −0.5 to +4.1 | V |
| V _I | Input Voltage | −0.5 to +4.1 | V |
| V _O | Output Voltage | −0.5 to V _{DD} +0.5 | V |
| T _J | Junction Temperature | 150 | °C |
| T _{STG} | Storage Temperature | −65 to +165 | °C |

NOTE:

- Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{IN} = 0V)

| Parameter | Description | Typ. | Max. | Unit |
|------------------|--------------------|------|------|------|
| C _{IN} | Input Capacitance | 2.5 | 3 | pF |
| C _{OUT} | Output Capacitance | — | — | pF |

NOTE:

- Capacitance applies to all inputs except SELmode.

RECOMMENDED OPERATING RANGE

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|-------|---------------------|-------|------|
| T _A | Ambient Operating Temperature | −40 | +25 | +85 | °C |
| V _{DD} | Power Supply Voltage | 2.375 | — | 3.465 | V |
| V _T | Termination Voltage (LVPECL) | — | V _{DD} − 2 | — | V |
| | Termination Voltage (LVDS) | — | 1.2 | — | |

INPUT FREQUENCY RANGE⁽¹⁾

| |
|-------------------|
| 19.4MHz - 20.9MHz |
| 38.8MHz - 41.7MHz |
| 77.7MHz - 83.4MHz |
| 155.5MHz - 167MHz |
| 311MHz - 334MHz |
| 622MHz - 667MHz |

NOTE:

1. The PLL will automatically detect the input frequency and adjust the multiply ratio to generate the appropriate output frequency.

LOCK FREQUENCY DETECTOR

The 5T929 will lock to, and track, a valid CLKIN signal; $\overline{\text{LOCK}}$ will be low when this has occurred. If CLKIN fails, the 5T929 PLL will smoothly switch to lock to REFIN without generating any glitches on the output. The fact that the PLL is locked to REFIN rather than CLKIN is indicated by a high state on $\overline{\text{LOCK}}$. When a valid input is then applied to CLKIN, the 5T929 will smoothly switch back to locking on CLKIN, and $\overline{\text{LOCK}}$ will go low. $\overline{\text{LOCK}}$ will also switch to high should the frequency of CLKIN drift close to the limits of the VCO tuning range.

OUTPUT FREQUENCY RANGE

| SELmode | QOUT/ $\overline{\text{QOUT}}$ | QREG/ $\overline{\text{QREG}}$ | Unit |
|---------|--------------------------------|--|------|
| L | 155.5 - 166.6 | regenerated CLKIN/ $\overline{\text{CLKIN}}$ | MHz |
| H | 622 - 666.5 | regenerated CLKIN/ $\overline{\text{CLKIN}}$ | MHz |

PIN DESCRIPTION

| Pin Name | I/O | Type | Description |
|----------------------------------|-----|---------------------------|---|
| CLKIN, $\overline{\text{CLKIN}}$ | I | Adjustable ⁽¹⁾ | Differential or single-ended clock input signal. For differential, LVPECL or LVDS supported. If left open-circuited, inputs will float to LVTTTL threshold voltage so that either input may be used as a single-ended input. A capacitor to ground should be connected on the floating input. |
| REFIN, $\overline{\text{REFIN}}$ | I | Adjustable ⁽¹⁾ | Differential reference clock input. The reference clock input is used as an input to the PLL when CLKIN/ $\overline{\text{CLKIN}}$ fails. Differential or single-ended clock input signal. For differential, LVPECL or LVDS supported. If left open-circuited, inputs will float to LVTTTL threshold voltage so that either input may be used as a single-ended input. A capacitor to ground should be connected on the floating input. |
| SELmode | I | 2-level ⁽²⁾ | 2 level input to select output frequency range for QOUT/ $\overline{\text{QOUT}}$ and QREG/ $\overline{\text{QREG}}$ (see Output Frequency Range table) |
| $\overline{\text{PD}}$ | I | LVTTTL | Power Down Control. Shuts off entire chip when LOW. |
| QOUT, $\overline{\text{QOUT}}$ | O | Adjustable ⁽³⁾ | Differential clock output. LVPECL or LVDS outputs. |
| QREG, $\overline{\text{QREG}}$ | O | Adjustable ⁽³⁾ | Regenerated clock output from CLKIN/ $\overline{\text{CLKIN}}$, LVPECL, or LVDS outputs. |
| $\overline{\text{LOCK}}$ | O | LVTTTL | LOW when PLL is locked to CLKIN, HIGH in all other conditions |
| TEST | | | Factory testing only. This pin should be left unconnected. |
| NC | | | No connection |
| VDD | | PWR | Power Supply |
| GND | | PWR | Ground |

NOTES:

1. Inputs are capable of translating the following interface standards:
Single-ended 3.3V LVTTTL levels
Single-ended 2.5V LVTTTL levels
Differential LVPECL levels
Differential LVDS levels
2. 2-level inputs are static inputs and must be tied to VDD or GND.
3. Outputs can be LVPECL or LVDS.

CLOCK INPUT/OUTPUT CONFIGURATION DESCRIPTION

| Application | REFIN (MHz) | CKIN (MHz) | SELmode | QREG (MHz) | QOUT (MHz) |
|--------------|---|------------|---------|------------|------------|
| Non-FEC | 19.44, 38.88, 77.76, 155.52, 311.04, 622.08 | 19.44 | LOW | 19.44 | 155.52 |
| | | | HIGH | 19.44 | 622.08 |
| | | 38.88 | LOW | 38.88 | 155.52 |
| | | | HIGH | 38.88 | 622.08 |
| | | 77.76 | LOW | 77.76 | 155.52 |
| | | | HIGH | 77.76 | 622.08 |
| | | 155.52 | LOW | 155.52 | 155.52 |
| | | | HIGH | 155.52 | 622.08 |
| | | 311.04 | LOW | 311.04 | 155.52 |
| | | | HIGH | 311.04 | 622.08 |
| | | 622.08 | LOW | 622.08 | 155.52 |
| | | | HIGH | 622.08 | 622.08 |
| FEC | 20.83, 41.66, 83.31, 166.63, 333.26, 666.52 | 20.83 | LOW | 20.83 | 166.63 |
| | | | HIGH | 20.83 | 666.52 |
| | | 41.66 | LOW | 41.66 | 166.63 |
| | | | HIGH | 41.66 | 666.52 |
| | | 83.31 | LOW | 83.31 | 166.63 |
| | | | HIGH | 83.31 | 666.52 |
| | | 166.63 | LOW | 166.63 | 166.63 |
| | | | HIGH | 166.63 | 666.52 |
| | | 333.26 | LOW | 333.26 | 166.63 |
| | | | HIGH | 333.26 | 666.52 |
| | | 666.52 | LOW | 666.52 | 166.63 |
| | | | HIGH | 666.52 | 666.52 |
| 10GE copper | 19.53, 39.06, 78.12, 156.25, 312.5, 625 | 19.53 | LOW | 19.53 | 156.25 |
| | | | HIGH | 19.53 | 625 |
| | | 39.06 | LOW | 39.06 | 156.25 |
| | | | HIGH | 39.06 | 625 |
| | | 78.12 | LOW | 78.12 | 156.25 |
| | | | HIGH | 78.12 | 625 |
| | | 156.25 | LOW | 156.25 | 156.25 |
| | | | HIGH | 156.25 | 625 |
| | | 312.5 | LOW | 312.50 | 156.25 |
| | | | HIGH | 312.5 | 625 |
| | | 625 | LOW | 625 | 156.25 |
| | | | HIGH | 625 | 625 |
| 10GE optical | 20.14, 40.28, 80.56, 161.13, 322.26, 644.53 | 20.14 | LOW | 20.14 | 161.13 |
| | | | HIGH | 20.14 | 644.53 |
| | | 40.28 | LOW | 40.28 | 161.13 |
| | | | HIGH | 40.28 | 644.53 |
| | | 80.56 | LOW | 80.56 | 161.13 |
| | | | HIGH | 80.56 | 644.53 |
| | | 161.13 | LOW | 161.13 | 161.13 |
| | | | HIGH | 161.13 | 644.53 |
| | | 322.26 | LOW | 322.26 | 161.13 |
| | | | HIGH | 322.26 | 644.53 |
| | | 644.53 | LOW | 644.53 | 161.13 |
| | | | HIGH | 644.53 | 644.53 |

POWER SUPPLY CHARACTERISTICS^(1,2)

| Symbol | Parameter | Test Conditions | Typ. | Max | Unit |
|--------------------|--|---|------|-----|------|
| I _{DD_PD} | Power Supply Current | V _{DD} = Max., \overline{PD} = GND, All outputs unloaded | — | 50 | μA |
| ΔI _{DD} | Power Supply Current per Input HIGH (LVTTTL inputs only) | V _{DD} = Max., V _{IN} = 2.375V | — | 100 | μA |
| I _{TOT} | Total Power Supply Current | V _{DD} = Max., Q _{OUT} = 622MHz, All outputs unloaded | — | 200 | mA |

NOTES:

- These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
- As a general requirement, these parts must be capable of operating at the maximum frequency under a nominal load at a reasonable operating temperature. That means that these parts must not burn up under extended use in a typical application.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Test Conditions | | Min. | Max | Unit |
|------------------|---|-----------------------------------|------------|-----------------------|-----|------|
| V _{IHH} | Input HIGH Voltage Level ⁽¹⁾ | 2-Level Inputs Only | | V _{DD} - 0.4 | — | V |
| V _{ILL} | Input LOW Voltage Level ⁽¹⁾ | 2-Level Inputs Only | | — | 0.4 | V |
| I ₂ | 2-Level Input DC Current | V _{IN} = V _{DD} | HIGH Level | — | 200 | μA |
| | | V _{IN} = GND | LOW Level | -200 | — | |

NOTE:

- These inputs are normally wired to V_{DD} or GND. If these inputs are switched dynamically after powerup, the function and timing of the outputs may be glitched, and the PLL may require additional t_{AO} time before all datasheet limits are achieved.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVTTTL

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max | Unit |
|-----------------|---------------------|---|------|------|--------|------|
| I _{IH} | Input HIGH Current | V _{DD} = 3.465V | — | — | ±1 | μA |
| I _{IL} | Input LOW Current | V _{DD} = 3.465V | — | — | ±1 | |
| V _{IK} | Clamp Diode Voltage | V _{DD} = 2.375V, I _{IN} = -18mA | — | -0.7 | -1.2 | V |
| V _{IN} | DC Input Voltage | | -0.3 | — | +3.465 | V |
| V _{IH} | DC Input HIGH | | 1.7 | — | — | V |
| V _{IL} | DC Input LOW | | — | — | 0.7 | V |

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVPECL⁽¹⁾

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|--|--------------------------|------------------------|------|------------------------|------|
| Input Characteristics | | | | | | |
| I _{IN} | Input Current (CLKIN, REFIN) | V _{DD} = 3.465V | -20 | — | +20 | μA |
| V _{CMR} | Common Mode Input Voltage | | 1 | — | V _{DD} - 0.3 | V |
| V _{DIF} | Differential Voltage Required to Toggle Input | | 100 | — | — | mV |
| Output Characteristics | | | | | | |
| V _{OH} | Output Voltage HIGH (terminated through 50Ω tied to V _{DD} - 2V) ⁽²⁾ | | V _{DD} - 1.15 | — | V _{DD} - 0.9 | V |
| V _{OL} | Output Voltage LOW (terminated through 50Ω tied to V _{DD} - 2V) ⁽²⁾ | | V _{DD} - 1.95 | — | V _{DD} - 1.61 | V |
| V _{SWING} | Peak-to-Peak Output Voltage Swing | | 0.55 | — | 0.93 | V |

NOTES:

- V_{DD} = 2.375 - 3.645V.
- Not to exceed V_{DD} - 0.05V.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVDS

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|---|--|-------|------|------------------------|------|
| Input Characteristics | | | | | | |
| I _{IN} | Input Current (CLKIN, REFIN) | V _{DD} = 3.465V | -20 | — | +20 | μA |
| V _{CM} | Common Mode Input Voltage Range ⁽¹⁾ | | 0.9 | — | V _{DD} - 0.05 | V |
| V _{DIF} | Differential Voltage Required to Toggle Input | | 100 | — | — | mV |
| Output Characteristics | | | | | | |
| V _{OT(+)} | Differential Output Voltage for the TRUE Binary State | | 247 | — | 454 | mV |
| V _{OT(-)} | Differential Output Voltage for the FALSE Binary State | | -247 | — | -454 | mV |
| ΔV _{OT} | Change in V _{OT} Between Complementary Output States | | — | — | 50 | mV |
| V _{OS} | Output Common Mode Voltage (Offset Voltage) | | 1.125 | 1.2 | 1.375 | V |
| ΔV _{OS} | Change in V _{OS} Between Complementary Output States | | — | — | 50 | mV |
| I _{OS} | Outputs Short Circuit Current | V _{OUT(+)} and V _{OUT(-)} = 0V | — | 9 | 24 | mA |
| I _{OSD} | Differential Outputs Short Circuit Current | V _{OUT(+)} = V _{OUT(-)} | — | 6 | 12 | mA |

NOTE:

1. Not to exceed V_{DD} - 0.05V.

INPUT TIMING REQUIREMENTS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|----------------------|---|----------------------|------|--------|------|
| REF _H | Input Reference Clock Duty Cycle | 40 | 50 | 60 | % |
| F _{REF} | Input Reference Clock Range | 19.44 | — | 666.52 | MHz |
| REF _{TOL} | Input Reference Clock Frequency Tolerance | -100 | — | 100 | ppm |
| F _{CLKIN} | Clock in Frequency Range | 19.44 | — | 666.52 | MHz |
| CLKIN _H | Clock in Duty Cycle | 40 | 50 | 60 | % |
| t _{AO} | Acquisition Time from Return of Valid CLKIN | — | 60 | 150 | us |
| LOCK _{TOL} | Frequency Tolerance for LOCK | -600 | ±450 | 600 | ppm |
| t _{UI(TOL)} | Tolerance to Input Jitter | GR-253 Sect. 5.6.2.2 | | | |

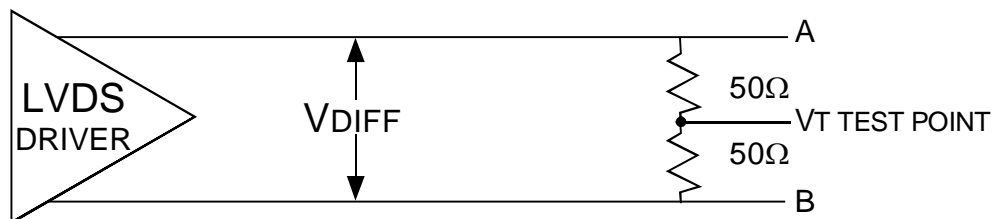
AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | | Min. | Typ. | Max. | Unit |
|--------|--|--|--------|------|--------|----------|
| QOUT | Multiplied Clock Output Frequency | SELmode = LOW | 155.52 | — | 166.63 | MHz |
| | | SELmode = HIGH | 622.08 | — | 666.52 | |
| QREG | Regenerated Clock Output Frequency | | 19.44 | — | 666.52 | MHz |
| CLKIN | Input Clock Frequency | | 19.44 | — | 667 | MHz |
| tr | Output Rise Time | LVPECL | — | 150 | — | ps |
| | | LVDS | — | 100 | — | |
| tf | Output Fall Time | LVPECL | — | 150 | — | ps |
| | | LVDS | — | 100 | — | |
| tsk | Skew between QOUT and QREG | | — | 10 | 20 | ps |
| PLLBW | PLL Bandwidth | | 250 | 305 | 500 | KHz |
| fp | Jitter Transfer Peaking | | — | 0.05 | 0.1 | dB |
| tj | Jitter Generation ⁽¹⁾ (with 12KHz to 20MHz filter) | Output frequency = 622MHz - 666.5MHz | — | 0.4 | 1 | ps (RMS) |
| | | Output frequency = 155.5MHz - 166.6MHz | — | 0.8 | 3.4 | |
| | | Output frequency = 77.7MHz - 83.4MHz | — | 1.2 | 3.5 | |
| tduty | Output Duty Cycle | | 45 | — | 55 | % |

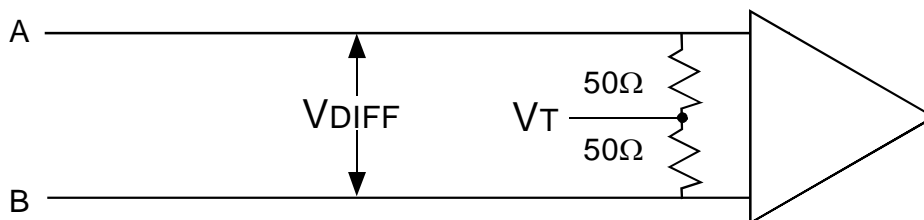
NOTE:

1. All input frequencies permitted by PLL bandwidth.

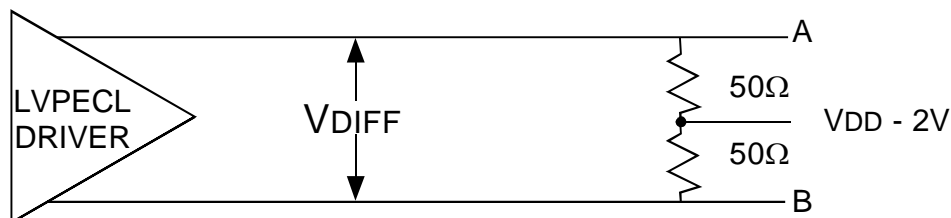
TEST CONDITIONS



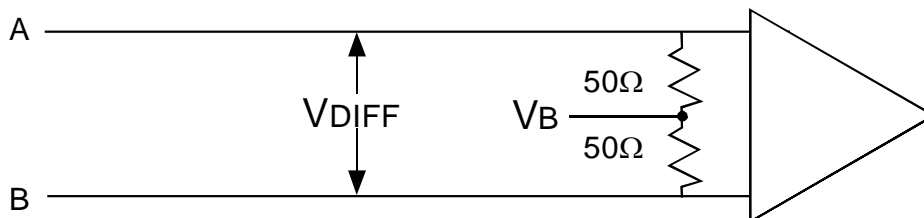
Test Circuit for LVDS Output Characteristics



Test Circuit for LVDS Input Characteristics



Test Circuit for LVPECL Output Characteristics



$$V_B = V_{DD} - 2V$$

Test Circuit for LVPECL Input Characteristics

ORDERING INFORMATION

| IDT | XXXXX | XX | X | | |
|-------------|---------|---------|----------|--|--|
| Device Type | Package | Process | | | |
| | | | I | | -40°C to +85°C (Industrial) |
| | | | NL | | Thermally Enhanced Plastic Very Fine Pitch Quad Flat No Lead Package |
| | | | 5T929-10 | | Precision Clock Generator - LVDS Output |
| | | | 5T929-30 | | Precision Clock Generator - LVPECL Output |



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
(408) 654-6459