



## 3.3V/2.5V PHASE-LOCK LOOP CLOCK DRIVER ZERO DELAY BUFFER

**IDT5V9352**

### FEATURES:

- Phase-lock loop clock distribution for high performance clock tree applications
- Output enable bank control
- External feedback (FBIN) pin is used to synchronize the outputs to the clock input signal
- No external RC network required for PLL loop stability
- Operates at 3.3V/2.5V Vcc
- Spread Spectrum Compatible
- Operating frequency up to 200MHz
- Compatible with Motorola MPC9352
- Available in 32-pin TQFP package

### DESCRIPTION:

The 5V9352 is a low-skew, low-jitter, phase-lock loop (PLL) clock driver targeted for high performance clock tree applications. It uses a PLL to precisely align, in both frequency and phase. The 5V9352 operates at 2.5V and 3.3V.

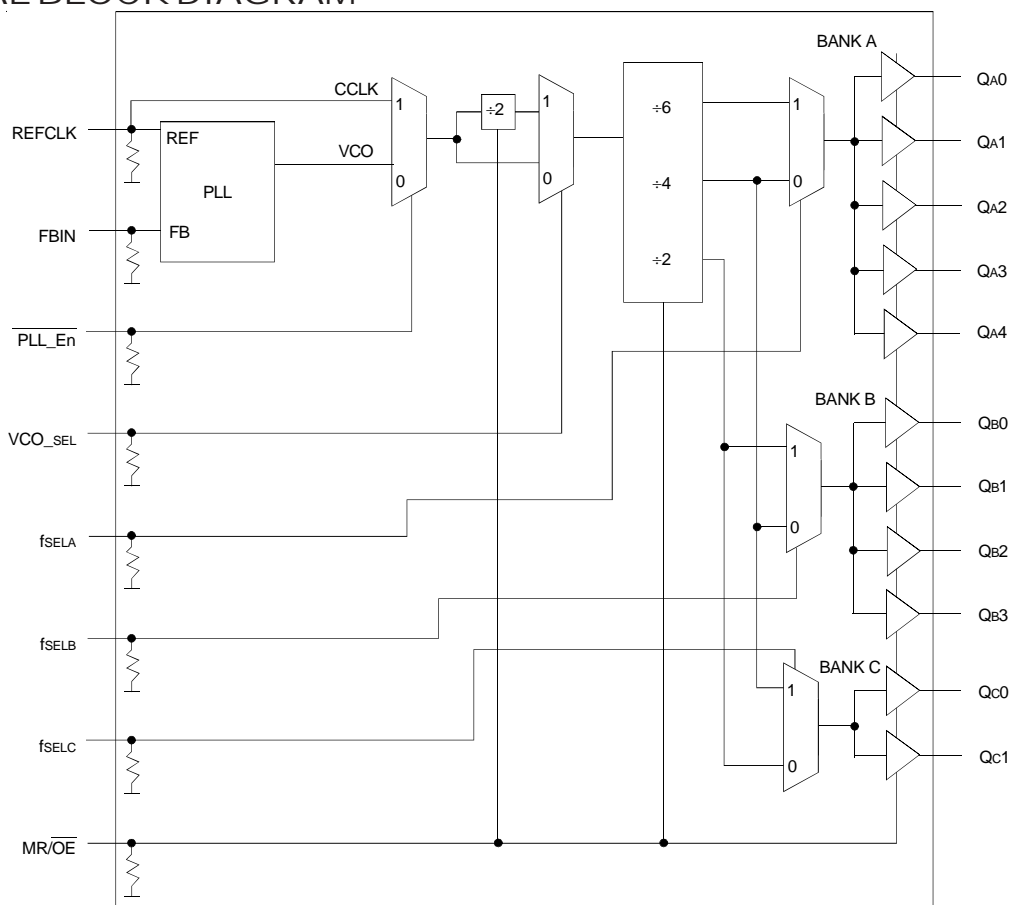
The 5V9352 features three banks of individually configurable outputs. The banks are configured with five, four, and two outputs. The internal divide circuitry allows for output frequency ratios of 1:1, 2:1, 3:1, and 3:2:1. The output frequency relationship is controlled by the fSEL frequency control pins. The fSEL pins, as well as other inputs, are LVCMOS/LVTTL compatible inputs

Unlike many products containing PLLs, the 5V9352 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the 5V9352 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at REFCLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by setting the PLL\_EN to high.

The 5V9352 is available in Industrial temperature range (-40°C to +85°C).

### FUNCTIONAL BLOCK DIAGRAM

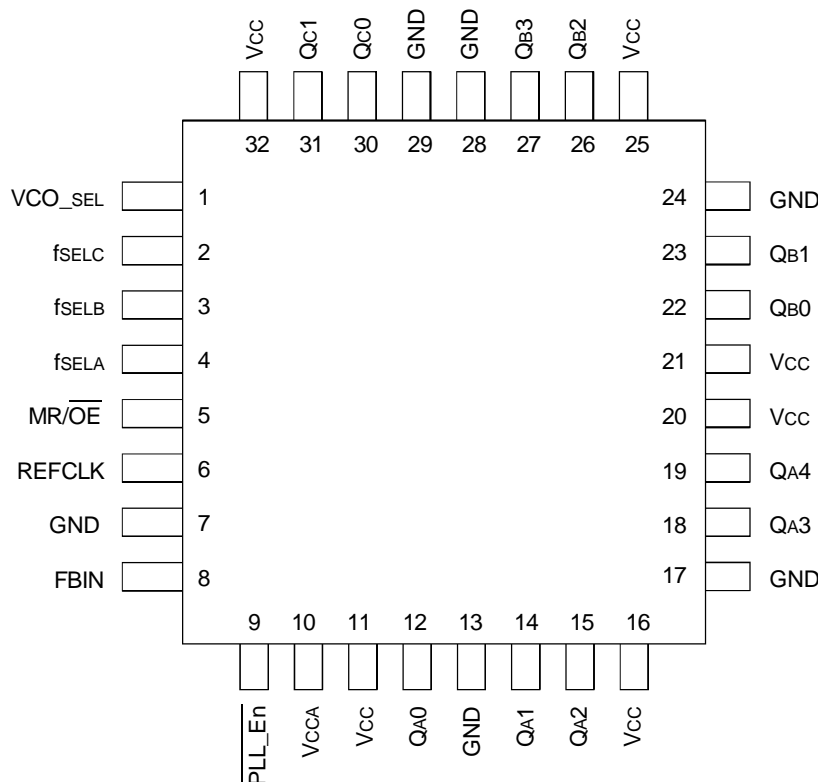


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INDUSTRIAL TEMPERATURE RANGE

AUGUST 2003

## PIN CONFIGURATION



TQFP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Max.	Unit
V <sub>CC</sub>	Supply Voltage Range	-0.3 to +3.6	V
V <sub>I</sub>	Input Voltage Range	-0.3 to V <sub>CC</sub> +0.3	V
I <sub>IN</sub>	Input Current	±20	mA
I <sub>OUT</sub>	DC Output Current	±50	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +125	°C

### NOTE:

- Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

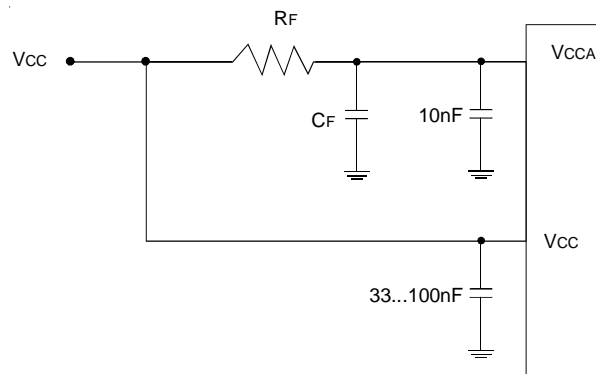
## GENERAL SPECIFICATIONS

Symbol	Description	Min.	Typ.	Max.	Unit
V <sub>TT</sub>	Output Termination Voltage		V <sub>CC</sub> /2		V
HBM	ESD Protection (human body model)	2000			V
LU	Latch-Up Immunity	200			mA

## CAPACITANCE

Parameter	Description	Min.	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	—	4	—	pF
CPD	Power Dissipation Capacitance	—	10	—	pF

## LOGIC DIAGRAM<sup>(1,2)</sup>



### NOTES:

- IDT5V9352 requires an external RC filter for the analog power supply pin VCCA.
- For V<sub>CC</sub> = 2.5V, R<sub>F</sub> = 9-10Ω, C<sub>F</sub> = 22μF.  
For V<sub>CC</sub> = 3.3V, R<sub>F</sub> = 5-15Ω, C<sub>F</sub> = 22μF.

## FUNCTION TABLES

fSELA	QAn	fSELB	QBn	fSELC	QCn
0	÷4	0	÷4	0	÷2
1	÷6	1	÷2	1	÷4

Control Pin	Logic 0	Logic 1
VCO_SEL	fVCO	fVCO / 2
MR/ $\overline{\text{OE}}$	Output Enable	Outputs disable (high-impedance state) and reset of the device.
PLL_En	Enable PLL	Disable PLL

### NOTE:

- IDT5V9352 requires reset at power up and after any loss of PLL lock. Length of reset pulse should be greater than two REF CLK cycles (REFCLK).

## PIN DESCRIPTION

Terminal		Type	Description
Name	No.		
REFCLK	6	I	Reference clock input
FBIN	8	I	Feedback input.
VCCA	10	PWR	Analog power supply
GND	7, 13, 17, 24, 28, 29	Ground	Negative power supply
VCO_SEL	1	I	Allows for the choice of two VCO ranges to optimize PLL stability and jitter performance
MR/ $\overline{\text{OE}}$	5	I	Allows the user to force the outputs into HIGH impedance for board level test
QA(0:4)	12, 14, 15, 18, 19	O	Clock outputs. These outputs provide low skew copies of REFCLK or can be at different frequencies than REFCLK.
QB(0:3)	22, 23, 26, 27		
QC(0:1)	30, 31		
VCC	11, 16, 20, 21, 25, 32	PWR	Positive power supply for I/O and core
PLL_EN	9	I	PLL enable input. When set LOW, PLL is enabled. When set HIGH, PLL is disabled.
fSEL(C:A)	2, 3, 4	I	Frequency control pin

## DC ELECTRICAL CHARACTERISTICS

T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 3.3V ± 5%

Parameter	Description	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Level		2		V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Level				0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -24mA	2.4			V
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 12mA			0.3	V
		I <sub>OL</sub> = 24mA			0.55	
Z <sub>OUT</sub>	Output Impedance			14 - 17		Ω
I <sub>I</sub>	Input Current <sup>(2)</sup>	V <sub>I</sub> = V <sub>CC</sub> or GND			±200	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current <sup>(3)</sup>	All V <sub>CC</sub> pins			1	mA
I <sub>CCA</sub>	PLL Supply Current	V <sub>CCA</sub> pin		3	5	mA

### NOTES:

- For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
- Inputs have pull-down resistors affecting the input current.
- I<sub>CC</sub> is the DC current consumption of the device with all outputs open in high-impedance state and the inputs in its default state or open.

## INPUT TIMING REQUIREMENTS

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 5\%$

Symbol	Description		Min.	Max.	Unit
REF	Reference CLK input in PLL mode <sup>(1)</sup>	$\div 4$ feedback	50	100	MHz
		$\div 6$ feedback	33.3	66.6	
		$\div 8$ feedback	25	50	
		$\div 12$ feedback	16.67	33.3	
	Reference CLK input in PLL bypass mode <sup>(2)</sup>			250	
d H	Input clock duty cycle		25	75	%
t <sub>R</sub> , t <sub>F</sub>	Maximum input rise and fall times, 0.8V to 2V		—	1	ns

### NOTES:

1. PLL mode requires  $\overline{\text{PLL\_EN}} = 0$  to enable the PLL and zero delay operation.
2. In PLL bypass mode, the IDT5V9352 divides the input reference clock.

## AC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 3.3V ± 5%

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall Time	0.55V to 2.4V	0.1		1	ns
t <sub>SK(O)</sub>	Output to Output Skew	All Outputs, any frequency			200	ps
		within Q <sub>A</sub> output bank			200	
		within Q <sub>B</sub> output bank			100	
		within Q <sub>C</sub> output bank			100	
f <sub>VCO</sub>	PLL VCO Lock Range <sup>(2)</sup>		200		400	MHz
f <sub>MAX</sub>	Maximum Output Frequency	÷2 output	100		200	MHz
		÷4 output	50		100	
		÷6 output	33.3		66.6	
		÷8 output	25		50	
		÷12 output	16.67		33.3	
t <sub>PW</sub>	Output Duty Cycle		47	50	53	%
t <sub>PD</sub>	REFCLK to FBIN Delay	f <sub>REF</sub> < 40MHz	-200		+150	ps
	PLL Locked	f <sub>REF</sub> > 40MHz, PLL locked	-50		+150	
t <sub>PLZ</sub>	Output Disable Time				8	ns
t <sub>PHZ</sub>	MR/ $\overline{\text{OE}}$ (LOW-HIGH) to any Q					
t <sub>PZL</sub>	Output Enable Time				10	ns
t <sub>PZH</sub>	MR/ $\overline{\text{OE}}$ (HIGH-LOW) to any Q					
t <sub>J</sub>	Cycle-to-Cycle Jitter	Output frequencies mixed			400	ps
		Outputs in any ÷4 and ÷6 combination			250	
		All outputs same frequency			100	
t <sub>J(PER)</sub>	Period Jitter	Output frequencies mixed			200	ps
		Outputs in any ÷4 and ÷6 combination			150	
		All outputs same frequency			75	
t <sub>J(φ)</sub>	I/O Phase Jitter	÷4 feedback divider RMS (1σ)		15		ps
		÷6 feedback divider RMS (1σ)		20		
		÷8 feedback divider RMS (1σ)		18-20		
		÷12 feedback divider RMS (1σ)		25		
BW	PLL Closed Loop Bandwidth	÷4 feedback		3 - 10		MHz
		÷6 feedback		1.5 - 6		
		÷8 feedback		1 - 3.5		
		÷12 feedback		0.5 - 2		
t <sub>LOCK</sub>	Maximum PLL Lock Time				10	ms

### NOTES:

- AC characteristics apply for parallel output termination of 50Ω to V<sub>TT</sub>.
- The input frequency on CCLK must match the VCO frequency range divided by the feedback divide ratio FB: freq. = f<sub>VCO</sub> ÷ FB.

## DC ELECTRICAL CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 2.5\text{V} \pm 5\%$

Parameter	Description	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	LVC MOS	1.7		$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Level	LVC MOS	-0.3		0.7	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -15\text{mA}$	1.8			V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 15\text{mA}$			0.6	V
$Z_{OUT}$	Output Impedance			17 - 20		$\Omega$
$I_I^{(2)}$	Input Current	$V_I = V_{CC}$ or GND			$\pm 200$	$\mu\text{A}$
$I_{CC}^{(3)}$	Maximum Quiescent Supply Current				1	mA
$I_{CCA}$	PLL Supply Current			2	5	mA

### NOTES:

1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
2. Inputs have pull-down resistors affecting the input current.
3.  $I_{CC}$  is the DC current consumption of the device with all outputs open in High-Impedance state and the inputs in its default state (or open).

## INPUT TIMING REQUIREMENTS

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 2.5\text{V} \pm 5\%$

Symbol	Description		Min.	Max.	Unit
REF	Reference CLK input <sup>(1)</sup>	÷4 feedback	50	100	MHz
		÷6 feedback	33.3	66.6	
		÷8 feedback	25	50	
		÷12 feedback	16.67	33.3	
	Reference CLK input in PLL bypass mode <sup>(2)</sup>			250	
d H	Input clock duty cycle		25	75	%
tR, tF	Maximum input rise and fall times, 0.8V to 2V		—	1	ns

### NOTES:

1. Maximum and minimum input reference is limited by the VCO clock range and the feedback divider.
2. In PLL bypass mode, the 5V9352 divides the input reference clock.

## AC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

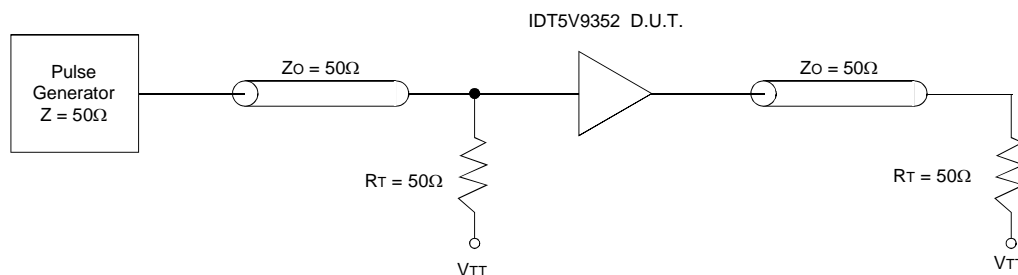
T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 2.5V ± 5%

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>R</sub> , t <sub>F</sub>	Output Rise/Fall Time	0.6V to 1.8V	0.1		1	ns
t <sub>SK(O)</sub>	Output to Output Skew	All Outputs, any frequency			200	ps
		within Q <sub>A</sub> output bank			200	
		within Q <sub>B</sub> output bank			100	
		within Q <sub>C</sub> output bank			100	
f <sub>VCO</sub>	PLL VCO Lock Range		200		400	MHz
f <sub>MAX</sub>	Maximum Output Frequency	÷2 output	100		200	MHz
		÷4 output	50		100	
		÷6 output	33.3		66.6	
		÷8 output	25		50	
		÷12 output	16.67		33.3	
t <sub>PW</sub>	Output Duty Cycle		47	50	53	%
t <sub>PD</sub>	REFCLK to FBIN Delay	f <sub>REF</sub> < 40MHz	-200		+150	ps
	PLL Locked	f <sub>REF</sub> > 40MHz	-50		+150	
t <sub>PLZ</sub>	Output Disable Time				8	ns
t <sub>PHZ</sub>	MR/ $\overline{\text{OE}}$ (LOW-HIGH) to any Q					
t <sub>PZL</sub>	Output Enable Time				10	ns
t <sub>PZH</sub>	MR/ $\overline{\text{OE}}$ (HIGH-LOW) to any Q					
t <sub>J</sub>	Cycle-to-Cycle Jitter	Output frequencies mixed			400	ps
		Outputs in any ÷4 and ÷6 combination			250	
		All outputs same frequency			100	
t <sub>J(PER)</sub>	Period Jitter	Output frequencies mixed			200	ps
		Outputs in any ÷4 and ÷6 combination			150	
		All outputs same frequency			75	
t <sub>J(φ)</sub>	I/O Phase Jitter	÷4 feedback divider RMS (1σ)		15		ps
		÷6 feedback divider RMS (1σ)		20		
		÷8 feedback divider RMS (1σ)		18-20		
		÷12 feedback divider RMS (1σ)		25		
BW	PLL Closed Loop Bandwidth	÷4 feedback		1 - 8		MHz
		÷6 feedback		0.7 - 3		
		÷8 feedback		0.5 - 2.5		
		÷12 feedback		0.4 - 1		
t <sub>LOCK</sub>	Maximum PLL Lock Time				10	ms

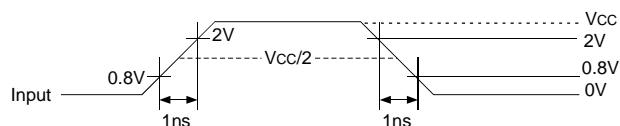
### NOTE:

1. AC characteristics apply for parallel output termination of 50Ω to V<sub>TT</sub>.

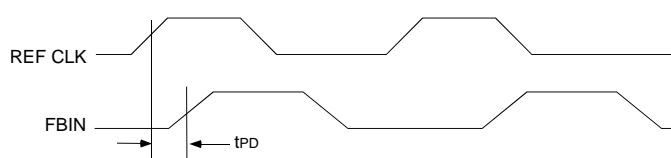
## TEST CIRCUITS AND WAVEFORMS



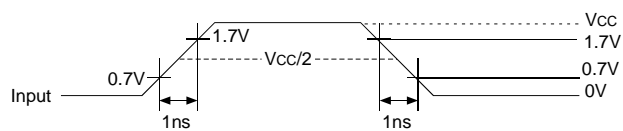
*AC Test Reference for  $V_{CC} = 2.5V$  and  $V_{CC} = 3.3V$*



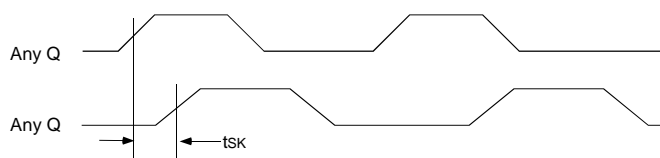
*Input Characteristics for 3.3V*



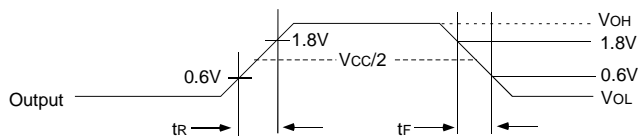
*Prop Delay*



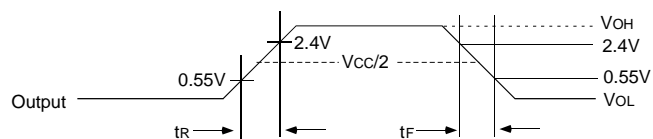
*Input Characteristics for 2.5V*



*Skew Calculations*

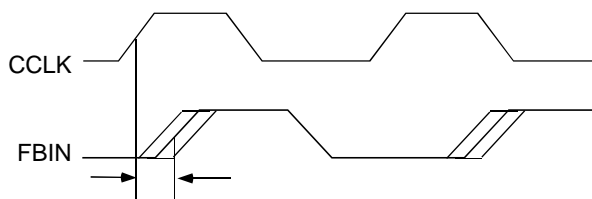


*Output Test Conditions for  $V_{CC} = 2.5V \pm 5\%$*



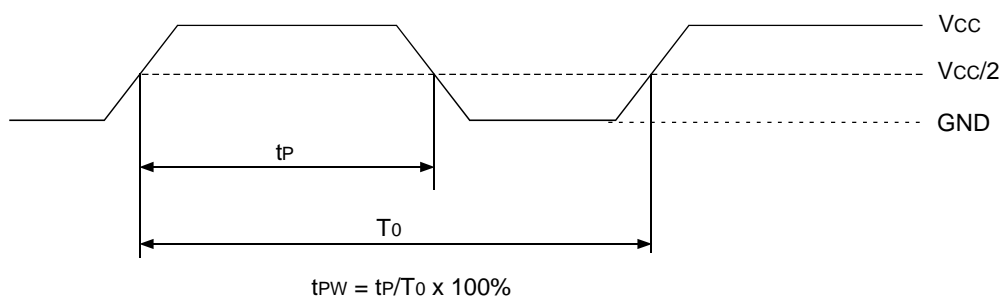
*Output Test Conditions for  $V_{CC} = 3.3V \pm 5\%$*



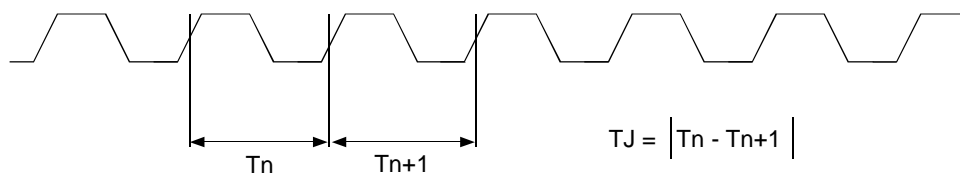


$$T_{J(0)} = |T_0 - T_1 \text{ MEAN}|$$

*I/O Jitter*

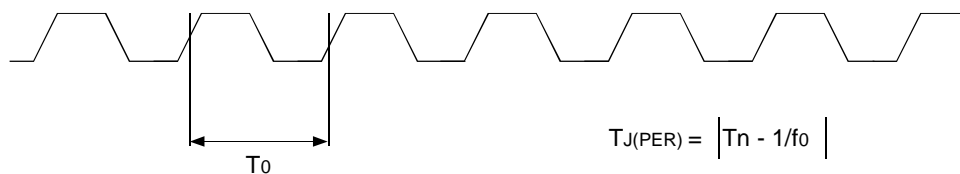


*Output Duty Cycle*



$$T_J = |T_n - T_{n+1}|$$

*Cycle-to-Cycle Jitter*



$$T_{J(PER)} = |T_n - 1/f_0|$$

*Period Jitter*

## ORDERING INFORMATION

IDT	XXXXX	XX	X		
Device Type	Package	Process			
			I		-40°C to +85°C (Industrial)
			PR		Thin Quad Flat Pack
			5V9352		3.3V/2.5V Phase-Lock Loop Clock Driver Zero Delay Buffer



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