



## 3.3V PROGRAMMABLE SKEW DUAL PLL CLOCK DRIVER TURBOCLOCK™ W

IDT5V9955

### FEATURES:

- Ref input is 5V tolerant
- 8 pairs of programmable skew outputs
- Two separate A and B banks for individual control
- Low skew: 185ps same pair, 250ps same bank, 350ps both banks
- Selectable positive or negative edge synchronization on each bank: excellent for DSP applications
- Synchronous output enable on each bank
- Input frequency: 2MHz to 200MHz
- Output frequency: 6MHz to 200MHz
- 3-level inputs for skew and PLL range control
- 3-level inputs for feedback divide selection multiply / divide ratios of (1-6, 8, 10, 12) / (2, 4)
- PLL bypass for DC testing
- External feedback, internal loop filter
- 12mA balanced drive outputs
- Low Jitter: <100ps cycle-to-cycle
- Power-down mode on each bank
- Lock indicator on each bank
- Available in BGA package

### DESCRIPTION

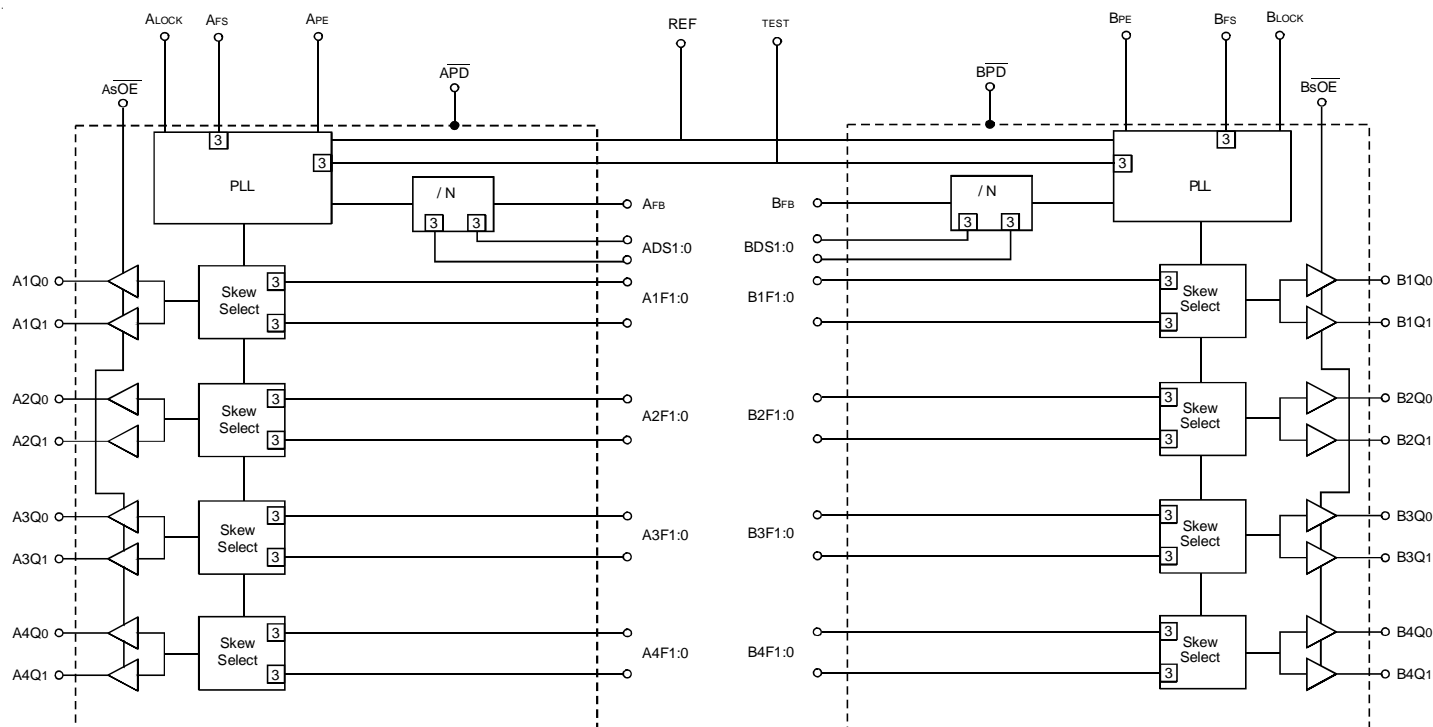
The IDT5V9955 is a high fanout 3.3V PLL based clock driver intended for high performance computing and data-communications applications. A key feature of the programmable skew is the ability of outputs to lead or lag the REF input signal. The IDT5V9955 has sixteen programmable skew outputs in eight banks of 2. The two separate PLLs allow the user to independently control A and B banks. Skew is controlled by 3-level input signals that may be hard-wired to appropriate HIGH-MID-LOW levels.

The feedback input allows divide-by-functionality from 1 to 12 through the use of the xDS[1:0] inputs. This provides the user with frequency multiplication from 1 to 12 without using divided outputs for feedback.

When the x $\overline{\text{SOE}}$  pin is held low, all the xbank outputs are synchronously enabled. However, if x $\overline{\text{SOE}}$  is held high, all the xbank outputs except x2Q0 and x2Q1 are synchronously disabled. The xLOCK is high when the xbank PLL has achieved phase lock.

Furthermore, when xPE is held high, all the outputs are synchronized with the positive edge of the REF clock input. When xPE is held low, all the xbank outputs are synchronized with the negative edge of REF. The IDT5V9955 has LVTTTL outputs with 12mA balanced drive outputs.

### FUNCTIONAL BLOCK DIAGRAM



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INDUSTRIAL TEMPERATURE RANGE

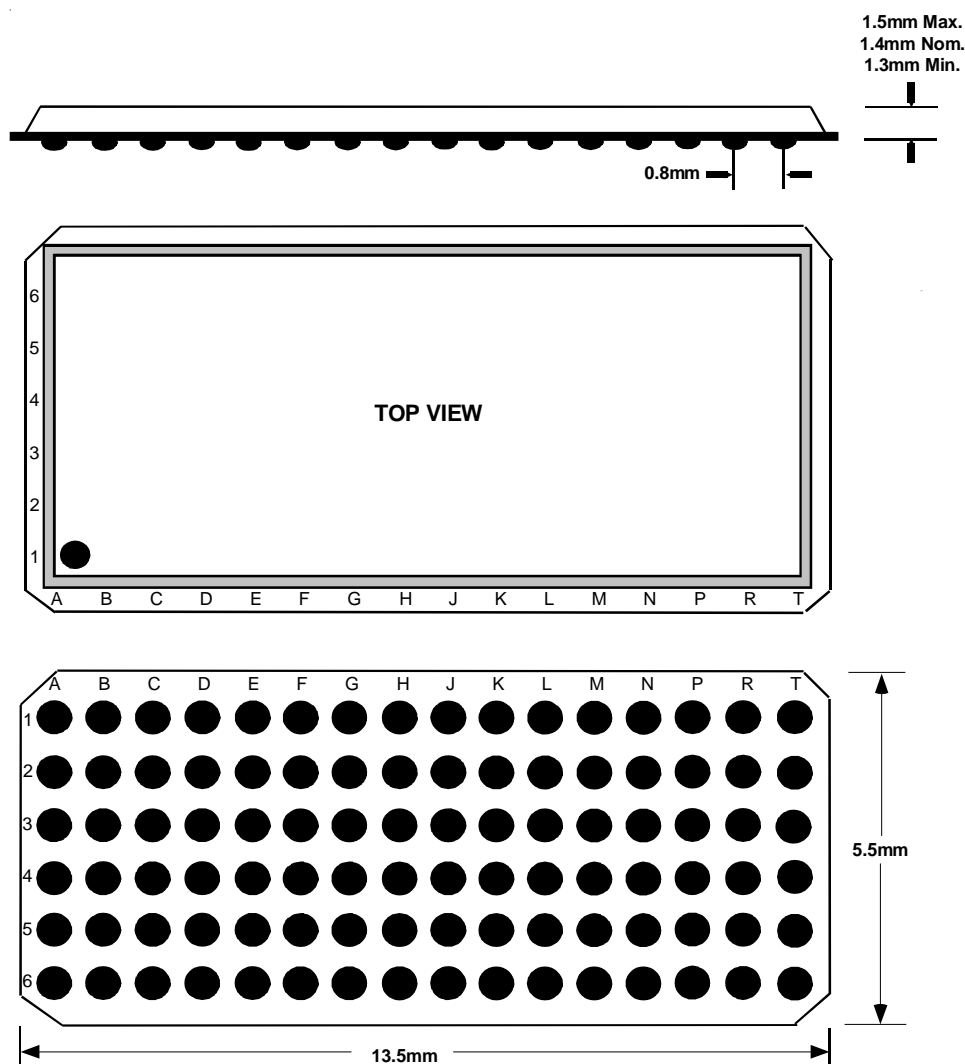
JUNE 2002

## PIN CONFIGURATION

6	A3Q1	A4Q0	A4Q1	APE	$\overline{APD}$	A4F1	A3F1	AFS	B2F1	B1F1	BDS1	BLOCK	BVDDQ	B1Q0	B1Q1	B2Q0
5	A3Q0	AGND	AGND	AGND	$\overline{ASOE}$	A4F0	A3F0	AVDD	BGND	B2F0	B1F0	BDS0	BVDDQ	BGND	BGND	B2Q1
4	AGND	AGND	AGND	AVDDQ	AVDDQ	AVDDQ	AVDDQ	TEST	BVDDQ	BVDDQ	BVDDQ	BVDDQ	BVDDQ	BGND	BGND	BFB
3	AFB	AGND	AGND	AVDDQ	AVDDQ	AVDDQ	AVDDQ	REF	BVDDQ	BVDDQ	BVDDQ	BVDDQ	BVDDQ	BGND	BGND	BGND
2	A2Q1	AGND	AGND	AVDDQ	ADS0	A1F0	A2F0	AGND	BVDD	B3F0	B4F0	$\overline{BSOE}$	BGND	BGND	BGND	B3Q0
1	A2Q0	A1Q1	A1Q0	AVDDQ	ALOCK	ADS1	A1F1	A2F1	BFS	B3F1	B4F1	$\overline{BPD}$	BPE	B4Q1	B4Q0	B3Q1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

FPBGA  
TOP VIEW

## 96 BALL FPBGA PACKAGE ATTRIBUTES



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description		Max	Unit
V <sub>DDQ</sub> , V <sub>DD</sub>	Supply Voltage to Ground		−0.5 to +4.6	V
V <sub>I</sub>	DC Input Voltage		−0.5 to V <sub>DD</sub> +0.5	V
	REF Input Voltage		−0.5 to +5.5	V
	Maximum Power Dissipation	T <sub>A</sub> = 85°C	1.1	W
		T <sub>A</sub> = 55°C	1.9	
T <sub>STG</sub>	Storage Temperature Range		−65 to +150	°C

### NOTE:

- Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1MHz, V<sub>IN</sub> = 0V)

Parameter	Description		Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	REF	8	10	pF
		Others	5	7	

### NOTE:

- Capacitance applies to all inputs except TEST, xFS, xnF[1:0], and xDS[1:0].

## PIN DESCRIPTION

Pin Name	Type	Description
REF	IN	Reference Clock Input
xFB	IN	Individual Feedback Inputs for A and B banks
TEST <sup>(1)</sup>	IN	When MID or HIGH, disables PLL for A and B banks (except for conditions of Note 1). REF goes to all outputs. Skew Selections (See Control Summary Table) remain in effect. Set LOW for normal operation.
xsOE <sup>(1)</sup>	IN	Individual Synchronous Output Enable for A and B banks. When HIGH, it stops clock outputs (except x2Q0 and x2Q1) in a LOW state (for xPE = H) - x2Q0 and x2Q1 may be used as the feedback signal to maintain phase lock. When TEST is held at MID level and xsOE is HIGH, the nF[1:0] pins act as output disable controls for individual banks when xnF[1:0] = LL. Set xsOE LOW for normal operation (has internal pull-down).
xPE	IN	Individual Selectable positive or negative edge control for A and B banks. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock (has internal pull-up).
xnF[1:0]	IN	3-level inputs for selecting 1 of 9 skew taps or frequency functions
xFS	IN	Selects appropriate oscillator circuit based on anticipated frequency range. (See Programmable Skew Range.) Individual control on A and B banks.
xnQ[1:0]	OUT	Eight banks of two outputs with programmable skew
xDS[1:0]	IN	3-level inputs for feedback divider selection for A and B banks
xPD	IN	Power down control. Shuts off either A or B bank of the chip when LOW (has internal pull-up).
xLOCK	OUT	PLL lock indication signal for A and B banks. HIGH indicates lock. LOW indicates that the PLL is not locked and outputs may not be synchronized to the inputs.
V <sub>DDQ</sub>	PWR	Power supply for output buffers
V <sub>DD</sub>	PWR	Power supply for phase locked loop, lock output, and other internal circuitry
GND	PWR	Ground

### NOTE:

- When TEST = MID and xsOE = HIGH, PLL remains active with xnF[1:0] = LL functioning as an output disable control for individual output banks. Skew selections remain in effect unless xnF[1:0] = LL.

## PROGRAMMABLE SKEW

Output skew with respect to the REF input is adjustable to compensate for PCB trace delays, backplane propagation delays or to accommodate requirements for special timing relationships between clocked components. Skew is selectable as a multiple of a time unit (tu) which ranges from 625ps to 1.3ns (see Programmable Skew Range and Resolution Table). There are nine skew configurations available for each output pair. These configurations are chosen by the xnF1:0 control pins. In

order to minimize the number of control pins, 3-level inputs (HIGH-MID-LOW) are used, they are intended for but not restricted to hard-wiring. Undriven 3-level inputs default to the MID level. Where programmable skew is not a requirement, the control pins can be left open for the zero skew default setting. The Control Summary Table shows how to select specific skew taps by using the xnF1:0 control pins.

## EXTERNAL FEEDBACK

By providing two separate external feedbacks, the IDT5V9955 gives users flexibility with regard to skew adjustment. The xFB signal is compared with the input REF signal at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly.

An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

## PROGRAMMABLE SKEW RANGE AND RESOLUTION TABLE

	xFS = LOW	xFS = MID	xFS = HIGH	Comments
Timing Unit Calculation (tu)	$1/(32 \times F_{NOM})$	$1/(16 \times F_{NOM})$	$1/(8 \times F_{NOM})$	
VCO Frequency Range ( $F_{NOM}$ ) <sup>(1,2)</sup>	24 to 50MHz	48 to 100MHz	96 to 200MHz	
Skew Adjustment Range <sup>(3)</sup>				
Max Adjustment:	$\pm 7.8125ns$	$\pm 7.8125ns$	$\pm 7.8125ns$	ns
	$\pm 67.5^\circ$	$\pm 135^\circ$	$\pm 270^\circ$	Phase Degrees
	$\pm 18.75\%$	$\pm 37.5\%$	$\pm 75\%$	% of Cycle Time
Example 1, $F_{NOM} = 25MHz$	tu = 1.25ns	—	—	
Example 2, $F_{NOM} = 37.5MHz$	tu = 0.833ns	—	—	
Example 3, $F_{NOM} = 50MHz$	tu = 0.625ns	tu = 1.25ns	—	
Example 4, $F_{NOM} = 75MHz$	—	tu = 0.833ns	—	
Example 5, $F_{NOM} = 100MHz$	—	tu = 0.625ns	tu = 1.25ns	
Example 6, $F_{NOM} = 150MHz$	—	—	tu = 0.833ns	
Example 7, $F_{NOM} = 200MHz$	—	—	tu = 0.625ns	

### NOTES:

- The device may be operated outside recommended frequency ranges without damage, but functional operation is not guaranteed.
- The level to be set on xFS is determined by the nominal operating frequency of the VCO and Time Unit Generator. The VCO frequency always appears at x1Q1:0, x2Q1:0, and the higher outputs when they are operated in their undivided modes. The frequency appearing at the REF and xFB inputs will be  $F_{NOM}$  when the output connected to xFB is undivided and xDS[1:0] = MM. The frequency of the REF and xFB inputs will be  $F_{NOM}/2$  or  $F_{NOM}/4$  when the part is configured for frequency multiplication by using a divided output as the xFB input and setting xDS[1:0] = MM. Using the xDS[1:0] inputs allows a different method for frequency multiplication (see Divide Selection Table).
- Skew adjustment range assumes that a zero skew output is used for feedback. If a skewed xQ output is used for feedback, then adjustment range will be greater. For example if a 4tu skewed output is used for feedback, all other outputs will be skewed  $-4tu$  in addition to whatever skew value is programmed for those outputs. 'Max adjustment' range applies to output pairs 3 and 4 where  $\pm 6tu$  skew adjustment is possible and at the lowest  $F_{NOM}$  value.

## DIVIDE SELECTION TABLE

xDS[1:0]	xFB Divide-by-n	Permitted Output Divide-by-n connected to xFB <sup>(1)</sup>
LL	2	1 or 2
LM	3	1
LH	4	1, 2, or 4
ML	5	1 or 2
MM	1	1, 2, or 4
MH	6	1 or 2
HL	8	1 or 2
HM	10	1
HH	12	1

**NOTE:**  
1. Permissible output division ratios connected to xFB. The frequency of the REF input will be  $F_{NOM}/N$  when the part is configured for frequency multiplication by using an undivided output for xFB and setting xDS[1:0] to N (N = 1-6, 8, 10, 12).

## CONTROL SUMMARY TABLE FOR FEEDBACK SIGNALS

nF1:0	Skew (Pair #1, #2)	Skew (Pair #3)	Skew (Pair #4)
LL <sup>(1)</sup>	-4t <sub>u</sub>	Divide by 2	Divide by 2
LM	-3t <sub>u</sub>	-6t <sub>u</sub>	-6t <sub>u</sub>
LH	-2t <sub>u</sub>	-4t <sub>u</sub>	-4t <sub>u</sub>
ML	-1t <sub>u</sub>	-2t <sub>u</sub>	-2t <sub>u</sub>
MM	Zero Skew	Zero Skew	Zero Skew
MH	1t <sub>u</sub>	2t <sub>u</sub>	2t <sub>u</sub>
HL	2t <sub>u</sub>	4t <sub>u</sub>	4t <sub>u</sub>
HM	3t <sub>u</sub>	6t <sub>u</sub>	6t <sub>u</sub>
HH	4t <sub>u</sub>	Divide by 4	Inverted <sup>(2)</sup>

**NOTES:**  
1. LL disables outputs if TEST = MID and  $\overline{xsOE}$  = HIGH.  
2. When pair #4 is set to HH (inverted),  $\overline{xsOE}$  disables pair #4 HIGH when xPE = HIGH,  $\overline{xsOE}$  disables pair #4 LOW when xPE = LOW.

## RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub> /V <sub>DDO</sub>	Power Supply Voltage	3	3.3	3.6	V
T <sub>A</sub>	Ambient Operating Temperature	-40	+25	+85	°C

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions <sup>(1)</sup>	Min.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Logic HIGH (REF, xFB Inputs Only)	2	—	V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Logic LOW (REF, xFB Inputs Only)	—	0.8	V
V <sub>IHH</sub>	Input HIGH Voltage <sup>(2)</sup>	3-Level Inputs Only	V <sub>DD</sub> −0.6	—	V
V <sub>IMM</sub>	Input MID Voltage <sup>(2)</sup>	3-Level Inputs Only	V <sub>DD</sub> /2−0.3	V <sub>DD</sub> /2+0.3	V
V <sub>ILL</sub>	Input LOW Voltage <sup>(2)</sup>	3-Level Inputs Only	—	0.6	V
I <sub>IN</sub>	Input Leakage Current (REF, xFB Inputs Only)	V <sub>IN</sub> = V <sub>DD</sub> or GND V <sub>DD</sub> = Max.	−5	+5	μA
I <sub>3</sub>	3-Level Input DC Current (TEST, xFS, xnF[1:0], xDS[1:0])	V <sub>IN</sub> = V <sub>DD</sub> HIGH Level	—	+400	μA
		V <sub>IN</sub> = V <sub>DD</sub> /2 MID Level	−100	+100	
		V <sub>IN</sub> = GND LOW Level	−400	—	
I <sub>PU</sub>	Input Pull-Up Current (xPE, xPD)	V <sub>DD</sub> = Max., V <sub>IN</sub> = GND	−25	—	μA
I <sub>PD</sub>	Input Pull-Down Current (xsOE)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>DD</sub>	—	+100	μA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = −2mA (xLOCK Output)	2.4	—	V
		V <sub>DDQ</sub> = Min., I <sub>OH</sub> = −12mA (xnQ[1:0] Outputs)	2.4	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 2mA (xLOCK Output)	—	0.4	V
		V <sub>DDQ</sub> = Min., I <sub>OL</sub> = 12mA (xnQ[1:0] Outputs)	—	0.4	

### NOTES:

1. All conditions apply to A and B banks.
2. These inputs are normally wired to V<sub>DD</sub>, GND, or unconnected. Internal termination resistors bias unconnected inputs to V<sub>DD</sub>/2. If these inputs are switched, the function and timing of the outputs may be glitched, and the PLL may require an additional t<sub>LOCK</sub> time before all datasheet limits are achieved.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>DDQ</sub>	Quiescent Power Supply Current	V <sub>DD</sub> = Max., TEST = MID, REF = LOW, xPE = LOW, xsOE = LOW, xPD = HIGH xFS = MID, All outputs unloaded	40	60	mA
I <sub>DDPD</sub>	Power Down Current	V <sub>DD</sub> = Max., PD = LOW, xsOE = LOW xPE = HIGH, TEST = HIGH, xFS = HIGH xnF[1:0] = HH, xDS[1:0] = HH	—	50	μA
ΔI <sub>DD</sub>	Power Supply Current per Input HIGH (REF and xFB inputs only)	V <sub>IN</sub> = 3V, V <sub>DD</sub> = Max., xPD = LOW, TEST = HIGH	1	60	μA
I <sub>DDO</sub>	Dynamic Power Supply Current per Output	xFS = L	190	290	μA/MHz
		xFS = M	150	230	
		xFS = H	130	200	
I <sub>TOT</sub>	Total Power Supply Current	xFS = L, F <sub>VCO</sub> = 50MHz, C <sub>L</sub> = 0pF	112	—	mA
		xFS = M, F <sub>VCO</sub> = 100MHz, C <sub>L</sub> = 0pF	160	—	
		xFS = H, F <sub>VCO</sub> = 200MHz, C <sub>L</sub> = 0pF	250	—	

### NOTES:

1. Measurements are for divide-by-1 outputs, xnF[1:0] = MM, and xDS[1:0] = MM. All conditions apply to A and B banks.
2. For nominal voltage and temperature.

## INPUT TIMING REQUIREMENTS

Symbol	Description <sup>(1)</sup>		Min.	Max.	Unit
t <sub>r</sub> , t <sub>f</sub>	Maximum input rise and fall times, 0.8V to 2V		—	10	ns/V
t <sub>pw</sub>	Input clock pulse, HIGH or LOW		2	—	ns
D <sub>H</sub>	Input duty cycle		10	90	%
F <sub>REF</sub>	Reference clock input frequency	xFS = LOW	2	50	MHz
		xFS = MID	4	100	
		xFS = HIGH	8	200	

### NOTE:

- Where pulse width implied by D<sub>H</sub> is less than t<sub>pw</sub> limit, t<sub>pw</sub> limit applies.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

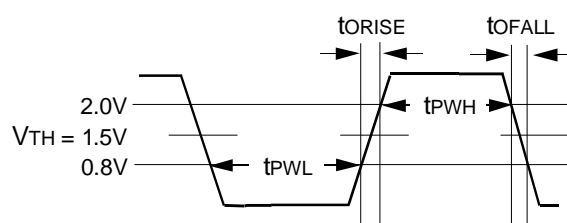
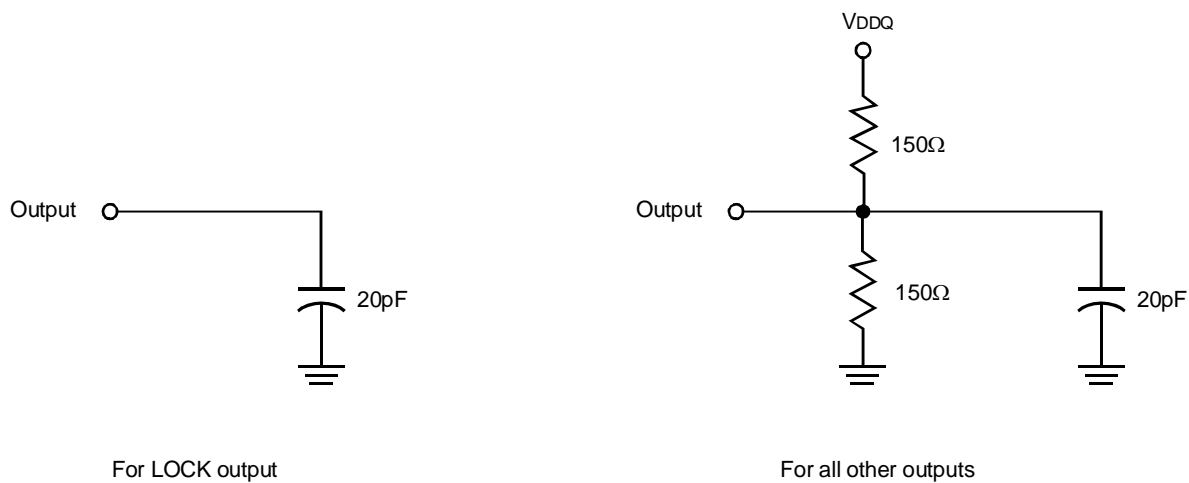
Symbol	Parameter	Min.	Typ.	Max.	Unit
F <sub>NOM</sub>	VCO Frequency Range	See Programmable Skew Range and Resolution Table			
t <sub>RPWH</sub>	REF Pulse Width HIGH <sup>(1)</sup>	2	—	—	ns
t <sub>RPWL</sub>	REF Pulse Width LOW <sup>(1)</sup>	2	—	—	ns
t <sub>U</sub>	Programmable Skew Time Unit	See Control Summary Table			
t <sub>SKWPR</sub>	Zero Output Matched-Pair Skew (x <sub>nQ0</sub> , x <sub>nQ1</sub> ) <sup>(2,3)</sup>	—	50	185	ps
t <sub>SKWB</sub>	Bank Skew <sup>(4)</sup>	—	0.1	0.35	ns
t <sub>SKW0</sub>	Zero Output Skew (All Outputs from the same A or B bank) <sup>(5)</sup>	—	0.1	0.25	ns
t <sub>SKW1</sub>	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs) <sup>(6)</sup>	—	0.1	0.25	ns
t <sub>SKW2</sub>	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided) <sup>(6)</sup>	—	0.2	0.5	ns
t <sub>SKW3</sub>	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs) <sup>(6)</sup>	—	0.15	0.5	ns
t <sub>SKW4</sub>	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted) <sup>(2)</sup>	—	0.3	0.9	ns
t <sub>DEV</sub>	Device-to-Device Skew <sup>(2,7)</sup>	—	—	0.75	ns
t <sub>φ1-3</sub>	Static Phase Offset (xFS = L, M, H) (FB Divide-by-n = 1, 2, 3) <sup>(8)</sup>	−0.25	—	0.25	ns
t <sub>φH</sub>	Static Phase Offset (xFS = H) <sup>(8)</sup>	−0.25	—	0.25	ns
t <sub>φM</sub>	Static Phase Offset (xFS = M) <sup>(8)</sup>	−0.5	—	0.5	ns
t <sub>φL1-6</sub>	Static Phase Offset (xFS = L) (x <sub>FB</sub> Divide-by-n = 1, 2, 3, 4, 5, 6) <sup>(8)</sup>	−0.7	—	0.7	ns
t <sub>φL8-12</sub>	Static Phase Offset (xFS = L) (x <sub>FB</sub> Divide-by-n = 8, 10, 12) <sup>(8)</sup>	−1	—	1	ns
t <sub>ODCV</sub>	Output Duty Cycle Variation from 50%	−1	0	1	ns
t <sub>PWH</sub>	Output HIGH Time Deviation from 50% <sup>(9)</sup>	—	—	1.5	ns
t <sub>PWL</sub>	Output LOW Time Deviation from 50% <sup>(10)</sup>	—	—	2	ns
t <sub>ORISE</sub>	Output Rise Time	0.15	0.7	1.5	ns
t <sub>OFALL</sub>	Output Fall Time	0.15	0.7	1.5	ns
t <sub>LOCK</sub>	PLL Lock Time <sup>(11,12)</sup>	—	—	0.5	ms
t <sub>CCJH</sub>	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, xFS = H, FB divide-by-n=1,2)	—	—	100	ps
t <sub>CCJHA</sub>	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, xFS = H, FB divide-by-n=any)	—	—	150	
t <sub>CCJM</sub>	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, xFS = M)	—	—	150	
t <sub>CCJL</sub>	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, xFS = L, F <sub>REF</sub> > 3MHz)	—	—	200	
t <sub>CCJLA</sub>	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, xFS = L, F <sub>REF</sub> < 3MHz)	—	—	300	

### NOTES:

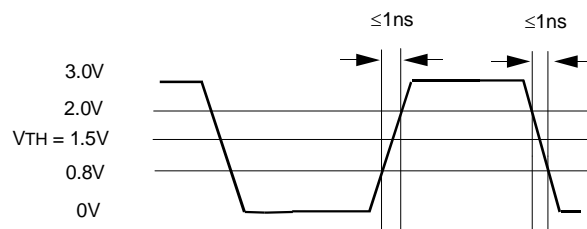
1. Refer to Input Timing Requirements table for more detail.
2. Skew is the time between the earliest and the latest output transition among all outputs for which the same t<sub>U</sub> delay has been selected when all are loaded with the specified load.
3. t<sub>SKWPR</sub> is the skew between a pair of outputs (x<sub>nQ0</sub> and x<sub>nQ1</sub>) when all sixteen outputs are selected for 0t<sub>U</sub>.
4. t<sub>SKWB</sub> is the skew between outputs (x<sub>nQ0</sub> and x<sub>nQ1</sub>) from A and B banks when they are selected for 0t<sub>U</sub>.
5. t<sub>SK(0)</sub> is the skew between outputs when they are selected for 0t<sub>U</sub>.
6. There are 3 classes of outputs: Nominal (multiple of t<sub>U</sub> delay), Inverted (x<sub>4Q0</sub> and x<sub>4Q1</sub> only with x<sub>4F0</sub> = x<sub>4F1</sub> = HIGH), and Divided (x<sub>3Q1:0</sub> and x<sub>4Q1:0</sub> only in Divide-by-2 or Divide-by-4 mode). Test condition: x<sub>nF0:1</sub>=MM is set on unused outputs.
7. t<sub>DEV</sub> is the output-to-output skew between any two devices operating under the same conditions (V<sub>DDQ</sub>, V<sub>DD</sub>, ambient temperature, air flow, etc.)
8. t<sub>φ</sub> is measured with REF input rise and fall times (from 0.8V to 2V) of 0.5ns. Measured from 1.5V on REF to 1.5V on xFB.
8. Measured at 2V.
10. Measured at 0.8V.
11. t<sub>LOCK</sub> is the time that is required before synchronization is achieved. This specification is valid only after V<sub>DD</sub>/V<sub>DDQ</sub> is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or xFB until t<sub>PD</sub> is within specified limits.
12. Lock detector may be unreliable for input frequencies less than approximately 4MHz, or for input signals which contain significant jitter.



## AC TEST LOADS AND WAVEFORMS

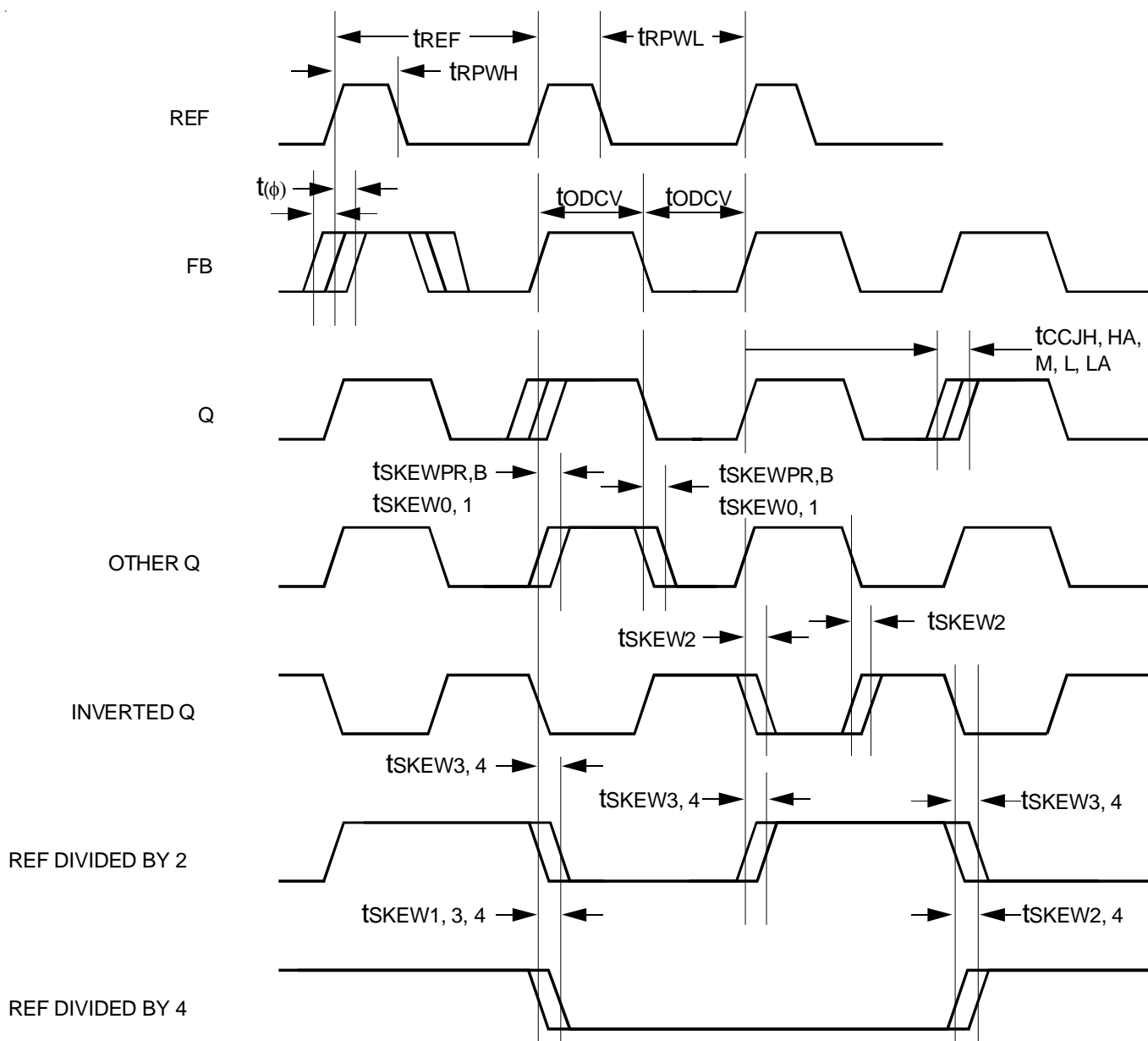


*LVTTTL Output Waveform*



*LVTTTL Input Test Waveform*

## AC TIMING DIAGRAM



### NOTES:

PE: The AC Timing Diagram applies to PE=VDD. For PE=GND, the negative edge of FB aligns with the negative edge of REF, divided outputs change on the negative edge of REF, and the positive edges of the divide-by-2 and the divide-by-4 signals align.

Skew: The time between the earliest and the latest output transition among all outputs for which the same  $t_u$  delay has been selected when all are loaded with 20pF and terminated with  $75\Omega$  to  $V_{DDQ}/2$ .

$t_{SKEWPR}$ : The skew between a pair of outputs (xnQ0 and xnQ1) when all eight outputs are selected for 0tu.

$t_{SKEWB}$ : The skew between outputs (xnQ0 and xnQ1) from A and B banks when they are selected for 0tu.

$t_{SKEW0}$ : The skew between outputs when they are selected for 0tu.

$t_{DEV}$ : The output-to-output skew between any two devices operating under the same conditions ( $V_{DDQ}$ ,  $V_{DD}$ , ambient temperature, air flow, etc.)

$t_{ODCV}$ : The deviation of the output from a 50% duty cycle. Output pulse width variations are included in  $t_{SKEW2}$  and  $t_{SKEW4}$  specifications.

$t_{PW}$  is measured at 2V.

$t_{PWL}$  is measured at 0.8V.

$t_{ORISE}$  and  $t_{OFALL}$  are measured between 0.8V and 2V.

$t_{LOCK}$ : The time that is required before synchronization is achieved. This specification is valid only after  $V_{DD}/V_{DDQ}$  is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until  $t_{PD}$  is within specified limits.

## ORDERING INFORMATION

IDT	XXXXX Device Type	XX Package	X Package		
			I		-40°C to +85°C (Industrial)
			BF		Fine Pitch Ball Grid Array
			5V9955		3.3V Programmable Skew Dual PLL Clock Driver TurboClock W



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