



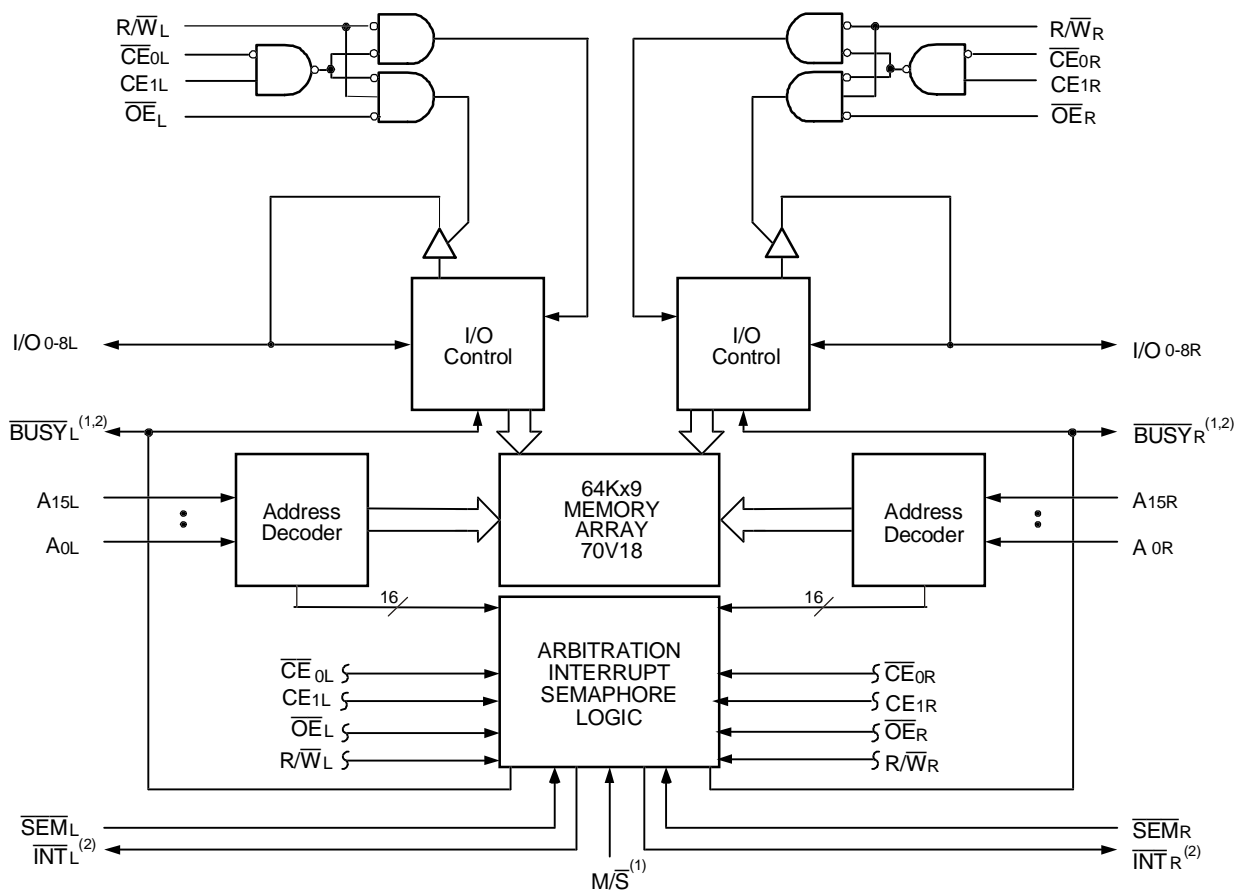
HIGH-SPEED 3.3V 64K x 9 DUAL-PORT STATIC RAM

PRELIMINARY
IDT70V18L

Features

- ♦ True Dual-Ported memory cells which allow simultaneous access of the same memory location
- ♦ High-speed access
 - Commercial: 15/20ns (max.)
 - Industrial: 20ns (max.)
- ♦ Low-power operation
 - IDT70V18L
 - Active: 440mW (typ.)
 - Standby: 660μW (typ.)
- ♦ Dual chip enables allow for depth expansion without external logic
- ♦ IDT70V18 easily expands data bus width to 18 bits or more using the Master/Slave select when cascading more than one device
- ♦ $\overline{M/\overline{S}} = V_{IH}$ for \overline{BUSY} output flag on Master, $\overline{M/\overline{S}} = V_{IL}$ for \overline{BUSY} input on Slave
- ♦ Busy and Interrupt Flags
- ♦ On-chip port arbitration logic
- ♦ Full on-chip hardware support of semaphore signaling between ports
- ♦ Fully asynchronous operation from either port
- ♦ LVTTTL-compatible, single 3.3V ($\pm 0.3V$) power supply
- ♦ Available in a 100-pin TQFP
- ♦ Industrial temperature range ($-40^{\circ}C$ to $+85^{\circ}C$) is available for selected speeds

Functional Block Diagram



NOTES:

1. \overline{BUSY} is an input as a Slave ($\overline{M/\overline{S}} = V_{IL}$) and an output when it is a Master ($\overline{M/\overline{S}} = V_{IH}$).
2. \overline{BUSY} and \overline{INT} are non-tri-state totem-pole outputs (push-pull).

JANUARY 2002

Description

The IDT70V18 is a high-speed 64K x 9 Dual-Port Static RAM. The IDT70V18 is designed to be used as a stand-alone 576K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 18-bit-or-more word system. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 18-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

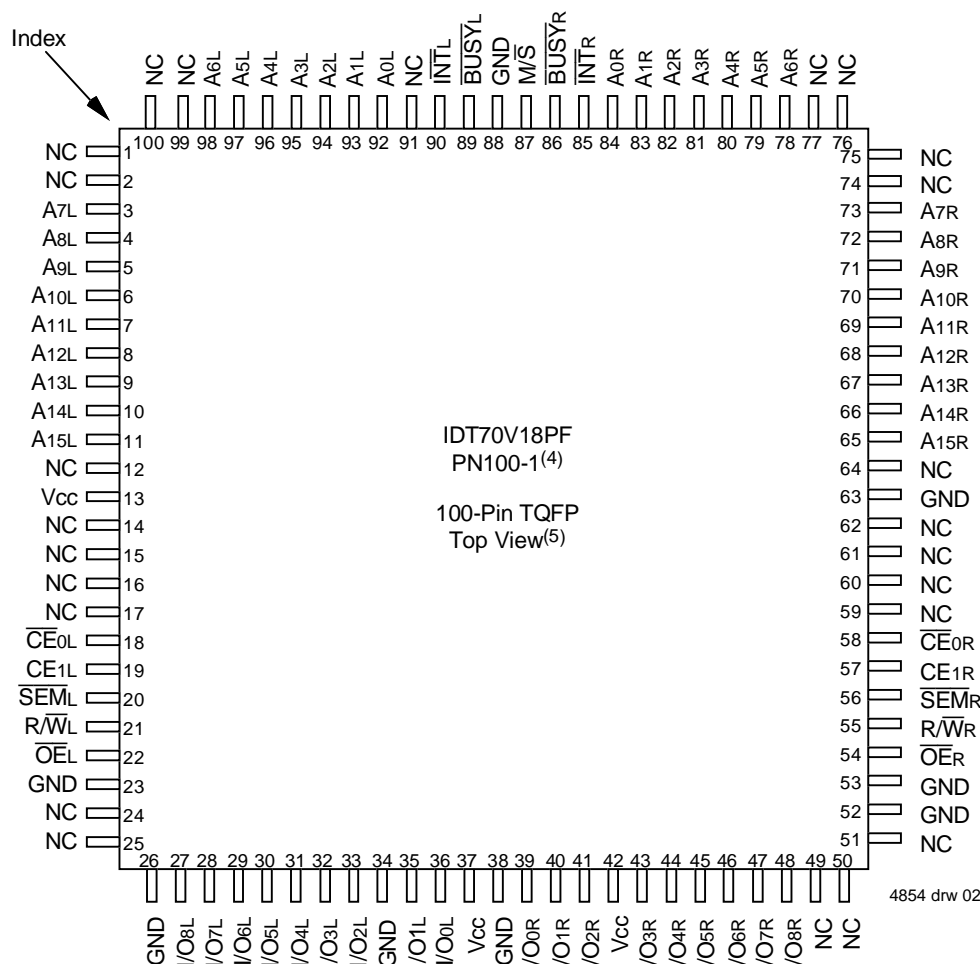
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access

for reads or writes to any location in memory. An automatic power down feature controlled by the chip enables (either $\overline{CE_0}$ or CE_1) permit the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 440mW of power.

The IDT70V18 is packaged in a 100-pin Thin Quad Flatpack (TQFP).

Pin Configurations^(1,2,3)



NOTES:

1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
\overline{CE}_{0L} , CE_{1L}	\overline{CE}_{0R} , CE_{1R}	Chip Enables
R/\overline{W}_L	R/\overline{W}_R	Read/Write Enable
\overline{OE}_L	\overline{OE}_R	Output Enable
A_{0L} - A_{15L}	A_{0R} - A_{15R}	Address
I/O_{0L} - I/O_{8L}	I/O_{0R} - I/O_{8R}	Data Input/Output
\overline{SEM}_L	\overline{SEM}_R	Semaphore Enable
\overline{INT}_L	\overline{INT}_R	Interrupt Flag
\overline{BUSY}_L	\overline{BUSY}_R	Busy Flag
M/\overline{S}		Master or Slave Select
V_{CC}		Power
GND		Ground

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Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed $V_{CC} + 0.3V$ for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq 20mA$ for the period of $V_{TERM} \geq V_{CC} + 0.3V$.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	$V_{CC} + 0.3^{(2)}$	V
V_{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

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NOTES:

- $V_{IL} \geq -1.5V$ for pulse width less than 10ns.
- V_{TERM} must not exceed $V_{CC} + 0.3V$.

Capacitance⁽¹⁾ ($T_A = +25^\circ C$, $f = 1.0MHz$)

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 3dV$	9	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 3dV$	10	pF

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NOTES:

- This parameter is determined by device characterization but is not production tested.
- 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage

Grade	Ambient Temperature ⁽¹⁾	GND	V_{CC}
Commercial	0°C to +70°C	0V	$3.3V \pm 0.3V$
Industrial	-40°C to +85°C	0V	$3.3V \pm 0.3V$

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NOTES:

- This is the parameter T_A . This is the "instant on" case temperature.

Truth Table I – Chip Enable^(1,2)

\overline{CE}	\overline{CE}_0	CE_1	Mode
L	V_{IL}	V_{IH}	Port Selected (TTL Active)
	$\leq 0.2V$	$\geq V_{CC} - 0.2V$	Port Selected (CMOS Active)
H	V_{IH}	X	Port Deselected (TTL Inactive)
	X	V_{IL}	Port Deselected (TTL Inactive)
	$\geq V_{CC} - 0.2V$	$X^{(3)}$	Port Deselected (CMOS Inactive)
	$X^{(3)}$	$\leq 0.2V$	Port Deselected (CMOS Inactive)

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NOTES:

1. Chip Enable references are shown above with the actual \overline{CE}_0 and CE_1 levels; \overline{CE} is a reference only.
2. 'H' = V_{IH} and 'L' = V_{IL} .
3. CMOS standby requires 'X' to be either $\leq 0.2V$ or $\geq V_{CC} - 0.2V$.

Truth Table II – Non-Contention Read/Write Control

Inputs ⁽¹⁾				Outputs	Mode
$\overline{CE}^{(2)}$	R/W	\overline{OE}	\overline{SEM}	I/O ₀₋₈	
H	X	X	H	High-Z	Deselected: Power-Down
L	L	X	H	DATA _{IN}	Write to Memory
L	H	L	H	DATA _{OUT}	Read Memory
X	X	H	X	High-Z	Outputs Disabled

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NOTES:

1. A_{0L} — A_{15L} ≠ A_{0R} — A_{15R}
2. Refer to Chip Enable Truth Table.

Truth Table III – Semaphore Read/Write Control⁽¹⁾

Inputs				Outputs	Mode
$\overline{CE}^{(2)}$	R/W	\overline{OE}	\overline{SEM}	I/O ₀₋₈	
H	H	L	L	DATA _{OUT}	Read Semaphore Flag Data Out
H	↑	X	L	DATA _{IN}	Write I/O ₀ into Semaphore Flag
L	X	X	L	—	Not Allowed

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NOTES:

1. There are eight semaphore flags written to I/O₀ and read from all the I/Os (I/O₀-I/O₈). These eight semaphore flags are addressed by A₀-A₂.
2. Refer to Chip Enable Truth Table.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{CC} = 3.3V \pm 0.3V$)

Symbol	Parameter	Test Conditions	70V18L		Unit
			Min.	Max.	
$ I_{LI} $	Input Leakage Current ⁽¹⁾	$V_{CC} = 3.6V$, $V_{IN} = 0V$ to V_{CC}	—	5	μA
$ I_{LO} $	Output Leakage Current	$\overline{CE}^{(2)} = V_{IH}$, $V_{OUT} = 0V$ to V_{CC}	—	5	μA
V_{OL}	Output Low Voltage	$I_{OL} = +4mA$	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4mA$	2.4	—	V

NOTES:

- At $V_{CC} \leq 2.0V$, input leakages are undefined.
- Refer to Truth Table I - Chip Enable- .

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DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽⁵⁾ ($V_{CC} = 3.3V \pm 0.3V$)

Symbol	Parameter	Test Condition	Version	70V18L15 Com'l Only		70V18L20 Com'l & Ind		Unit
				Typ. ⁽¹⁾	Max.	Typ. ⁽¹⁾	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$, Outputs Disabled $SEM = V_{IH}$ $f = f_{MAX}^{(2)}$	COM'L L	145	235	135	205	mA
			IND L	---	---	135	220	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $SEMR = SEM_L = V_{IH}$ $f = f_{MAX}^{(2)}$	COM'L L	40	70	35	55	mA
			IND L	---	---	35	65	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_A = V_{IL}$ and $\overline{CE}_B = V_{IH}^{(4)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(2)}$, $SEMR = SEM_L = V_{IH}$	COM'L L	100	155	90	140	mA
			IND L	---	---	90	150	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(3)}$ $SEMR = SEM_L \geq V_{CC} - 0.2V$	COM'L L	0.2	3.0	0.2	3.0	mA
			IND L	---	---	0.2	3.0	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_A \leq 0.2V$ and $\overline{CE}_B \geq V_{CC} - 0.2V^{(4)}$, $SEMR = SEM_L \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port Outputs Disabled, $f = f_{MAX}^{(2)}$	COM'L L	95	150	90	135	mA
			IND L	---	---	90	145	

NOTES:

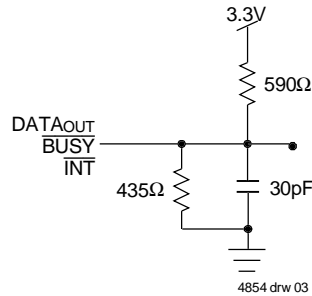
- $V_{CC} = 3.3V$, $T_A = +25^\circ C$, and are not production tested. $I_{CCDC} = 90mA$ (Typ.)
- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/trc, and using "AC Test Conditions" of input levels of GND to 3V.
- $f = 0$ means no address or control lines change.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- Refer to Truth Table I - Chip Enable.

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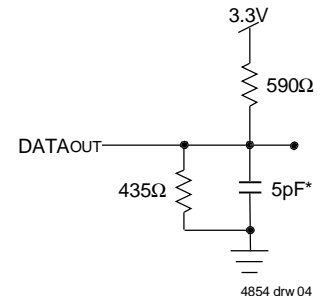
AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

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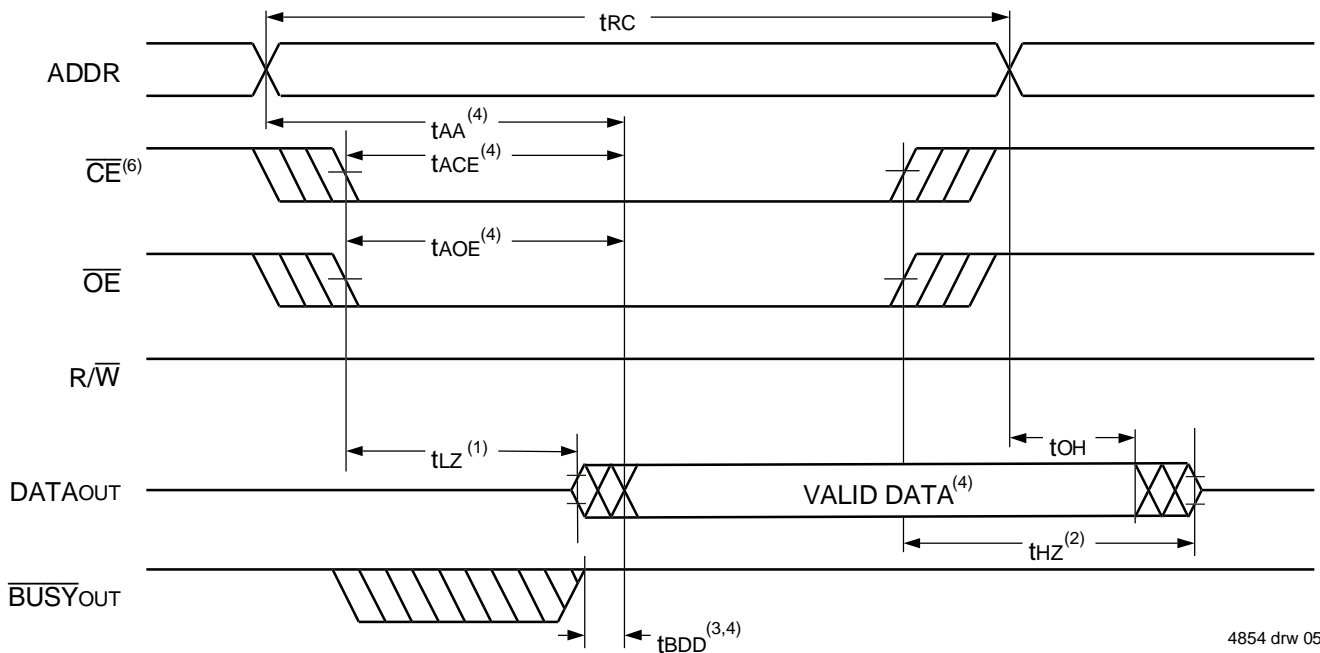


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Figure 1. AC Output Load

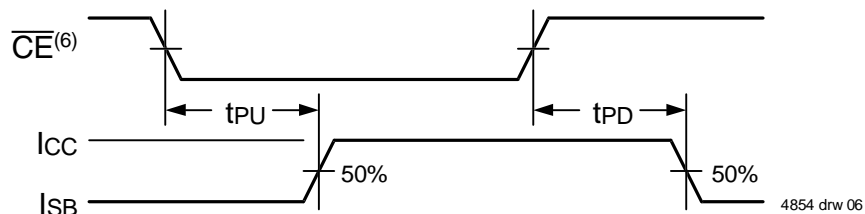
Figure 2. Output Test Load
(for tLZ, tHZ, tWZ, tOW)
* Including scope and jig.

Waveform of Read Cycles⁽⁵⁾



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Timing of Power-Up Power-Down



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NOTES:

1. Timing depends on which signal is asserted last, \overline{OE} or \overline{CE} .
2. Timing depends on which signal is de-asserted first, \overline{CE} or \overline{OE} .
3. t_{BDD} delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations \overline{BUSY} has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last t_{AOE} , t_{ACE} , t_{AA} or t_{BDD} .
5. $SEM = V_{IH}$.
6. Refer to Truth Table I - Chip Enable.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

		70V18L15 Com'l Only		70V18L20 Com'l & Ind		Unit
Symbol	Parameter	Min.	Max.	Min.	Max.	
READ CYCLE						
tRC	Read Cycle Time	15	—	20	—	ns
tAA	Address Access Time	—	15	—	20	ns
tACE	Chip Enable Access Time ⁽³⁾	—	15	—	20	ns
tAOE	Output Enable Access Time	—	10	—	12	ns
tOH	Output Hold from Address Change	3	—	3	—	ns
tLZ	Output Low-Z Time ^(1,2)	3	—	3	—	ns
tHZ	Output High-Z Time ^(1,2)	—	10	—	10	ns
tPU	Chip Enable to Power Up Time ⁽²⁾	0	—	0	—	ns
tPD	Chip Disable to Power Down Time ⁽²⁾	—	15	—	20	ns
tSOP	Semaphore Flag Update Pulse (\overline{OE} or \overline{SEM})	10	—	10	—	ns
tSAA	Semaphore Address Access Time	—	15	—	20	ns

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AC Electrical Characteristics Over the Operating Temperature and Supply Voltage

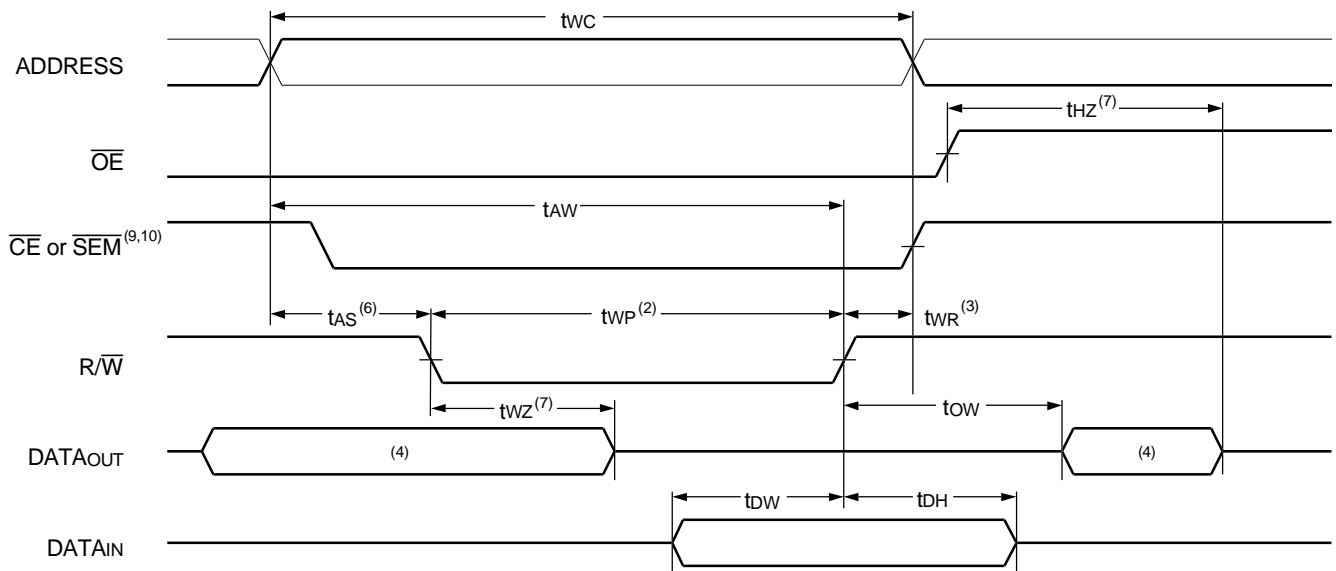
Symbol	Parameter	70V18L15 Com'l Only		70V18L20 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t _{WC}	Write Cycle Time	15	—	20	—	ns
t _{EW}	Chip Enable to End-of-Write ⁽³⁾	12	—	15	—	ns
t _{AW}	Address Valid to End-of-Write	12	—	15	—	ns
t _{AS}	Address Set-up Time ⁽³⁾	0	—	0	—	ns
t _{WP}	Write Pulse Width	12	—	15	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	ns
t _{DW}	Data Valid to End-of-Write	10	—	15	—	ns
t _{HZ}	Output High-Z Time ^(1,2)	—	10	—	10	ns
t _{DH}	Data Hold Time ⁽⁴⁾	0	—	0	—	ns
t _{WZ}	Write Enable to Output in High-Z ^(1,2)	—	10	—	10	ns
t _{OW}	Output Active from End-of-Write ^(1,2,4)	0	—	0	—	ns
t _{SWRD}	\overline{SEM} Flag Write to Read Time	5	—	5	—	ns
t _{SPS}	\overline{SEM} Flag Contention Window	5	—	5	—	ns

NOTES:

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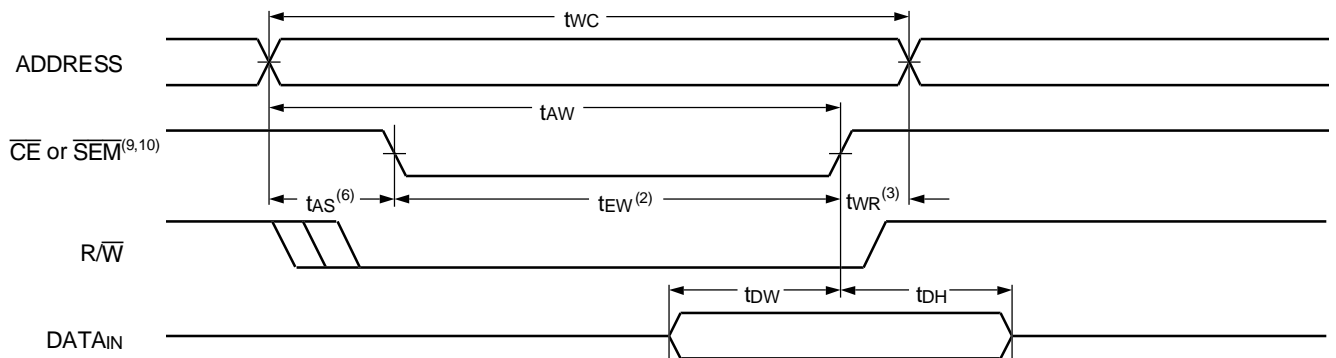
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE} = V_{IL}$ and $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$ and $\overline{SEM} = V_{IL}$. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.

Timing Waveform of Write Cycle No. 1, R/W Controlled Timing^(1,5,8)



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Timing Waveform of Write Cycle No. 2, \overline{CE} Controlled Timing^(1,5)

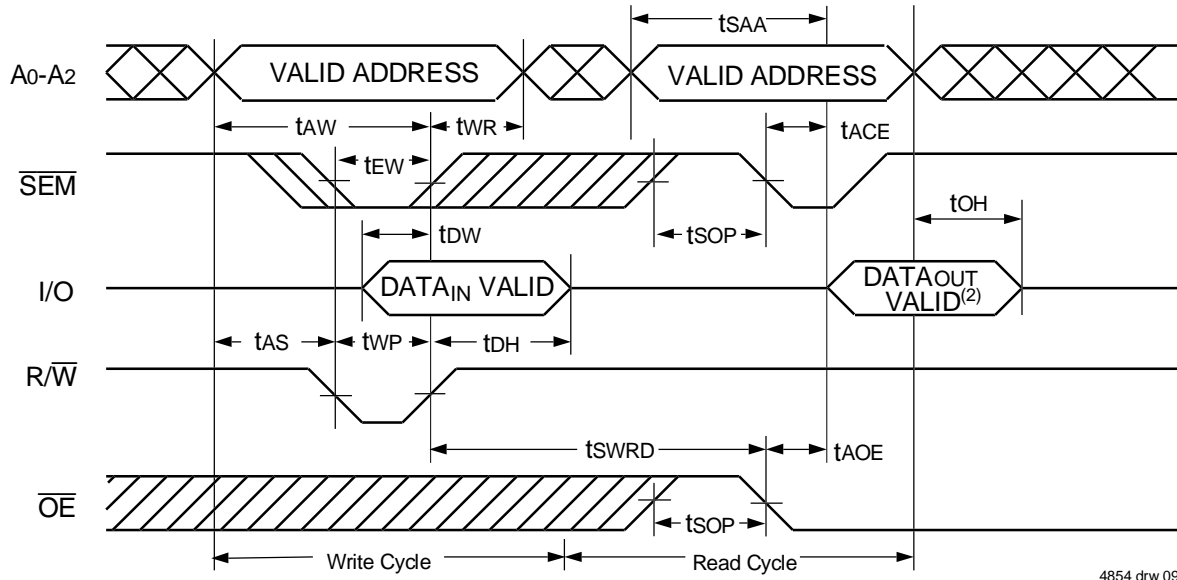


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NOTES:

1. R/\overline{W} or $\overline{CE} = V_{IH}$ during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE} = V_{IL}$ and a $R/\overline{W} = V_{IL}$ for memory array writing cycle.
3. t_{WR} is measured from the earlier of \overline{CE} or R/\overline{W} (or \overline{SEM} or R/\overline{W}) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the \overline{CE} or $\overline{SEM} = V_{IL}$ transition occurs simultaneously with or after the $R/\overline{W} = V_{IL}$ transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, \overline{CE} or R/\overline{W} .
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE} = V_{IL}$ during R/\overline{W} controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WZ} + t_{DW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If $\overline{OE} = V_{IH}$ during an R/\overline{W} controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .
9. To access RAM, $\overline{CE} = V_{IL}$ and $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$ and $\overline{SEM} = V_{IL}$. t_{EW} must be met for either condition.
10. Refer to Truth Table I - Chip Enable.

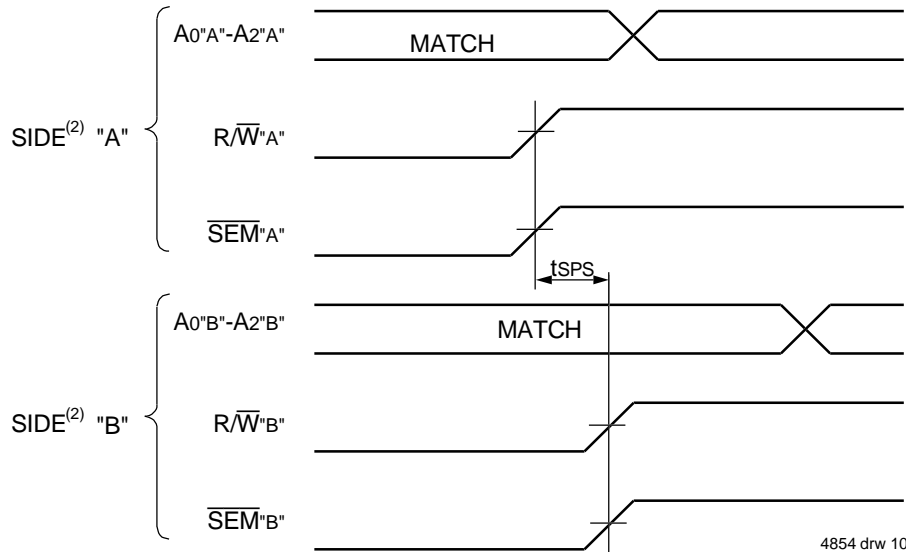
Timing Waveform of Semaphore Read after Write Timing, Either Side⁽¹⁾



NOTES:

1. $\overline{CE} = V_{IH}$ for the duration of the above timing (both write and read cycle) (Refer to Chip Enable Truth Table).
2. "DATAOUT VALID" represents all I/O's (I/O₀ - I/O₈) equal to the semaphore value.

Timing Waveform of Semaphore Write Contention^(1,3,4)



NOTES:

1. $D_{OR} = D_{OL} = V_{IL}$, $\overline{CE}_L = \overline{CE}_R = V_{IH}$ (Refer to Chip Enable Truth Table).
2. All timing is the same for left and right ports. Port "A" may be either left or right port. "B" is the opposite from port "A".
3. This parameter is measured from R/\overline{W}_A or \overline{SEM}_A going HIGH to R/\overline{W}_B or \overline{SEM}_B going HIGH.
4. If t_{SPS} is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will be granted the semaphore flag.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

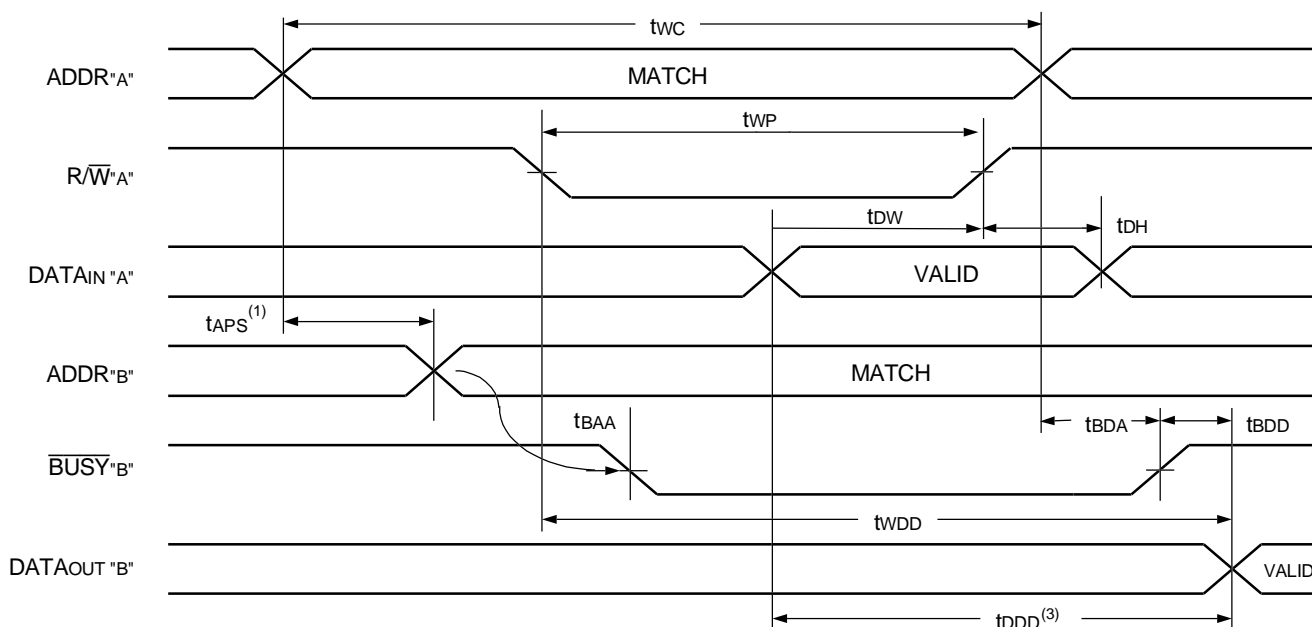
		70V18L15 Com'l Only		70V18L20 Com'l & Ind		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
BUSY TIMING (M/S=V _{IH})						
t _{BAA}	BUSY Access Time from Address Match	—	15	—	20	ns
t _{BDA}	BUSY Disable Time from Address Not Matched	—	15	—	20	ns
t _{BAC}	BUSY Access Time from Chip Enable Low	—	15	—	20	ns
t _{BDC}	BUSY Access Time from Chip Enable High	—	15	—	17	ns
t _{APS}	Arbitration Priority Set-up Time ⁽²⁾	5	—	5	—	ns
t _{BDD}	BUSY Disable to Valid Data ⁽³⁾	—	15	—	17	ns
t _{WH}	Write Hold After BUSY ⁽⁵⁾	12	—	15	—	ns
BUSY TIMING (M/S=V _{IL})						
t _{WB}	BUSY Input to Write ⁽⁴⁾	0	—	0	—	ns
t _{WH}	Write Hold After BUSY ⁽⁵⁾	12	—	15	—	ns
PORT-TO-PORT DELAY TIMING						
t _{WDD}	Write Pulse to Data Delay ⁽¹⁾	—	30	—	45	ns
t _{DDD}	Write Data Valid to Read Data Delay ⁽¹⁾	—	25	—	30	ns

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NOTES:

- Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{\text{BUSY}}$ (M/ \bar{S} = V_{IH})".
- To ensure that the earlier of the two ports wins.
- t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} – t_{WP} (actual), or t_{DDD} – t_{WR} (actual).
- To ensure that the write cycle is inhibited on port "B" during contention on port "A".
- To ensure that a write cycle is completed on port "B" after contention on port "A".

Timing Waveform of Write with Port-to-Port Read and $\overline{\text{BUSY}}$ ($\text{M}/\overline{\text{S}} = \text{V}_{\text{IH}}$)^(2,4,5)

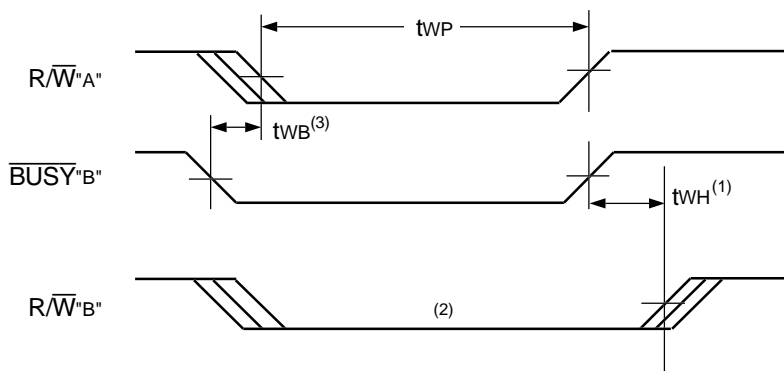


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NOTES:

1. To ensure that the earlier of the two ports wins, t_{APS} is ignored for $\text{M}/\overline{\text{S}} = \text{V}_{\text{IL}}$ (SLAVE).
2. $\overline{\text{CE}}_{\text{L}} = \overline{\text{CE}}_{\text{R}} = \text{V}_{\text{IL}}$, refer to Chip Enable Truth Table.
3. $\overline{\text{OE}} = \text{V}_{\text{IL}}$ for the reading port.
4. If $\text{M}/\overline{\text{S}} = \text{V}_{\text{IL}}$ (slave), $\overline{\text{BUSY}}$ is an input. Then for this example $\overline{\text{BUSY}}_{\text{A}} = \text{V}_{\text{IH}}$ and $\overline{\text{BUSY}}_{\text{B}}$ input is shown above.
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

Timing Waveform of Write with $\overline{\text{BUSY}}$ ($\text{M}/\overline{\text{S}} = \text{V}_{\text{IL}}$)

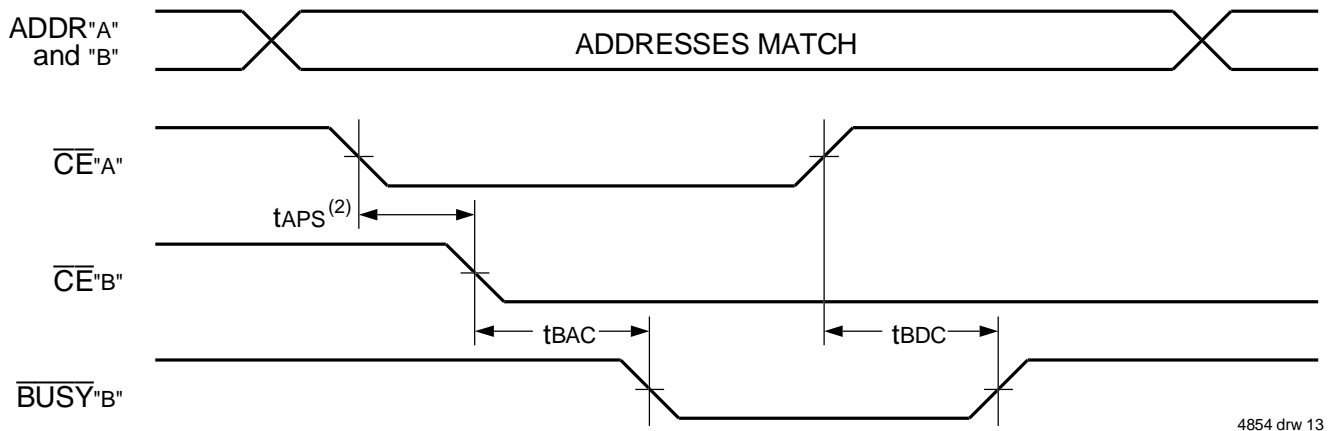


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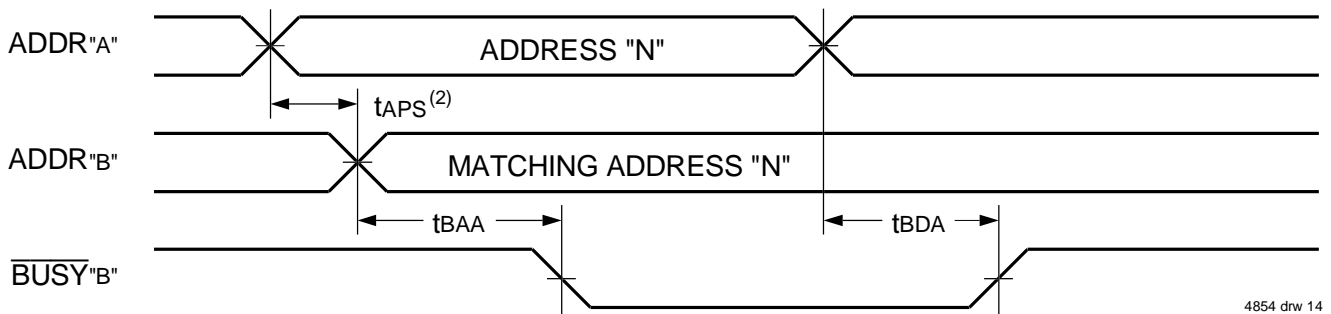
NOTES:

1. t_{WH} must be met for both $\overline{\text{BUSY}}$ input (SLAVE) and output (MASTER).
2. $\overline{\text{BUSY}}$ is asserted on port "B" blocking $\text{R}/\overline{\text{W}}_{\text{B}}$, until $\overline{\text{BUSY}}_{\text{B}}$ goes HIGH.
3. t_{WB} is only for the 'slave' version.

Waveform of $\overline{\text{BUSY}}$ Arbitration Controlled by $\overline{\text{CE}}$ Timing ($\text{M}/\overline{\text{S}} = \text{V}_{\text{IH}}$)^(1,3)



Waveform of $\overline{\text{BUSY}}$ Arbitration Cycle Controlled by Address Match Timing ($\text{M}/\overline{\text{S}} = \text{V}_{\text{IH}}$)⁽¹⁾



NOTES:

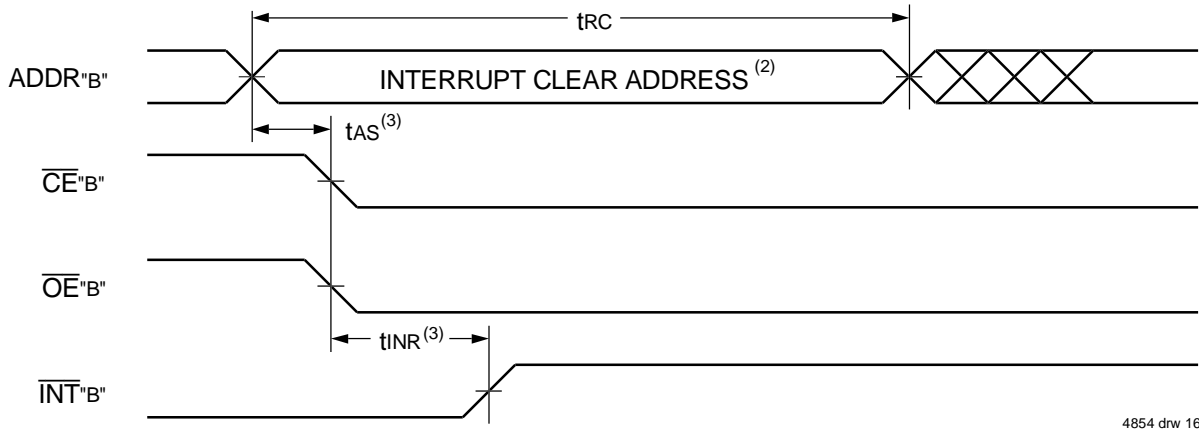
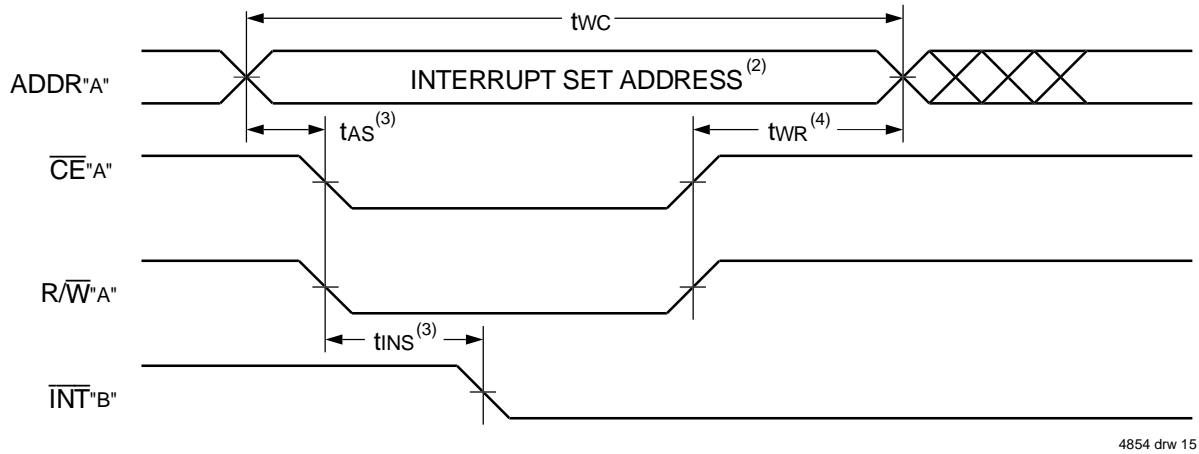
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the $\overline{\text{BUSY}}$ signal will be asserted on one side or another but there is no guarantee on which side $\overline{\text{BUSY}}$ will be asserted.
3. Refer to Truth Table I - Chip Enable.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

		70V18L15 Com'l Only		70V18L20 Com'l & Ind		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
INTERRUPT TIMING						
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tINS	Interrupt Set Time	—	15	—	20	ns
tINR	Interrupt Reset Time	—	15	—	20	ns

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Waveform of Interrupt Timing^(1,5)



NOTES:

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. Refer to Interrupt Truth Table.
3. Timing depends on which enable signal (\overline{CE} or R/\overline{W}) is asserted last.
4. Timing depends on which enable signal (\overline{CE} or R/\overline{W}) is de-asserted first.
5. Refer to Truth Table I - Chip Enable.

Truth Table IV — Interrupt Flag^(1,4,5)

Left Port					Right Port					Function
R/\overline{W}_L	\overline{CE}_L	\overline{OE}_L	A15L-A0L	\overline{INT}_L	R/\overline{W}_R	\overline{CE}_R	\overline{OE}_R	A15R-A0R	\overline{INT}_R	
L	L	X	FFFF	X	X	X	X	X	L ⁽²⁾	Set Right \overline{INT}_R Flag
X	X	X	X	X	X	L	L	FFFF	H ⁽³⁾	Reset Right \overline{INT}_R Flag
X	X	X	X	L ⁽³⁾	L	L	X	FFFE	X	Set Left \overline{INT}_L Flag
X	L	L	FFFE	H ⁽²⁾	X	X	X	X	X	Reset Left \overline{INT}_L Flag

NOTES:

1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$.
2. If $\overline{BUSY}_L = V_{IL}$, then no change.
3. If $\overline{BUSY}_R = V_{IL}$, then no change.
4. \overline{INT}_L and \overline{INT}_R must be initialized at power-up.
5. Refer to Truth Table I - Chip Enable.

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**Truth Table V —
Address $\overline{\text{BUSY}}$ Arbitration⁽⁴⁾**

Inputs			Outputs		Function
$\overline{\text{CE}}_{\text{L}}$	$\overline{\text{CE}}_{\text{R}}$	A _{0L} -A _{15L} A _{0R} -A _{15R}	$\overline{\text{BUSY}}_{\text{L}}^{(1)}$	$\overline{\text{BUSY}}_{\text{R}}^{(1)}$	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit ⁽³⁾

4854 tbl 17

NOTES:

1. Pins $\overline{\text{BUSY}}_{\text{L}}$ and $\overline{\text{BUSY}}_{\text{R}}$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{\text{BUSY}}$ outputs on the IDT70V18 are push-pull, not open drain outputs. On slaves the $\overline{\text{BUSY}}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If taps is not met, either $\overline{\text{BUSY}}_{\text{L}}$ or $\overline{\text{BUSY}}_{\text{R}}$ = LOW will result. $\overline{\text{BUSY}}_{\text{L}}$ and $\overline{\text{BUSY}}_{\text{R}}$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{\text{BUSY}}_{\text{L}}$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{\text{BUSY}}_{\text{R}}$ outputs are driving LOW regardless of actual logic level on the pin.
4. Refer to Truth Table I - Chip Enable.

Truth Table VI — Example of Semaphore Procurement Sequence^(1,2,3)

Functions	Do - D ₈ Left	Do - D ₈ Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

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NOTES:

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70V18.
2. There are eight semaphore flags written to via I/O₀ and read from all I/O's (I/O₀-I/O₈). These eight semaphores are addressed by A₀ - A₂.
3. $\overline{\text{CE}} = \text{V}_{\text{IH}}$, $\overline{\text{SEM}} = \text{V}_{\text{IL}}$ to access the semaphores. Refer to Truth Table III - Semaphore Read/Write Control.

Functional Description

The IDT70V18 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V18 has an automatic power down feature controlled by $\overline{\text{CE}}$. The $\overline{\text{CE}}_0$ and $\overline{\text{CE}}_1$ control the on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{\text{CE}} = \text{V}_{\text{IH}}$). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{\text{INT}}_{\text{L}}$) is asserted when the right port writes to memory location

FFFF (HEX), where a write is defined as $\overline{\text{CE}}_{\text{R}} = \text{R}/\overline{\text{W}}_{\text{R}} = \text{V}_{\text{IL}}$ per the Truth Table. The left port clears the interrupt through access of address location FFFE when $\overline{\text{CE}}_{\text{L}} = \overline{\text{OE}}_{\text{L}} = \text{V}_{\text{IL}}$, $\text{R}/\overline{\text{W}}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{\text{INT}}_{\text{R}}$) is asserted when the left port writes to memory location FFFF (HEX) and to clear the interrupt flag ($\overline{\text{INT}}_{\text{R}}$), the right port must read the memory location FFFF. The message (9 bits) at FFFE or FFFF is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations FFFE and FFFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table IV for the interrupt operation.

The BUSY outputs on the IDT70V18 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the BUSY indication for the resulting array requires the use of an external AND gate.



The **BUSY** arbitration on a master is based on the chip enable and

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then

verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT70V18 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{\text{SEM}}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{\text{CE}}$, and $\overline{\text{RW}}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table VI). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{\text{SEM}}$) and output enable ($\overline{\text{OE}}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{\text{SEM}}$ or $\overline{\text{OE}}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table VI). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in

question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will

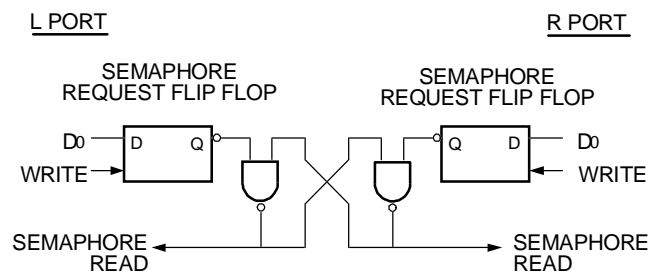


Figure 4. IDT70V18 Semaphore Logic

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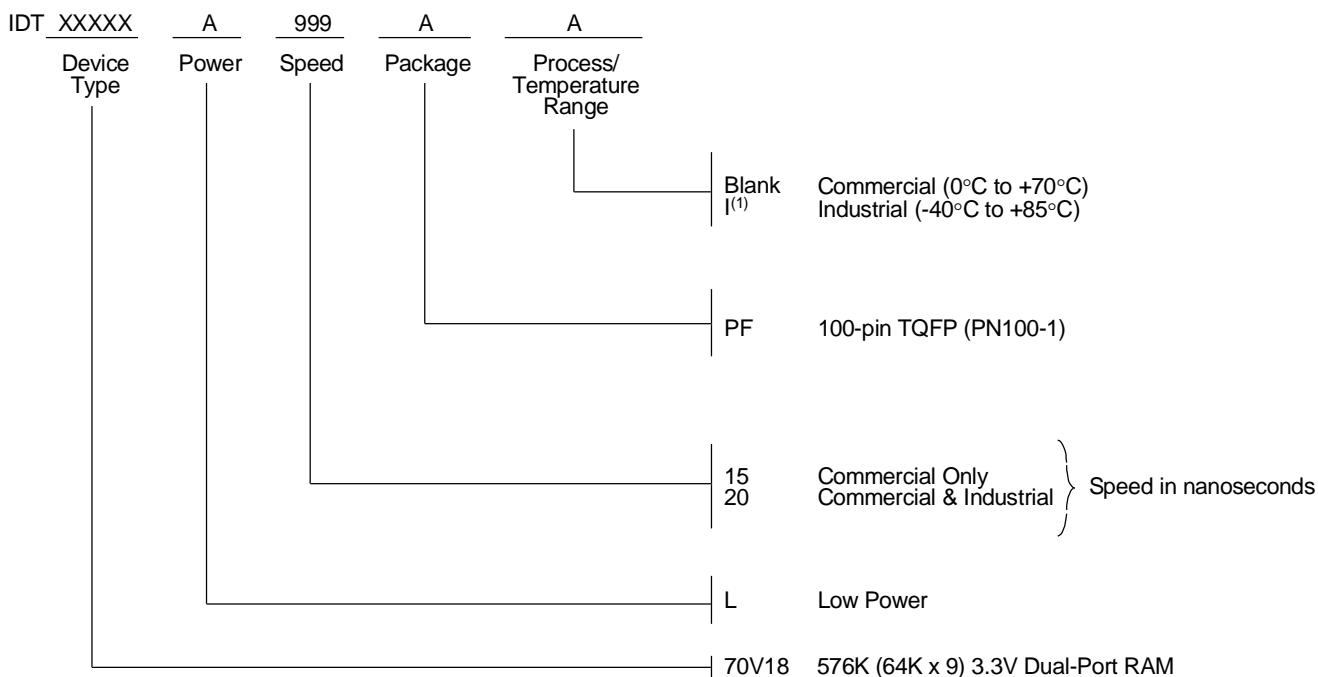
continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Ordering Information



NOTE:

1. Contact your sales office for Industrial Temperature range in other speeds, packages and powers.

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Preliminary Datasheet:

"PRELIMINARY" datasheets contain descriptions for products that are in early release.

Datasheet Document History:

- 9/30/99: Initial Public Offering
- 11/10/99: Page 1 & 17 Replaced IDT logo
- 4/10/00: Page 2 Fixed incorrect pin number
- 1/02/02: Page 3 Increased storage temperature parameter
Clarified TA parameter
- Page 4 Fixed I/Os in notes
- Page 5 DC Electrical parameters—changed wording from "open" to "disabled"
Added Truth Table I - Chip Enable as note 5
- Page 6 Fixed 5pF* in drawing 04
- Page 7 Corrected ±200mV to 0mV in notes
- Pages 5, 7, 10 & 12 Added industrial temperature range for 20ns to DC & AC Electrical Characteristics
- Page 3, 5, 7, 10 & 12 Removed industrial temp option footnote from all tables
- Page 1 & 17 Replace IDT TM logo with IDT [®] logo



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