



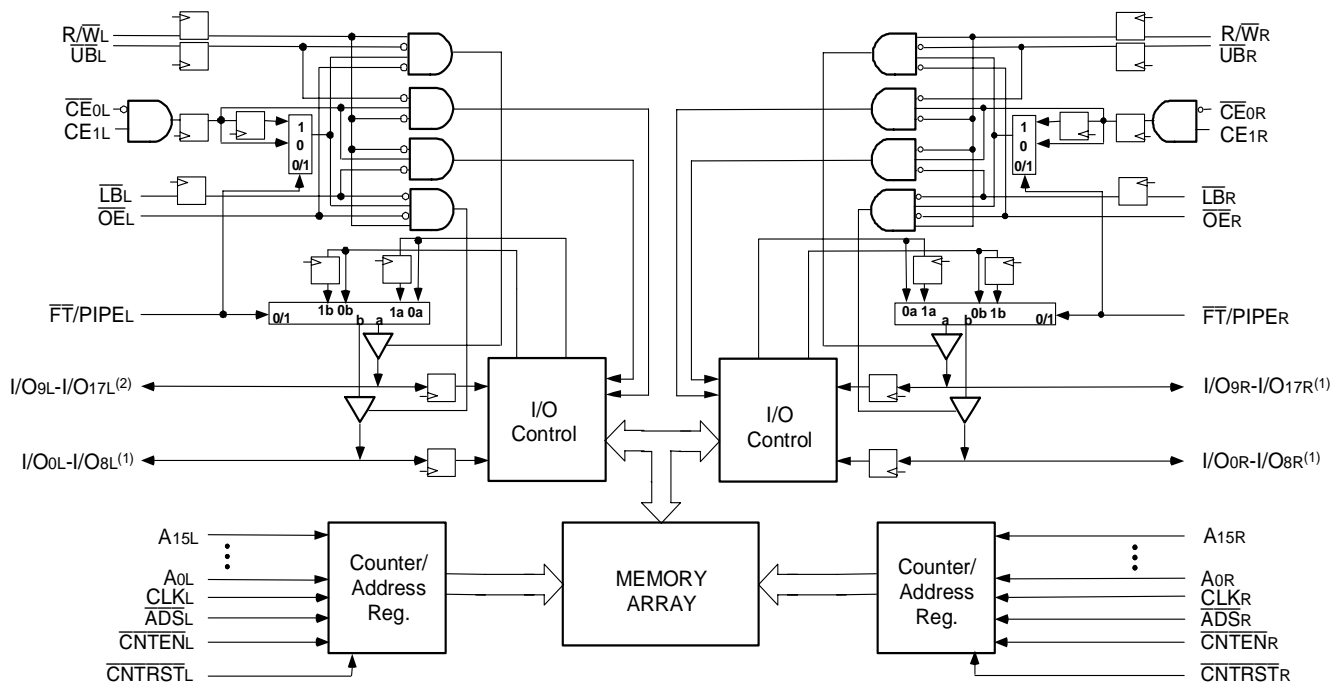
HIGH-SPEED 3.3V 64K x18/x16 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM

IDT70V9389/289L

Features:

- ♦ True Dual-Ported memory cells which allow simultaneous access of the same memory location
- ♦ High-speed clock to data access
 - Commercial: 6/7.5/9/12ns (max.)
 - Industrial: 9ns (max.)
- ♦ Low-power operation
 - IDT70V9389/289L
 - Active: 500mW (typ.)
 - Standby: 1.5mW (typ.)
- ♦ Flow-Through or Pipelined output mode on either port via the $\overline{\text{FT}}/\text{PIPE}$ pins
- ♦ Counter enable and reset features
- ♦ Dual chip enables allow for depth expansion without additional logic
- ♦ Full synchronous operation on both ports
 - 3.5ns setup to clock and 0ns hold on all control, data, and address inputs
 - Data input, address, and control registers
 - Fast 6.5ns clock to data out in the Pipelined output mode
 - Self-timed write allows fast cycle time
 - 10ns cycle time, 100MHz operation in Pipelined output mode
- ♦ Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility
- ♦ LVTTTL-compatible, single 3.3V ($\pm 0.3\text{V}$) power supply
- ♦ Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available for selected speeds
- ♦ Available in a 128-pin Thin Quad Flatpack (TQFP) and 100-pin Thin Quad Flatpack (TQFP)

Functional Block Diagram

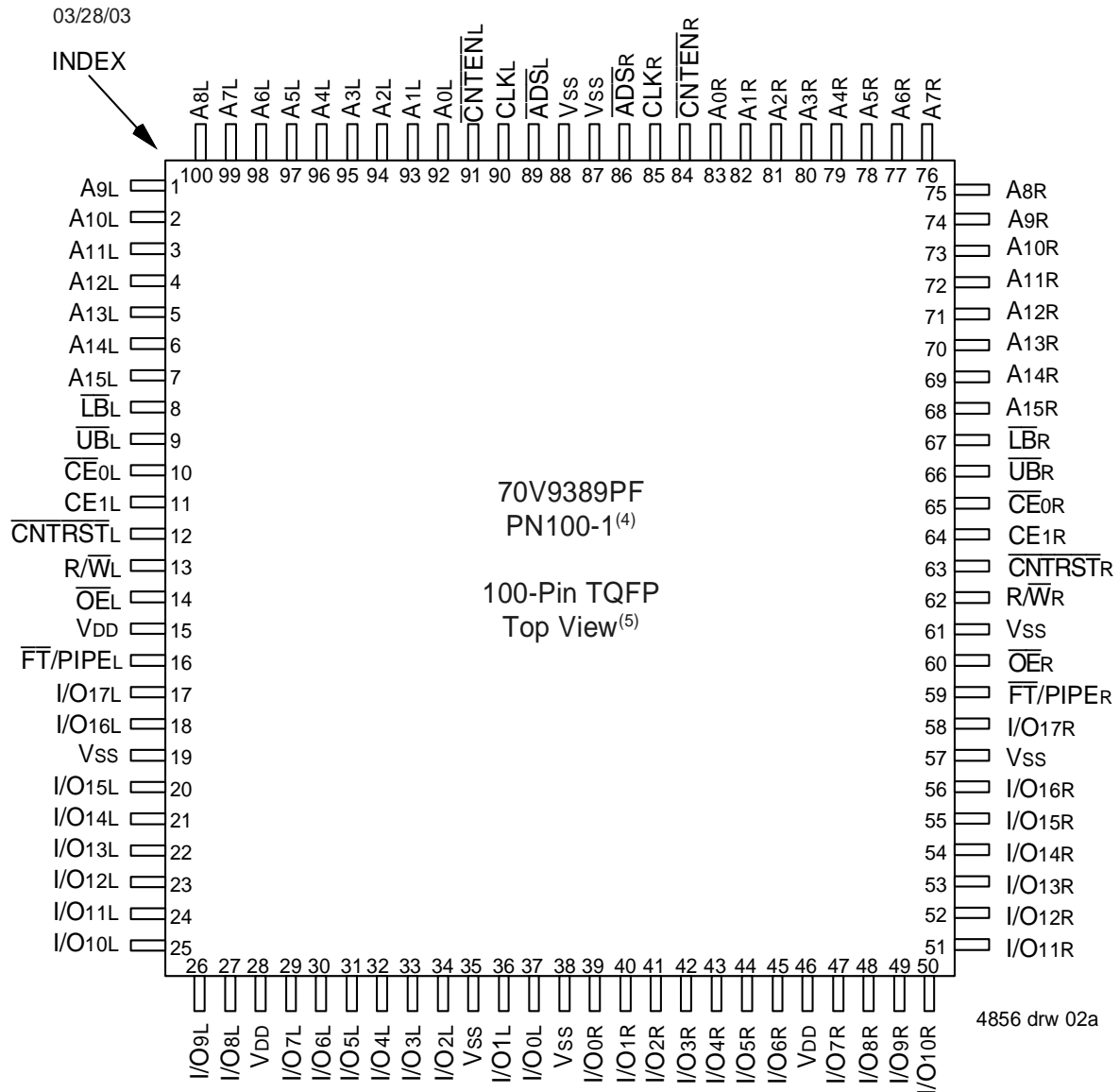


4856 drw 01

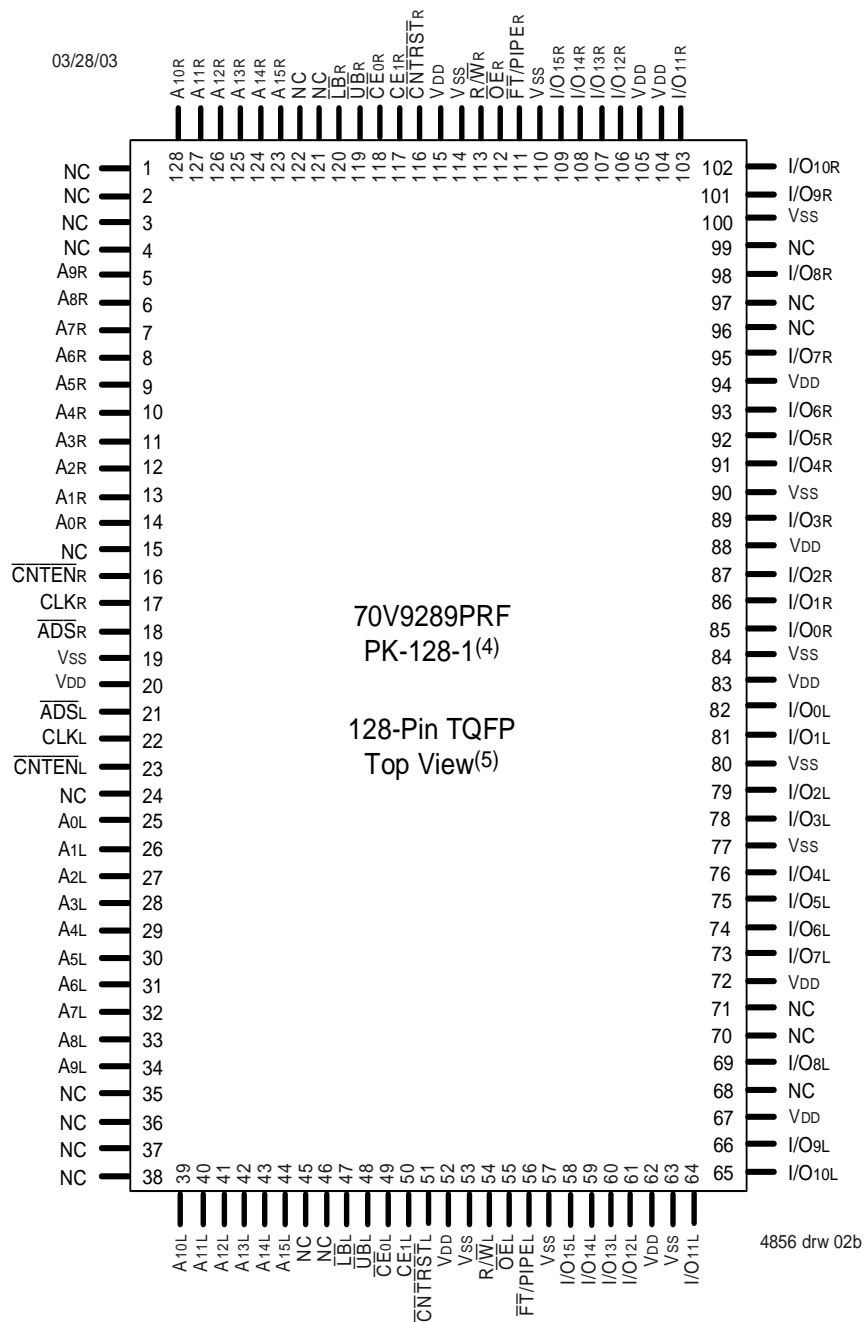
NOTE:

1. I/O0x - I/O7x for IDT70V9289.
2. I/O8x - I/O15x for IDT70V9289.

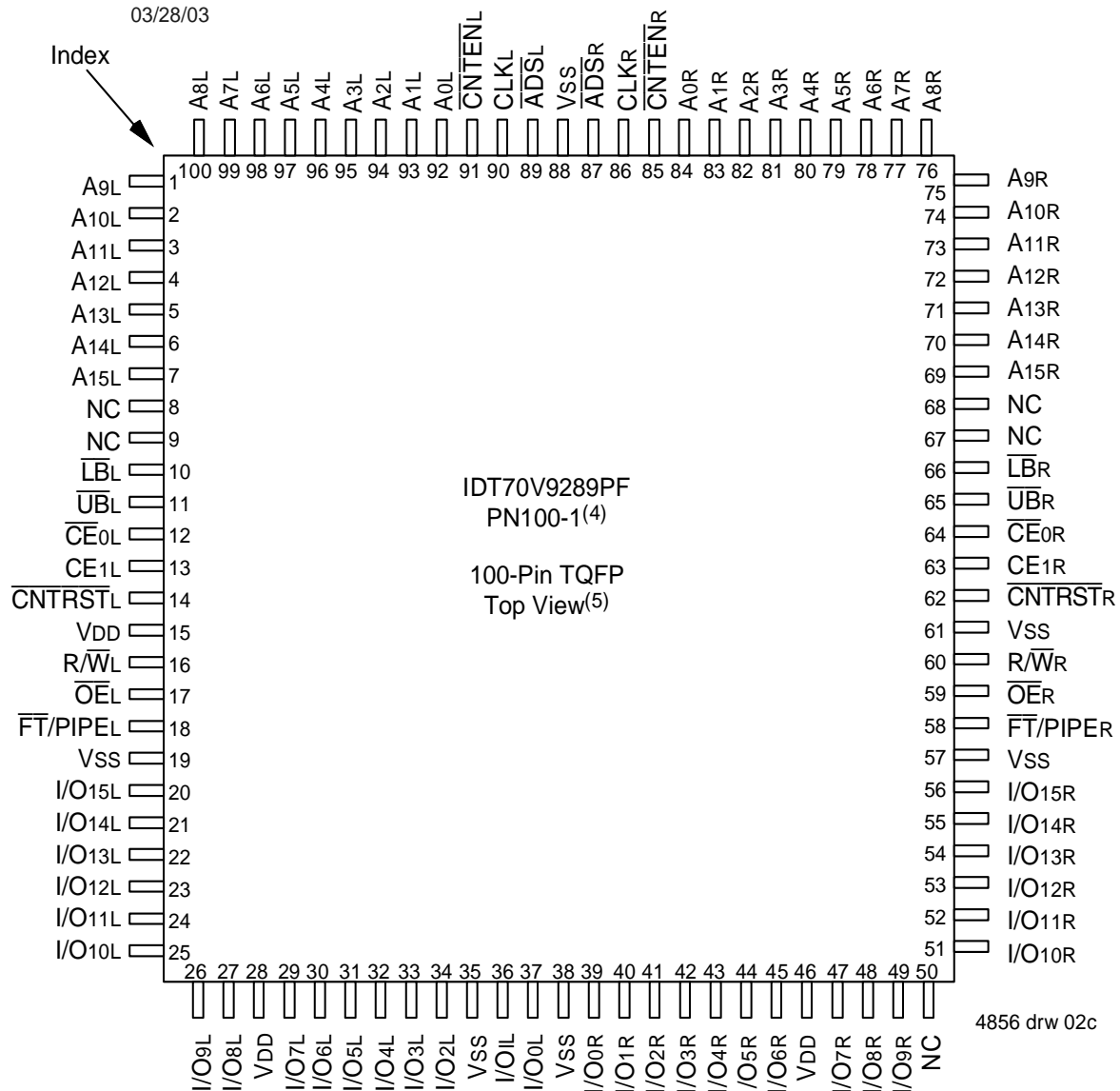
APRIL 2003

Pin Configurations^(1,2,3)(con't.)**NOTES:**

1. All V_{DD} pins must be connected to power supply.
2. All V_{SS} pins must be connected to ground.
3. Package body is approximately 14mm x 14mm x 1.4mm
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations^(1,2,3)(con't.)**NOTES:**

1. All VDD pins must be connected to power supply.
2. All VSS pins must be connected to ground.
3. Package body is approximately 14mm x 20mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations^(1,2,3)(con't.)**NOTES:**

1. All V_{DD} pins must be connected to power supply.
2. All V_{SS} pins must be connected to ground.
3. Package body is approximately 14mm x 14mm x 1.4mm
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}0L$, CE1L	$\overline{CE}0R$, CE1R	Chip Enables ⁽³⁾
R/ \overline{WL}	R/ \overline{WR}	Read/Write Enable
$\overline{OE}L$	$\overline{OE}R$	Output Enable
A0L - A15L	A0R - A15R	Address
I/O0L - I/O17L ⁽¹⁾	I/O0R - I/O17R ⁽¹⁾	Data Input/Output
CLKL	CLKR	Clock
$\overline{UB}L$	$\overline{UB}R$	Upper Byte Select ⁽²⁾
$\overline{LB}L$	$\overline{LB}R$	Lower Byte Select ⁽²⁾
$\overline{ADS}L$	$\overline{ADS}R$	Address Strobe Enable
$\overline{CNTEN}L$	$\overline{CNTEN}R$	Counter Enable
$\overline{CNTRST}L$	$\overline{CNTRST}R$	Counter Reset
$\overline{FT}/PIPEL$	$\overline{FT}/PIPER$	Flow-Through / Pipeline
VDD		Power (3.3V)
VSS		Ground (0V)

4856 tbl 01

NOTE:

1. I/O0x - I/O15x for IDT70V9289.
2. \overline{LB} and \overline{UB} are single buffered regardless of state of $\overline{FT}/PIPE$.
3. $\overline{CE}0$ and CE1 are single buffered when $\overline{FT}/PIPE = V_{IL}$,
 $\overline{CE}0$ and CE1 are double buffered when $\overline{FT}/PIPE = V_{IH}$,
i.e. the signals take two cycles to deselect.

Truth Table I—Read/Write and Enable Control^(1,2,3)

\overline{OE}	CLK	$\overline{CE}0^{(5)}$	CE1 ⁽⁵⁾	$\overline{UB}^{(4)}$	$\overline{LB}^{(4)}$	R/ \overline{W}	Upper Byte I/O9-17 ⁽⁶⁾	Lower Byte I/O0-8 ⁽⁷⁾	MODE
X	↑	H	X	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	X	High-Z	High-Z	Both Bytes Deselected
X	↑	L	H	L	H	L	DIN	High-Z	Write to Upper Byte Only
X	↑	L	H	H	L	L	High-Z	DATAIN	Write to Lower Byte Only
X	↑	L	H	L	L	L	DATAIN	DATAIN	Write to Both Bytes
L	↑	L	H	L	H	H	DATAOUT	High-Z	Read Upper Byte Only
L	↑	L	H	H	L	H	High-Z	DATAOUT	Read Lower Byte Only
L	↑	L	H	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
H	X	L	H	L	L	X	High-Z	High-Z	Outputs Disabled

4856 tbl 02

NOTES:

1. "H" = V_{IH} , "L" = V_{IL} , "X" = Don't Care.
2. \overline{ADS} , \overline{CNTEN} , \overline{CNTRST} = X.
3. \overline{OE} is an asynchronous input signal.
4. \overline{LB} and \overline{UB} are single buffered regardless of state of $\overline{FT}/PIPE$.
5. $\overline{CE}0$ and CE1 are single buffered when $\overline{FT}/PIPE = V_{IL}$. $\overline{CE}0$ and CE1 are double buffered when $\overline{FT}/PIPE = V_{IH}$, i.e. the signals take two cycles to deselect.
6. I/O8 - I/O15 for IDT70V9289.
7. I/O0 - I/O7 for IDT70V9289.

Truth Table II—Address Counter Control^(1,2)

External Address	Previous Internal Address	Internal Address Used	CLK	$\overline{\text{ADS}}$	$\overline{\text{CNTEN}}$	$\overline{\text{CNRST}}$	I/O ⁽³⁾	MODE
X	X	0	↑	X	X	L ⁽⁴⁾	D/I/O(0)	Counter Reset to Address 0
A _n	X	A _n	↑	L ⁽⁴⁾	X	H	D/I/O(n)	External Address Loaded into Counter
A _n	A _p	A _p	↑	H	H	H	D/I/O(p)	External Address Blocked—Counter disabled (A _p reused)
X	A _p	A _p + 1	↑	H	L ⁽⁵⁾	H	D/I/O(p+1)	Counter Enabled—Internal Address generation

NOTES:

4856 tbl 03

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- $\overline{\text{CE0}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$, and $\overline{\text{OE}}$ = V_{IL}; CE1 and R/W = V_{IH}.
- Outputs configured in Flow-Through Output mode; if outputs are in Pipelined mode the data out will be delayed by one cycle.
- $\overline{\text{ADS}}$ and $\overline{\text{CNRST}}$ are independent of all other signals including $\overline{\text{CE0}}$, CE1, $\overline{\text{UB}}$ and $\overline{\text{LB}}$.
- The address counter advances if $\overline{\text{CNTEN}}$ = V_{IL} on the rising edge of CLK, regardless of all other signals including $\overline{\text{CE0}}$, CE1, $\overline{\text{UB}}$ and $\overline{\text{LB}}$.

Recommended Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature ⁽²⁾	GND	V _{DD}
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

4856 tbl 04

NOTES:

- This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	3.0	3.3	3.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.0	—	V _{DD} +0.3V ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

4856 tbl 05

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10 ns.
- V_{TERM} must not exceed V_{DD} +0.3V.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T _{BIAS} ⁽³⁾	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
T _{JN}	Junction Temperature	+150	°C
I _{OUT}	DC Output Current	50	mA

4856 tbl 06

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{DD} +0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ V_{DD} + 0.3V.
- Ambient Temperature Under DC Bias. No AC Conditions. Chip Deselected.

**Capacitance⁽¹⁾
(T_A = +25°C, f = 1.0MHz)**

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	9	pF
C _{OUT} ⁽³⁾	Output Capacitance	V _{OUT} = 3dV	10	pF

4856 tbl 07

NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C_{OUT} also references C_{I/O}.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD} = 3.3V \pm 0.3V$)

Symbol	Parameter	Test Conditions	70V9389/289L		Unit
			Min.	Max.	
$ I_{LI} $	Input Leakage Current ⁽¹⁾	$V_{DD} = 3.6V$, $V_{IN} = 0V$ to V_{DD}	—	5	μA
$ I_{LO} $	Output Leakage Current	$\overline{CE} = V_{IH}$ or $CE_1 = V_{IL}$, $V_{OUT} = 0V$ to V_{DD}	—	5	μA
V_{OL}	Output Low Voltage	$I_{OL} = +4mA$	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4mA$	2.4	—	V

NOTE:

4856 tbl 08

1. At $V_{DD} \leq 2.0V$ input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range⁽³⁾ ($V_{DD} = 3.3V \pm 0.3V$)

Symbol	Parameter	Test Condition	Version	70V9389/289L6 Com'l Only		70V9389/289L7 Com'l Only		70V9389/289L9 Com'l & Ind		70V9389/289L12 Com'l Only		Unit
				Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	
IDD	Dynamic Operating Current (Both Ports Active)	\overline{CE}_L and $\overline{CE}_R = V_{IL}$, Outputs Disabled, $f = f_{MAX}$ ⁽¹⁾	COM'L L	220	280	200	250	175	230	150	200	mA
			IND L	—	—	—	—	180	240	—	—	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}$ ⁽¹⁾	COM'L L	60	85	50	75	40	65	30	50	mA
			IND L	—	—	—	—	50	70	—	—	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}$ ⁽⁵⁾ Active Port Outputs Disabled, $f = f_{MAX}$ ⁽¹⁾	COM'L L	145	185	130	165	110	145	95	130	mA
			IND L	—	—	—	—	110	155	—	—	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$ ⁽²⁾	COM'L L	0.4	2	0.4	2	0.4	2	0.4	2	mA
			IND L	—	—	—	—	0.4	2	—	—	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^*A \leq 0.2V$ and $\overline{CE}^*B \geq V_{DD} - 0.2V$ ⁽⁵⁾ $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port, Outputs Disabled, $f = f_{MAX}$ ⁽¹⁾	COM'L L	145	180	130	160	100	140	90	125	mA
			IND L	—	—	—	—	100	155	—	—	

4856 tbl 09

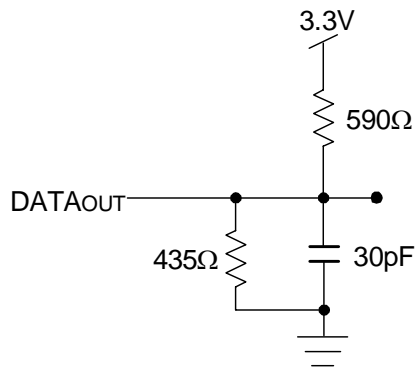
NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{CYC}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{DD} pc(f=0) = 90mA$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{DD} - 0.2V$
 $\overline{CE}_X \geq V_{DD} - 0.2V$ means $\overline{CE}_{0X} \geq V_{CC} - 0.2V$ or $CE_{1X} \leq 0.2V$
 "X" represents "L" for left port or "R" for right port.

AC Test Conditions

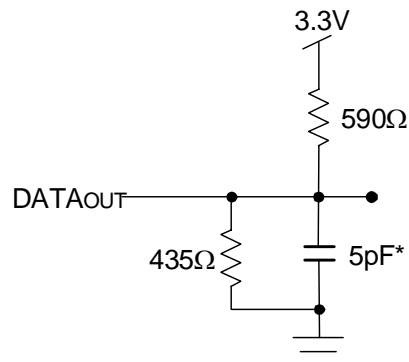
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2, and 3

4856 tbl 10



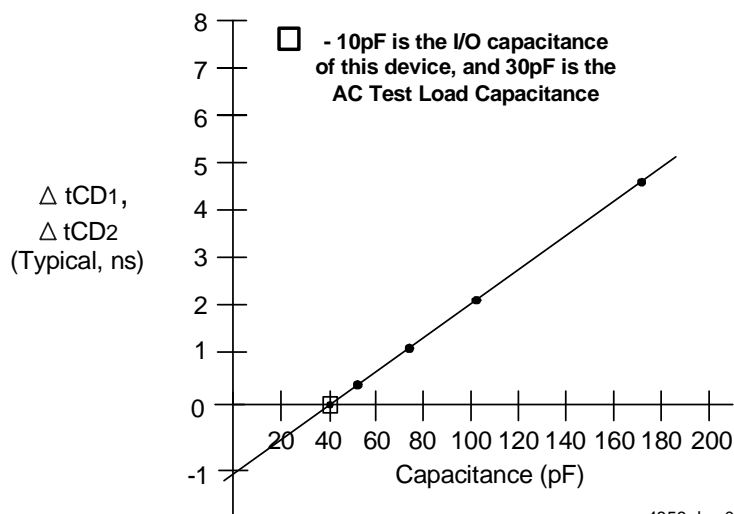
4856 drw 03

Figure 1. AC Output Test load.



4856 drw 04

Figure 2. Output Test Load
(For tCKLZ, tCKHZ, tOLZ, and tOHZ).
*Including scope and jig.



4856 drw 05

Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)⁽³⁾ ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$)

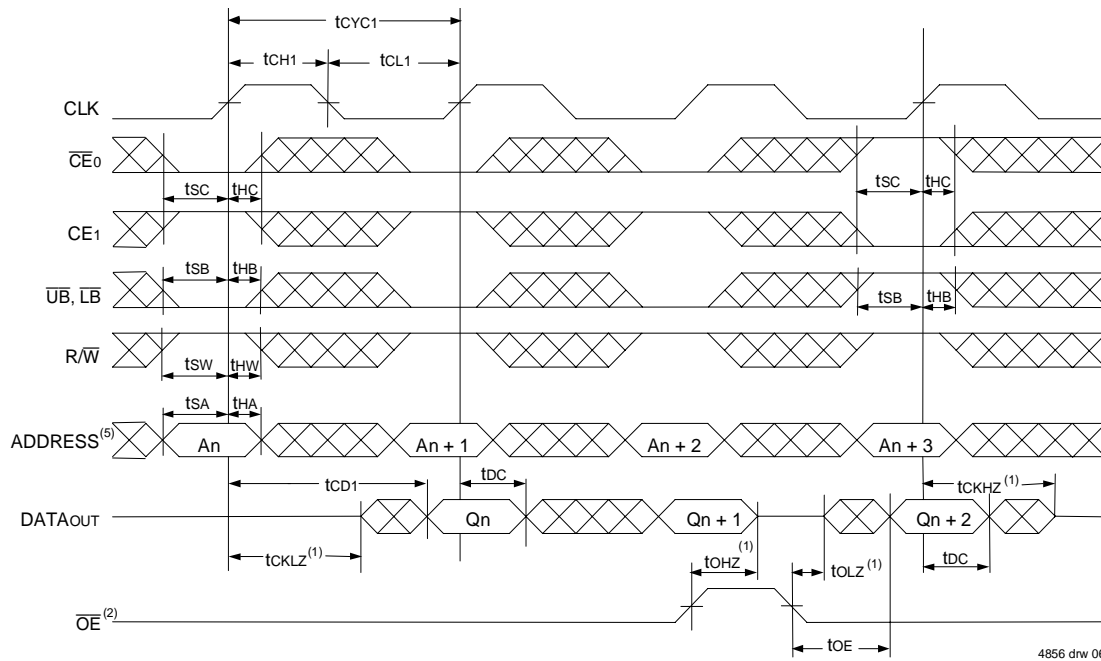
Symbol	Parameter	70V9389/289L6 Com'l Only		70V9389/289L7 Com'l Only		70V9389/289L9 Com'l & Ind		70V9389/289L12 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tcyc1	Clock Cycle Time (Flow-Through) ⁽²⁾	19	—	22	—	25	—	30	—	ns
tcyc2	Clock Cycle Time (Pipelined) ⁽²⁾	10	—	12	—	15	—	20	—	ns
tch1	Clock High Time (Flow-Through) ⁽²⁾	6.5	—	7.5	—	12	—	12	—	ns
tcl1	Clock Low Time (Flow-Through) ⁽²⁾	6.5	—	7.5	—	12	—	12	—	ns
tch2	Clock High Time (Pipelined) ⁽²⁾	4	—	5	—	6	—	8	—	ns
tcl2	Clock Low Time (Pipelined) ⁽²⁾	4	—	5	—	6	—	8	—	ns
tr	Clock Rise Time	—	3	—	3	—	3	—	3	ns
tf	Clock Fall Time	—	3	—	3	—	3	—	3	ns
tSA	Address Setup Time	3.5	—	4	—	4	—	4	—	ns
tHA	Address Hold Time	0	—	0	—	1	—	1	—	ns
tSC	Chip Enable Setup Time	3.5	—	4	—	4	—	4	—	ns
tHC	Chip Enable Hold Time	0	—	0	—	1	—	1	—	ns
tSB	Byte Enable Setup Time	3.5	—	4	—	4	—	4	—	ns
tHB	Byte Enable Hold Time	0	—	0	—	1	—	1	—	ns
tSW	R/W Setup Time	3.5	—	4	—	4	—	4	—	ns
tHW	R/W Hold Time	0	—	0	—	1	—	1	—	ns
tSD	Input Data Setup Time	3.5	—	4	—	4	—	4	—	ns
tHD	Input Data Hold Time	0	—	0	—	1	—	1	—	ns
tSAD	\overline{ADS} Setup Time	3.5	—	4	—	4	—	4	—	ns
tHAD	\overline{ADS} Hold Time	0	—	0	—	1	—	1	—	ns
tSCN	\overline{CNTEN} Setup Time	3.5	—	4	—	4	—	4	—	ns
tHCN	\overline{CNTEN} Hold Time	0	—	0	—	1	—	1	—	ns
tSRST	\overline{CNRST} Setup Time	3.5	—	4	—	4	—	4	—	ns
tHRST	\overline{CNRST} Hold Time	0	—	0	—	1	—	1	—	ns
toE	Output Enable to Data Valid	—	6.5	—	7.5	—	9	—	12	ns
tolZ	Output Enable to Output Low-Z ⁽¹⁾	2	—	2	—	2	—	2	—	ns
toHZ	Output Enable to Output High-Z ⁽¹⁾	1	7	1	7	1	7	1	7	ns
tcd1	Clock to Data Valid (Flow-Through) ⁽²⁾	—	15	—	18	—	20	—	25	ns
tcd2	Clock to Data Valid (Pipelined) ⁽²⁾	—	6.5	—	7.5	—	9	—	12	ns
tDC	Data Output Hold After Clock High	2	—	2	—	2	—	2	—	ns
tCKHZ	Clock High to Output High-Z ⁽¹⁾	2	9	2	9	2	9	2	9	ns
tCKLZ	Clock High to Output Low-Z ⁽¹⁾	2	—	2	—	2	—	2	—	ns
Port-to-Port Delay										
tcWDD	Write Port Clock High to Read Data Delay	—	24	—	28	—	35	—	40	ns
tCCS	Clock-to-Clock Setup Time	—	9	—	10	—	15	—	15	ns

NOTES:

4866 tbl 11

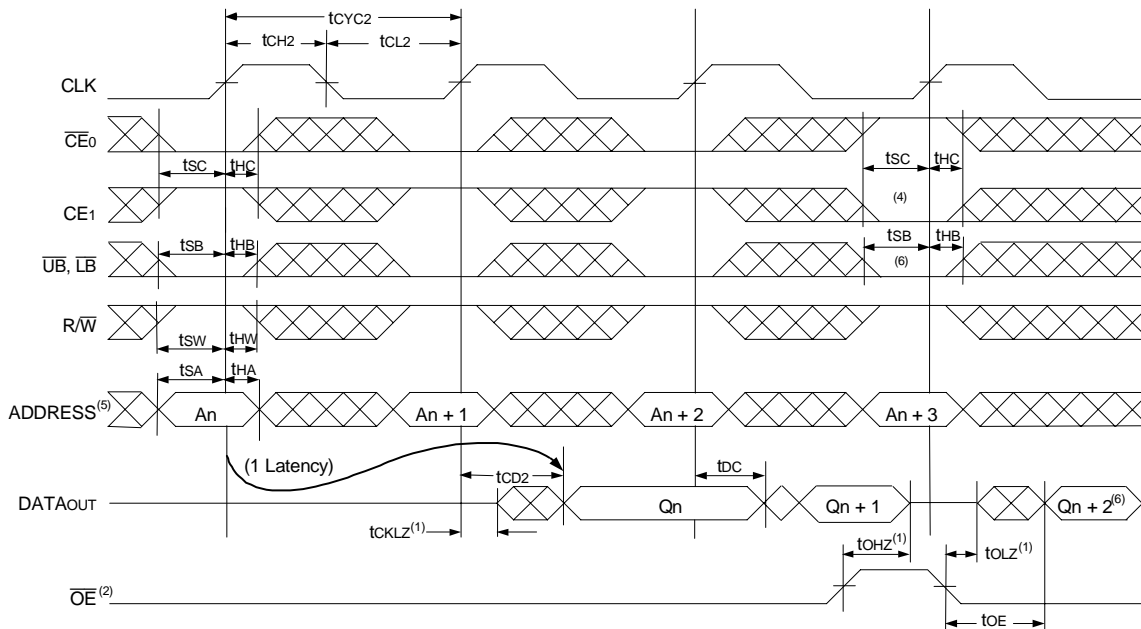
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (tcyc2, tcd2) apply to either or both the Left and Right ports when $\overline{FT}/PIPE = V_{IH}$. Flow-through parameters (tcyc1, tcd1) apply when $\overline{FT}/PIPE = V_{IL}$ for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (\overline{OE}), $\overline{FT}/PIPE_R$, and $\overline{FT}/PIPE_L$.

Timing Waveform of Read Cycle for Flow-Through Output ($\overline{FT}/PIPE^*X = V_{IL}$)^(3,7)



4856 drw 06

Timing Waveform of Read Cycle for Pipelined Operation ($\overline{FT}/PIPE^*X = V_{IH}$)^(3,7)

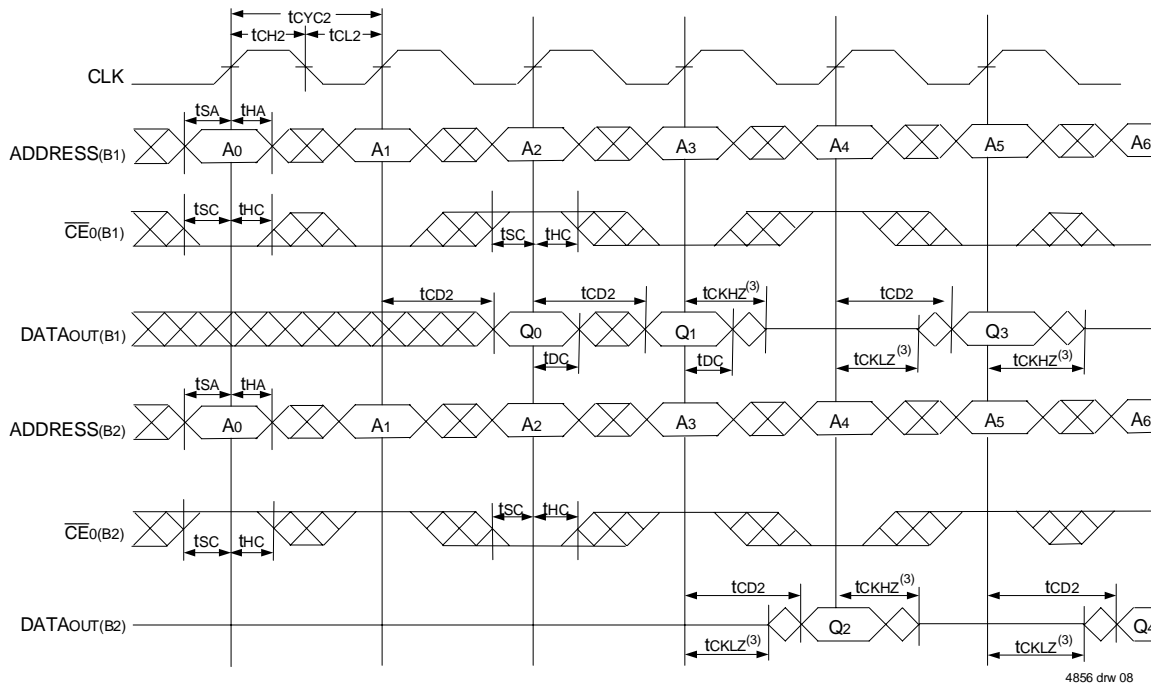


4856 drw 07

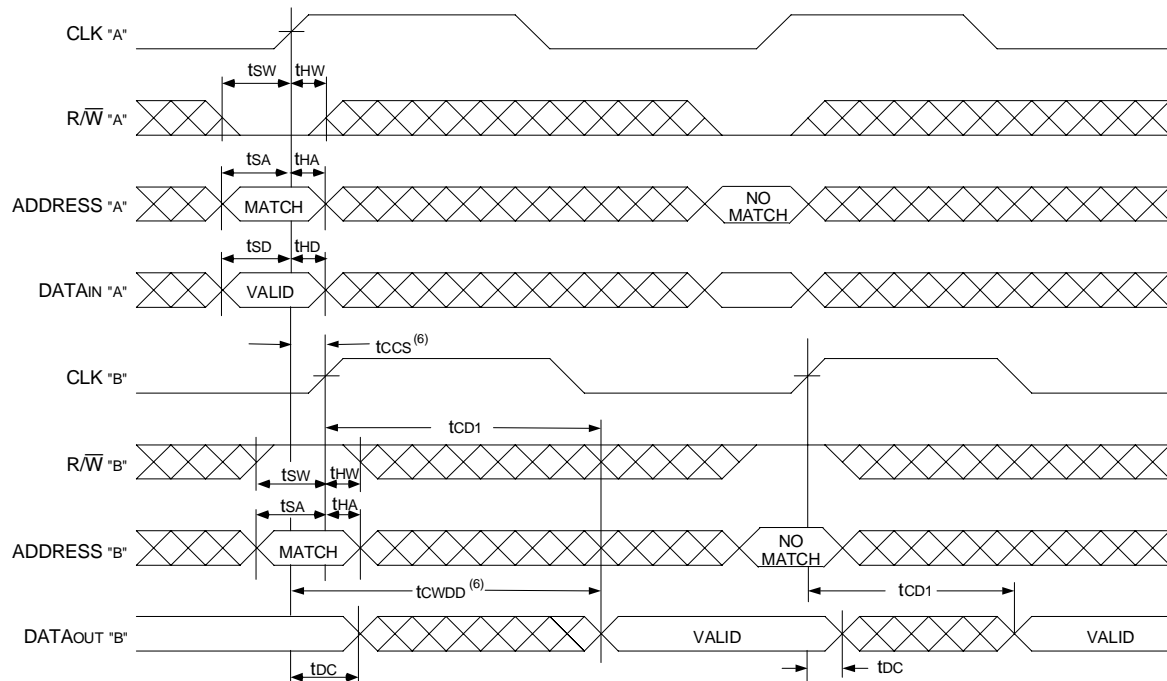
NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. \overline{OE} is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{ADS} = V_{IL}$, \overline{CNTEN} and $\overline{CNTRST} = V_{IH}$.
4. The output is disabled (High-Impedance state) by $\overline{CE0} = V_{IH}$, $CE1 = V_{IL}$, $\overline{UB} = V_{IH}$, or $\overline{LB} = V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. If \overline{UB} or \overline{LB} was HIGH, then the Upper Byte and/or Lower Byte of DATAout for $Qn + 2$ would be disabled (High-Impedance state).
7. "X" here denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Bank Select Pipelined Read^(1,2)



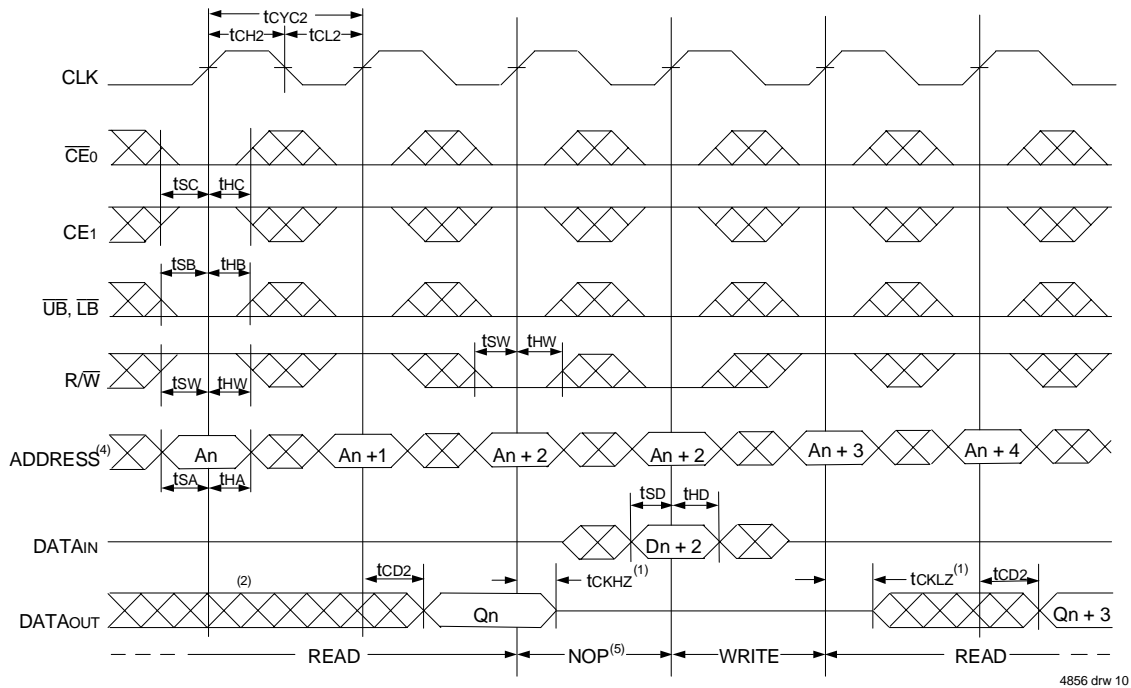
Timing Waveform with Port-to-Port Flow-Through Read^(4,5,7)



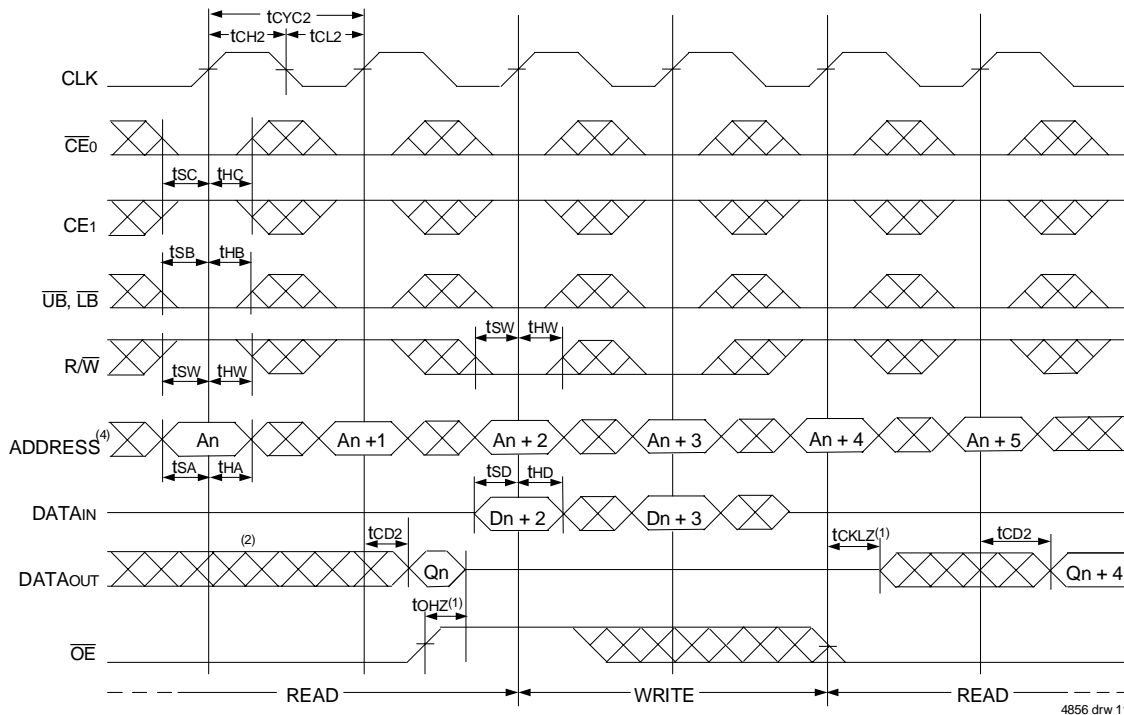
NOTES:

1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT70V9389 or IDT70V9289 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. \overline{UB} , \overline{LB} , \overline{OE} , and $\overline{ADS} = V_{IL}$; $CE_1(B1)$, $CE_1(B2)$, R/\overline{W} , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. $\overline{CE_0}$, \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; CE_1 , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$.
5. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
6. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWD} . If $t_{CCS} >$ maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD1}$. t_{CWD} does not apply in this case.
7. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite from Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽³⁾



Timing Waveform of Pipelined Read-to-Write-to-Read (\overline{OE} Controlled)⁽³⁾



NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. \overline{CE}_0 , \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; \overline{CE}_1 , \overline{CNTEN} , and $\overline{CNTST} = V_{IH}$. "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

The diagram illustrates the timing relationships for the 4856 device across several signals:

- CLK**: Clock signal with period t_{CYC1} , high pulse width t_{CH1} , and low pulse width t_{CL1} .
- \overline{CE}_0** : Chip enable signal with setup time t_{SC} and hold time t_{HC} relative to the clock.
- \overline{CE}_1** : Another chip enable signal with setup time t_{SB} and hold time t_{HB} relative to the clock.
- $\overline{UB}, \overline{LB}$** : Address bus enable signals with setup time t_{SW} and hold time t_{HW} relative to the clock.
- R/W**: Read/Write control signal with setup time t_{SW} and hold time t_{HW} relative to the clock.
- ADDRESS⁽⁴⁾**: Address bus signal showing a sequence of addresses: A_n , A_{n+1} , A_{n+2} , A_{n+2} , A_{n+3} , A_{n+4} . Setup time t_{SA} and hold time t_{HA} are indicated for A_n .
- DATAin**: Data input signal showing data D_{n+2} being written during a write cycle. Setup time t_{SD} and hold time t_{HD} are indicated.
- DATAout**: Data output signal showing a sequence of data: Q_n , Q_{n+1} , Q_{n+3} . The diagram shows a read cycle followed by a NOP cycle and then another read cycle. Timing parameters include t_{CD1} (data delay), t_{PC} (output delay), $t_{CKHZ}^{(1)}$ (clock period), and $t_{CKLZ}^{(1)}$ (clock low time).

At the bottom, the sequence of operations is indicated: READ, NOP⁽⁵⁾, WRITE, and READ.

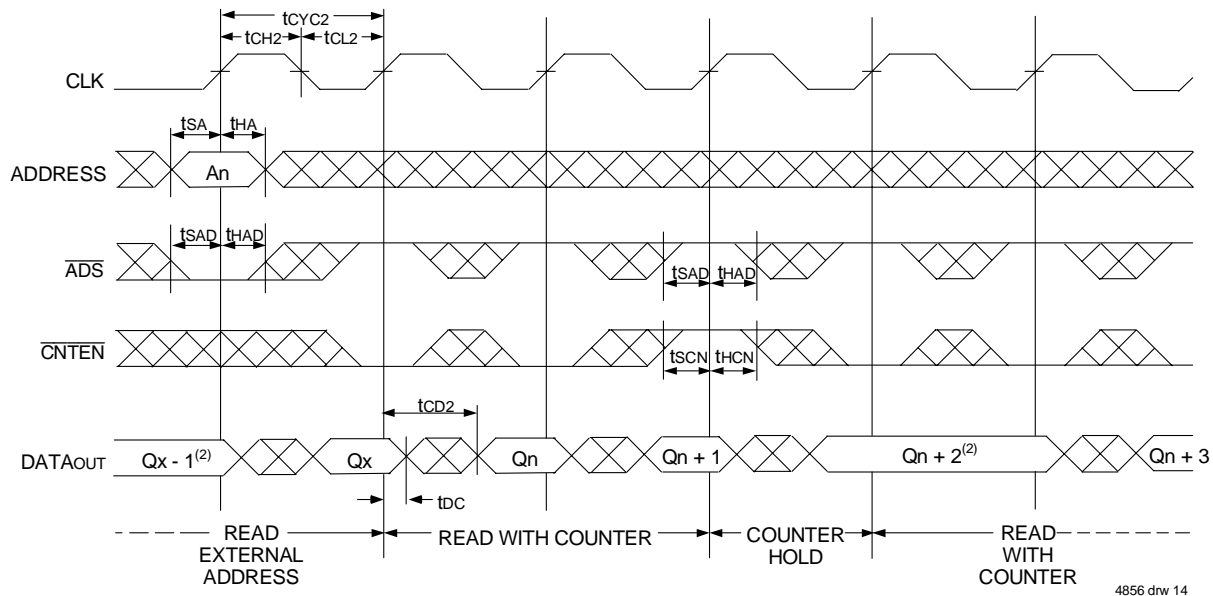
The timing diagram illustrates the operational timing for the 4856 device across three cycles: READ, WRITE, and READ. The signals and their timing parameters are as follows:

- CLK**: Clock signal. Timing parameters: t_{CYC1} (clock cycle), t_{CH1} (clock high), t_{CL1} (clock low).
- \overline{CE}_0** : Chip Enable 0. Timing parameters: t_{SC} (setup), t_{HC} (hold).
- \overline{CE}_1** : Chip Enable 1. Timing parameters: t_{SB} (setup), t_{HB} (hold).
- $\overline{UB}, \overline{LB}$** : Address Decoding signals. Timing parameters: t_{SB} (setup), t_{HB} (hold).
- $\overline{R}/\overline{W}$** : Read/Write control signal. Timing parameters: t_{SW} (setup), t_{HW} (hold).
- ADDRESS⁽⁴⁾**: Address bus. Timing parameters: t_{SA} (setup), t_{HA} (hold). Addresses shown: A_n to A_{n+5} .
- DATAin**: Data input bus. Timing parameters: t_{SD} (setup), t_{HD} (hold). Data shown: D_{n+2} to D_{n+3} .
- DATAout**: Data output bus. Timing parameters: t_{CD1} (output delay), t_{Q} (output delay), $t_{OHZ}^{(1)}$ (output high impedance), $t_{OELZ}^{(1)}$ (output low impedance), t_{DC} (output delay). Data shown: Q_n to Q_{n+4} .
- \overline{OE}** : Output Enable. Timing parameters: t_{OE} (output enable delay).

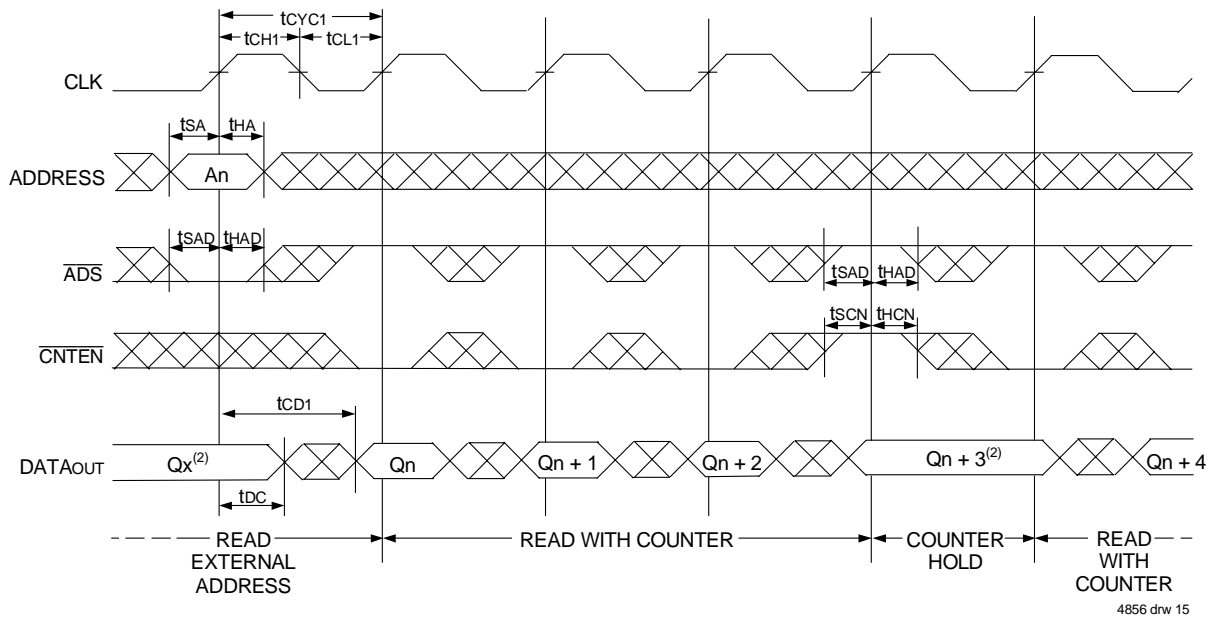
The diagram is divided into three main sections: READ, WRITE, and READ, each showing the sequence of signals and data flow.

5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



Timing Waveform of Flow-Through Read with Address Counter Advance⁽¹⁾

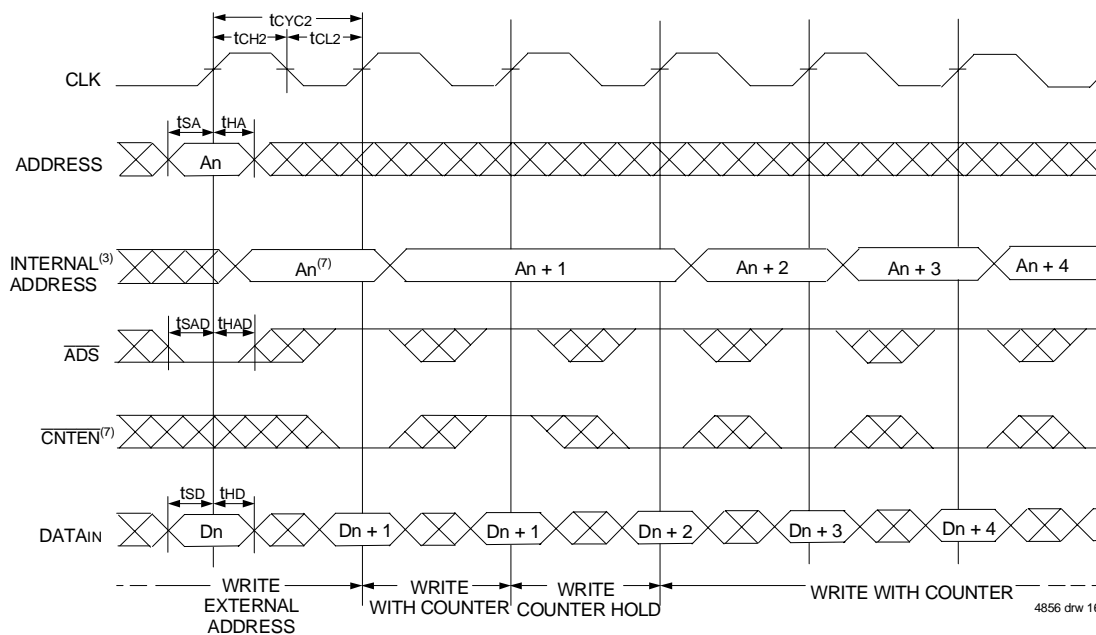


NOTES:

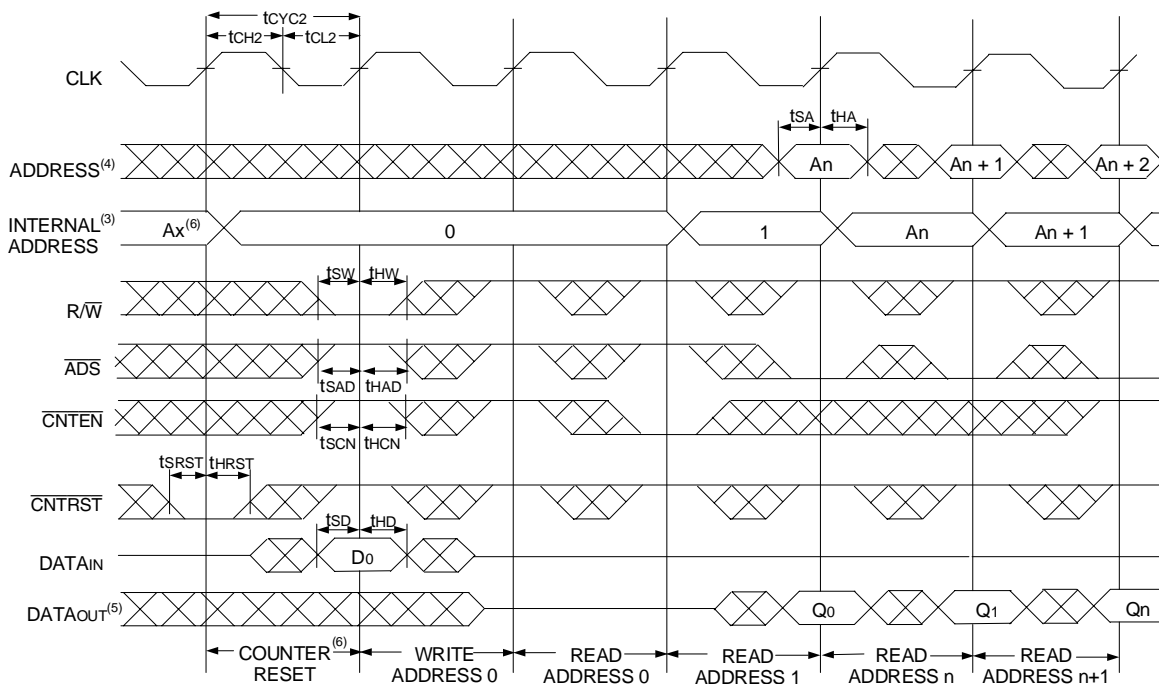
1. $\overline{CE_0}$, \overline{OE} , \overline{UB} , and $\overline{LB} = V_{IL}$; $\overline{CE_1}$, \overline{RW} , and $\overline{CNTRST} = V_{IH}$.

2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)⁽¹⁾



Timing Waveform of Counter Reset (Pipelined Outputs)⁽²⁾



NOTES:

1. \overline{CE}_0 , \overline{UB} , \overline{LB} , and R/\overline{W} = V_{IL} ; CE_1 and \overline{CNTRST} = V_{IH} .
2. \overline{CE}_0 , \overline{UB} , \overline{LB} = V_{IL} ; CE_1 = V_{IH} .
3. The "Internal Address" is equal to the "External Address" when \overline{ADS} = V_{IL} and equals the counter output when \overline{ADS} = V_{IH} .
4. Addresses do not have to be accessed sequentially since \overline{ADS} = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle. ADDR₀ will be accessed. Extra cycles are shown here simply for clarification.
7. \overline{CNTEN} = V_{IL} advances Internal Address from 'An' to 'An + 1'. The transition shown indicates the time required for the counter to advance. The 'An + 1' Address is written to during this cycle.

Functional Description

The IDT70V9389/289 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to staff the operation of the address counters for fast interleaved memory applications.

$\overline{CE_0} = V_{IH}$ or $CE_1 = V_{IL}$ for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V9389/289's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{CE_0} = V_{IL}$ and $CE_1 = V_{IH}$ to re-activate the outputs.

Depth and Width Expansion

The IDT70V9389/289 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V9389/289 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 36/32-bit or wider applications.

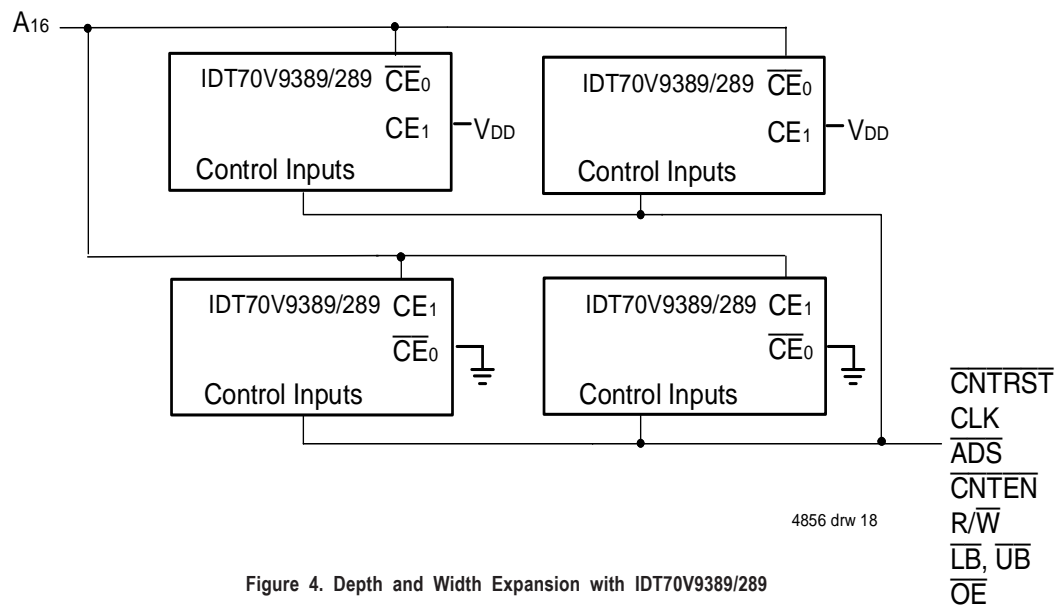


Figure 4. Depth and Width Expansion with IDT70V9389/289

Ordering Information

IDT	XXXXX	A	99	A	A		
	Device Type	Power	Speed	Package	Process/ Temperature Range		
					Blank 1 ⁽¹⁾	Commercial (0°C to +70°C) Industrial (-40°C to +85°C)	
					PRF PF	128-pin TQFP (PK128-1) 100-pin TQFP (PN100-1)	
					6 7 9 12	Commercial Only Commercial Only Commercial & Industrial Commercial Only	Speed in nanoseconds
					L	Low Power	
					70V9389 70V9289	1152K (64K x 18-Bit) Synchronous Dual-Port RAM 1024K (64K x 16-Bit) Synchronous Dual-Port RAM	

NOTE:

- Industrial temperature range is available.
For specific speeds, packages and powers contact your sales office.

4856 drw 19

IDT Clock Solution for IDT70V9389/289 Dual-Port

IDT Dual-Port Part Number	Dual-Port I/O Specifications		Dual-Port Clock Specifications				IDT PLL Clock Devices	IDT Non-PLL Clock Devices
	Voltage	I/O	Input Capacitance	Input Duty Cycle Requirement	Maximum Frequency	Jitter Tolerance		
70V9389/289	3.3	LVTTTL	9pF	40%	100	150ps	IDT2305 IDT2308 IDT2309	FCT3805 FCT3805D/E FCT3807 FCT3807D/E

4856 tbl12

Datasheet Document History

9/30/99:	Initial Public Release
11/12/99:	Replaced IDT logo
06/23/00:	Page 3 Changed information in Truth Table II
	Page 4 Increased storage temperature parameters Clarified TA parameter
	Page 5 DC Electrical parameters—changed wording from "open" to "disabled"
	Changed $\pm 200\text{mV}$ to 0mV in notes
04/09/03:	Consolidated multiple devices into one datasheet
	Changed naming conventions from V_{CC} to V_{DD} and from GND to V_{SS}
	Page 3 & 5 Added PN-100 TQFP pin configuration
	Page 1 & 18 Added PN-100 TQFP availability and ordering information
	Page 2 - 5 Added date revision to pin configurations
	Page 7 Added junction temperature to Absolute Maximum Ratings Table Added Ambient Temperature footnote
	Page 8, 10 & 18 Added 6ns speed grade
	Page 8 Added updated DC power numbers to the DC Electrical Characteristics Table
	Page 10 Added 6ns speed AC timing numbers and changed t_{OE} to be equal to t_{CD2} in the AC Electrical Characteristics Table
	Page 18 Added IDT Clock Solution Table
	Page 1 & 19 Removed "Preliminary" status


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