



## 3.3V CMOS 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS AND BUS-HOLD

**IDT74ALVCH16269**

### FEATURES:

- 0.5 MICRON CMOS Technology
- Typical  $t_{SK(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels ( $0.4\mu W$  typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SSOP, TSSOP, and TVSOP packages

### DRIVE FEATURES:

- High Output Drivers:  $\pm 24mA$  (A port)
- Suitable for heavy loads

### APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

### DESCRIPTION:

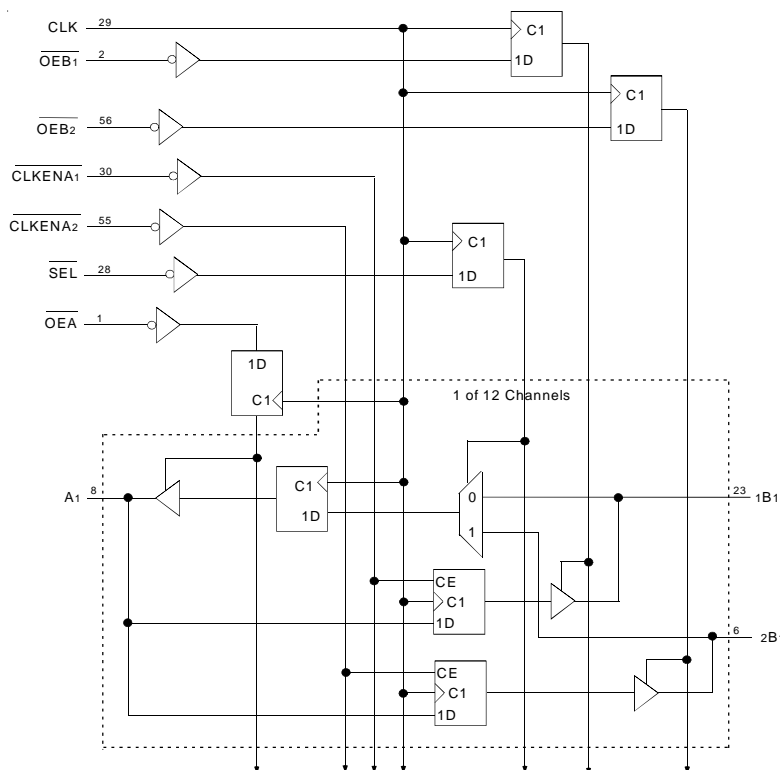
This 12-bit to 24-bit registered bus exchanger is used in applications in which two separate ports must be multiplexed onto, or demultiplexed from, a single port. It is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ( $\overline{CLKENA}$ ) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B-port. For data transfer in the B-to-A direction, a single storage register is provided. The select  $\overline{SEL}$  line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period during which the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables ( $\overline{OEA}$ ,  $\overline{OEB1}$  and  $\overline{OEB2}$ ).

The ALVCH16269 has been designed with a  $\pm 24mA$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16269 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

### FUNCTIONAL BLOCK DIAGRAM

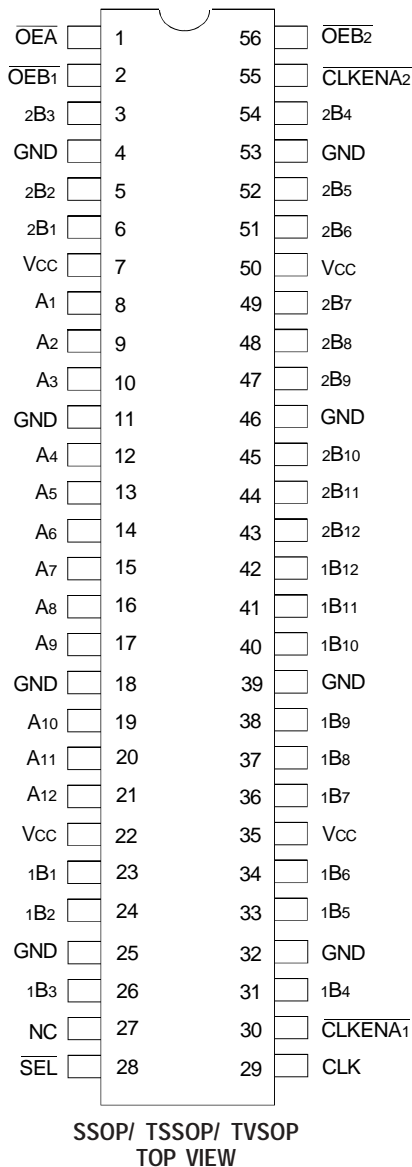


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

INDUSTRIAL TEMPERATURE RANGE

MARCH 1999

## PIN CONFIGURATION



## CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	7	pF
COUT	Output Capacitance	VOUT = 0V	7	9	pF
CI/O	I/O Port Capacitance	VIN = 0V	7	9	pF

### NOTE:

1. As applicable to the device type.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
IIK	Continuous Clamp Current, VI < 0 or VI > VCC	±50	mA
IOK	Continuous Clamp Current, VO < 0	-50	mA
ICC ISS	Continuous Current through each VCC or GND	±100	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VCC terminals.
- All terminals except VCC.

## FUNCTION TABLES<sup>(1)</sup>

### OUTPUT ENABLE

Inputs			Outputs	
CLK	$\overline{OEA}$	$\overline{OEBx}$	Ax	1Bx, 2Bx
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

### A-TO-B STORAGE ( $\overline{OEB} = L$ )

Inputs			Outputs		
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	Ax	1Bx	2Bx
H	H	X	X	1B <sub>0</sub> <sup>(2)</sup>	2B <sub>0</sub> <sup>(2)</sup>
L	X	↑	L	L	X
L	X	↑	H	H	X
X	L	↑	L	X	L
X	L	↑	H	X	H

### B-TO-A STORAGE ( $\overline{OEA} = L$ )

Inputs				Outputs
CLK	$\overline{SEL}$	1Bx	2Bx	Ax
X	H	X	X	A <sub>0</sub> <sup>(2)</sup>
X	L	X	X	A <sub>0</sub> <sup>(2)</sup>
↑	H	L	X	L
↑	H	H	X	H
↑	L	X	L	L
↑	L	X	H	H

### NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High Impedance  
↑ = LOW-to-HIGH transition
- Output level before the indicated steady-state input conditions were established.

## PIN DESCRIPTION

Pin Names	I/O	Description
Ax(1:12)	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus. <sup>(1)</sup>
1Bx(1:12)	I/O	Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory. <sup>(1)</sup>
2Bx(1:12)	I/O	Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory. <sup>(1)</sup>
CLK	I	Clock Input
CLKENA1	I	Clock Enable Input for the A-1B Register. If $\overline{\text{CLKENA1}}$ is LOW during the rising edge of CLK, data will be clocked into register A-1B (Active LOW).
CLKENA2	I	Clock Enable Input for the A-2B Register. If $\overline{\text{CLKENA2}}$ is LOW during the rising edge of CLK, data will be clocked into register A-2B (Active LOW).
SEL	I	1B or 2B Port Selection. When HIGH during the rising edge of CLK, $\overline{\text{SEL}}$ enables data transfer from 1B Port to A Port. When LOW during the rising edge of CLK, $\overline{\text{SEL}}$ enables data transfer from 2B Port to A Port.
$\overline{\text{OE}}\text{A}$	I	Synchronous Output Enable for A Port (Active LOW)
$\overline{\text{OE}}\text{B1}$	I	Synchronous Output Enable for 1B Port (Active LOW)
$\overline{\text{OE}}\text{B2}$	I	Synchronous Output Enable for 2B Port (Active LOW)

**NOTE:**

1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		1.7	—	—	V
		V <sub>CC</sub> = 2.7V to 3.6V		2	—	—	
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		—	—	0.7	V
		V <sub>CC</sub> = 2.7V to 3.6V		—	—	0.8	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = V <sub>CC</sub>	—	—	±5	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = GND	—	—	±5	μA
I <sub>OZH</sub> I <sub>OZL</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = 3.6V	V <sub>O</sub> = V <sub>CC</sub>	—	—	±10	μA
			V <sub>O</sub> = GND	—	—	±10	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = -18mA		—	-0.7	-1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	—	mV
I <sub>CC1</sub> I <sub>CC2</sub> I <sub>CC3</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V V <sub>IN</sub> = GND or V <sub>CC</sub>		—	0.1	40	μA
ΔI <sub>CC</sub>	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND		—	—	750	μA

**NOTE:**

1. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 3V	V <sub>I</sub> = 2V	-75	—	—	μA
			V <sub>I</sub> = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 2.3V	V <sub>I</sub> = 1.7V	-45	—	—	μA
			V <sub>I</sub> = 0.7V	45	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 3.6V	—	—	±500	μA

### NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> - 0.2	—	V
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -6mA	2	—	
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -12mA	1.7	—	
		V <sub>CC</sub> = 2.7V		2.2	—	
		V <sub>CC</sub> = 3V		2.4	—	
		V <sub>CC</sub> = 3V	I <sub>OH</sub> = -24mA	2	—	
VOL	Output LOW Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
		V <sub>CC</sub> = 2.3V	I <sub>OL</sub> = 6mA	—	0.4	
			I <sub>OL</sub> = 12mA	—	0.7	
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 12mA	—	0.4	
		V <sub>CC</sub> = 3V	I <sub>OL</sub> = 24mA	—	0.55	

### NOTE:

1. V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range.  
T<sub>A</sub> = -40°C to +85°C.

## OPERATING CHARACTERISTICS, T<sub>A</sub> = 25°C

Symbol	Parameter	Test Conditions	V <sub>CC</sub> = 2.5V ± 0.2V	V <sub>CC</sub> = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	C <sub>L</sub> = 0pF, f = 10Mhz	87	120	pF
CPD	Power Dissipation Capacitance Outputs disabled		80.5	118	

## SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f <sub>MAX</sub>		135	—	135	—	135	—	MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLK to Bx	1	8.2	—	7.3	1	6.2	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLK to Ax	1	6.4	—	5.8	1	5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time Synchronous $\overline{OE}$ : CLK to xBx	1	7.9	—	6.7	1	6.1	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time Synchronous $\overline{OE}$ : CLK to Ax	1	7.6	—	6.2	1	5.9	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time Synchronous $\overline{OE}$ : CLK to xBx	1	8.1	—	6.9	1	6.1	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time Synchronous $\overline{OE}$ : CLK to Ax	1	7.5	—	6.8	1	5.6	ns
t <sub>SU</sub>	Set-up Time, Ax data before CLK↑	2	—	2	—	1.7	—	ns
t <sub>SU</sub>	Set-up Time, Bx data before CLK↑	2.2	—	2.1	—	1.8	—	ns
t <sub>SU</sub>	Set-up Time, $\overline{SEL}$ before CLK↑	1.6	—	1.6	—	1.3	—	ns
t <sub>SU</sub>	Set-up Time, $\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK↑	1	—	1.2	—	0.9	—	ns
t <sub>SU</sub>	Set-up Time, $\overline{OE}$ before CLK↑	1.5	—	1.6	—	1.3	—	ns
t <sub>H</sub>	Hold Time, Ax data after CLK↑	0.7	—	0.6	—	0.6	—	ns
t <sub>H</sub>	Hold Time, Bx data after CLK↑	0.7	—	0.6	—	0.6	—	ns
t <sub>H</sub>	Hold Time, $\overline{SEL}$ after CLK↑	1.1	—	0.7	—	0.7	—	ns
t <sub>H</sub>	Hold Time, $\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK↑	1	—	0.8	—	1.1	—	ns
t <sub>H</sub>	Hold Time, $\overline{OE}$ after CLK↑	0.8	—	0.8	—	0.8	—	ns
t <sub>w</sub>	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t <sub>SK(0)</sub>	Output Skew <sup>(2)</sup>	—	—	—	—	—	500	ps

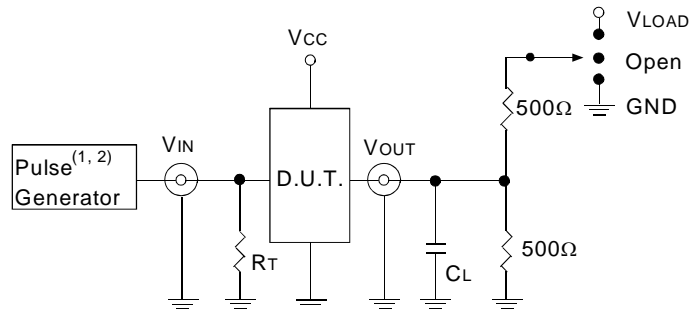
### NOTES:

- See TEST CIRCUITS AND WAVEFORMS. T<sub>A</sub> = – 40°C to + 85°C.
- Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
$V_{LOAD}$	6	6	$2 \times V_{CC}$	V
$V_{IH}$	2.7	2.7	$V_{CC}$	V
$V_T$	1.5	1.5	$V_{CC} / 2$	V
$V_{LZ}$	300	300	150	mV
$V_{HZ}$	300	300	150	mV
$C_L$	50	50	30	pF



Test Circuit for All Outputs

#### DEFINITIONS:

$C_L$  = Load capacitance: includes jig and probe capacitance.

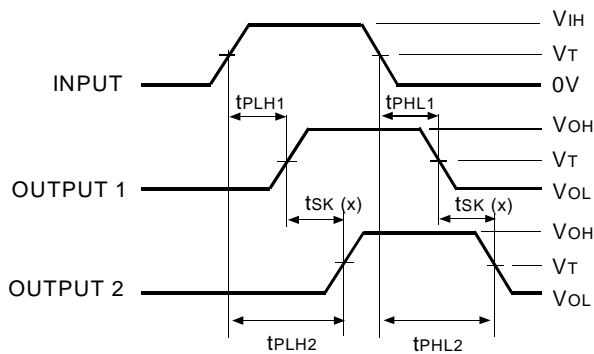
$R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2\text{ns}$ ;  $t_f \leq 2\text{ns}$ .

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	$V_{LOAD}$
Disable High Enable High	GND
All Other Tests	Open

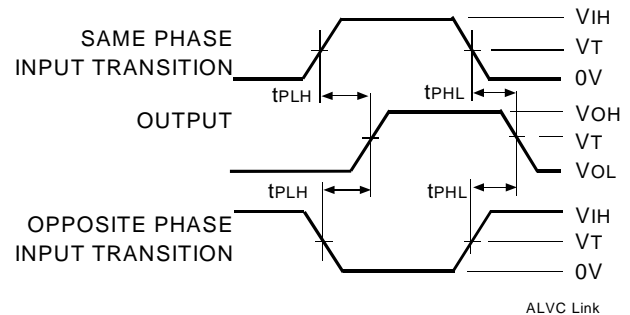


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

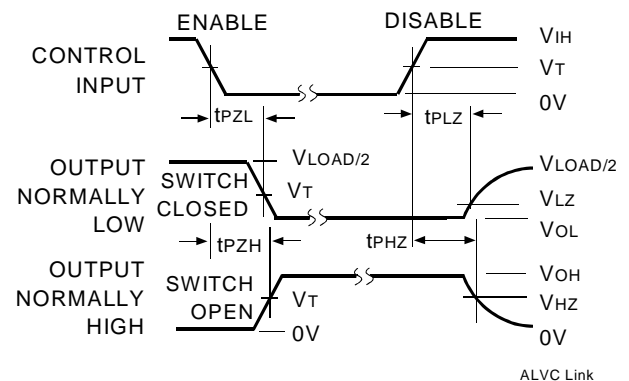
Output Skew -  $tsk(x)$

#### NOTES:

1. For  $tsk(o)$  OUTPUT1 and OUTPUT2 are any two outputs.
2. For  $tsk(b)$  OUTPUT1 and OUTPUT2 are in the same bank.



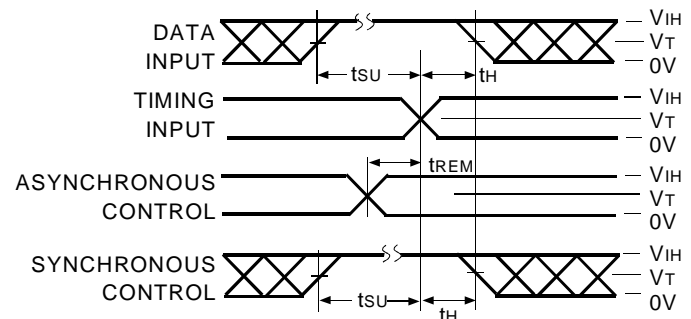
Propagation Delay



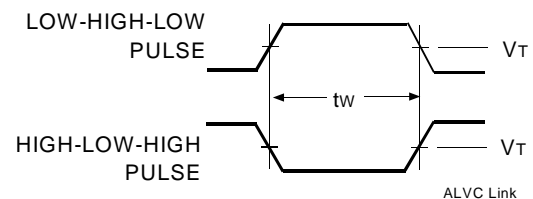
Enable and Disable Times

#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

## ORDERING INFORMATION

IDT	XX	ALVC	X	XX	XXX	XX	
Temp. Range	Bus-Hold	Family	Device Type	Package			
				PV			Shrink Small Outline Package
				PA			Thin Shrink Small Outline Package
				PF			Thin Very Small Outline Package
				269			12-Bit to 24-Bit Registered Bus Exchanger with 3-State Outputs
				16			Double-Density, $\pm 24\text{mA}$
				H			Bus-Hold
				74			$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$



**CORPORATE HEADQUARTERS**  
2975 Stender Way  
Santa Clara, CA 95054

**for SALES:**  
800-345-7015 or 408-727-6116  
fax: 408-492-8674  
www.idt.com

**for Tech Support:**  
logichelp@idt.com  
(408) 654-6459