



3.3V CMOS 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16409

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(O)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels ($0.4\mu W$ typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SSOP, TSSOP, and TVSOP packages

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$
- Suitable for heavy loads

APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

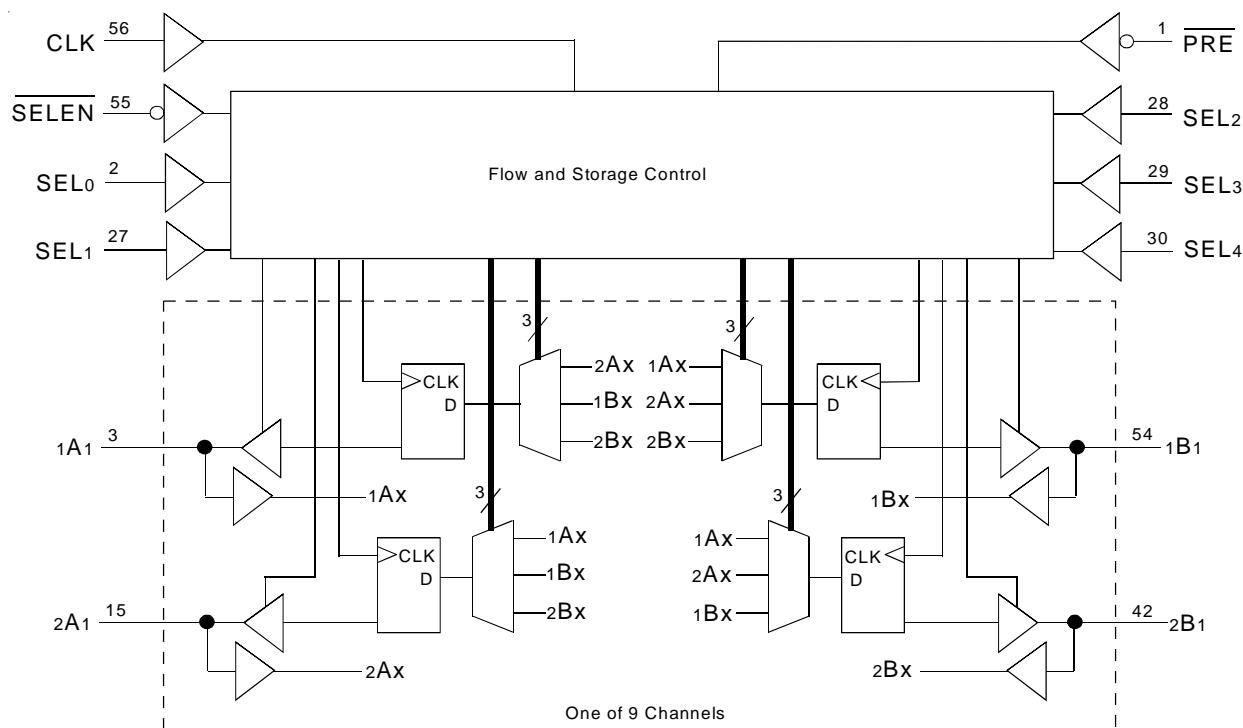
DESCRIPTION:

This 9-bit, 4-port universal bus exchanger is built using advanced dual metal CMOS technology. The ALVCH16409 allows synchronous data exchange between four different buses. Data flow is controlled by the select (SEL0–SEL4) inputs. A data-flow state is stored on the rising edge of the clock (CLK) input if the select-enable (\overline{SELEN}) input is low. Once a data-flow state has been established, data is stored in the flip-flop on the rising edge of CLK if \overline{SELEN} is high. The data-flow control logic is designed to allow glitch-free data transmission. When preset (\overline{PRE}) transitions high, the outputs are disabled immediately without waiting for a clock pulse. To leave the high-impedance state, both \overline{PRE} and \overline{SELEN} must be low and a clock pulse must be applied.

The ALVCH16409 has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16409 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

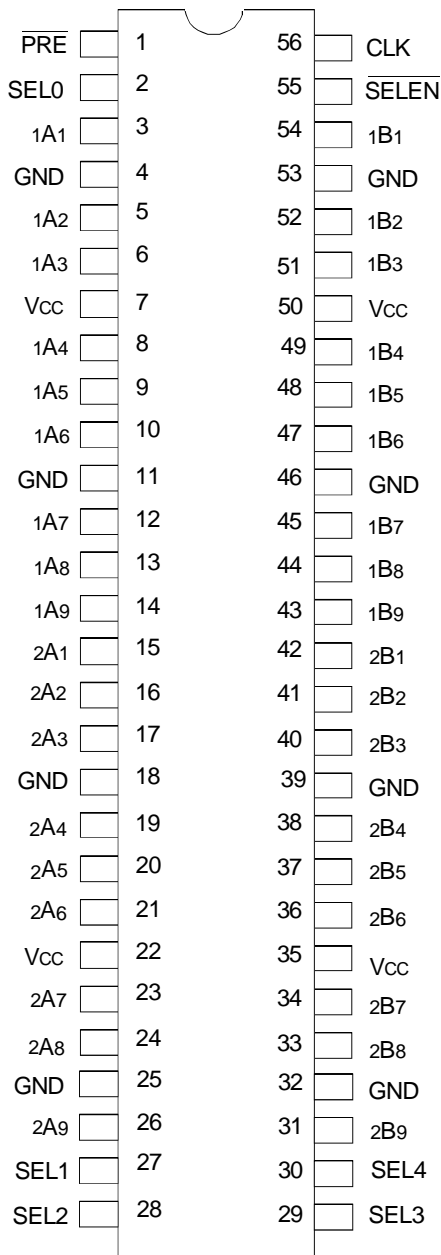


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INDUSTRIAL TEMPERATURE RANGE

OCTOBER 1999

PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
TSTG	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-50 to +50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _I > V _{CC}	±50	mA
I _{OK}	Continuous Clamp Current, V _O < 0	-50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
PRE	Preset Input (Active LOW)
SELEN	Select Enable Input (Active LOW)
SEL0 - SEL4	Select Inputs
CLK	Clock Input
x A x	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
x B x	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE⁽¹⁾

Inputs		Output
CLK	Send Port	Receive Port
↑	L	L
↑	H	H
H	X	B ⁽²⁾
L	X	B ⁽²⁾

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
- Output level before the indicated steady-state input conditions were established.

DATA FLOW CONTROL

Inputs								Data Flow
$\overline{\text{PRE}}$	$\overline{\text{SELEN}}$	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	
H	X	X	X	X	X	X	X	All outputs disabled
L	H	↑	X	X	X	X	X	No change
L	L	↑	0	0	0	0	0	None, all I/Os off
L	L	↑	0	0	0	0	1	Not used
L	L	↑	0	0	0	1	0	Not used
L	L	↑	0	0	0	1	1	Not used
L	L	↑	0	0	1	0	0	Not used
L	L	↑	0	0	1	0	1	Not used
L	L	↑	0	0	1	1	0	Not used
L	L	↑	0	0	1	1	1	Not used
L	L	↑	0	1	0	0	0	2A to 1A and 1B to 2B
L	L	↑	0	1	0	0	1	2A to 1A
L	L	↑	0	1	0	1	0	2B to 1B
L	L	↑	0	1	0	1	1	2A to 1A and 2B to 1B
L	L	↑	0	1	1	0	0	1A to 2A and 1B to 2B
L	L	↑	0	1	1	0	1	1A to 2A
L	L	↑	0	1	1	1	0	1B to 2B
L	L	↑	0	1	1	1	1	1A to 2A and 2B to 1B
L	L	↑	1	0	0	0	0	1A to 1B and 2B to 2A
L	L	↑	1	0	0	0	1	1A to 1B
L	L	↑	1	0	0	1	0	2A to 2B
L	L	↑	1	0	0	1	1	1A to 1B and 2A to 2B
L	L	↑	1	0	1	0	0	1B to 1A and 2A to 2B
L	L	↑	1	0	1	0	1	1B to 1A
L	L	↑	1	0	1	1	0	2B to 2A
L	L	↑	1	0	1	1	1	1B to 1A and 2B to 2A
L	L	↑	1	1	0	0	0	2B to 1A and 2A to 1B
L	L	↑	1	1	0	0	1	1B to 2A
L	L	↑	1	1	0	1	0	2B to 1A
L	L	↑	1	1	0	1	1	2B to 1A and 1B to 2A
L	L	↑	1	1	1	0	0	1A to 2B and 1B to 2A
L	L	↑	1	1	1	0	1	1A to 2B
L	L	↑	1	1	1	1	0	2A to 1B
L	L	↑	1	1	1	1	1	1A to 2B and 2A to 1B

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	$V_{CC} = 3.6\text{V}$	$V_I = V_{CC}$	—	—	± 5	μA
I_{IL}	Input LOW Current	$V_{CC} = 3.6\text{V}$	$V_I = \text{GND}$	—	—	± 5	μA
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = V_{CC}$	—	—	± 10	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 10	
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$ $V_{IN} = \text{GND}$ or V_{CC}		—	0.1	40	μA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	750	μA

NOTE:

1. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 3\text{V}$	$V_I = 2\text{V}$	-75	—	—	μA
			$V_I = 0.8\text{V}$	75	—	—	
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	-45	—	—	μA
			$V_I = 0.7\text{V}$	45	—	—	
I_{BHHO} I_{BHL0}	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 3.6V	—	—	± 500	μA

NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 6mA	2	—	
		VCC = 2.3V	IOH = - 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3V		2.4	—	
		VCC = 3V	IOH = - 24mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IoL = 0.1mA	—	0.2	V
		VCC = 2.3V	IoL = 6mA	—	0.4	
			IoL = 12mA	—	0.7	
		VCC = 2.7V	IoL = 12mA	—	0.4	
		VCC = 3V	IoL = 24mA	—	0.55	

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range.
TA = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	—	60	pF
CPD	Power Dissipation Capacitance Outputs disabled		—	60	

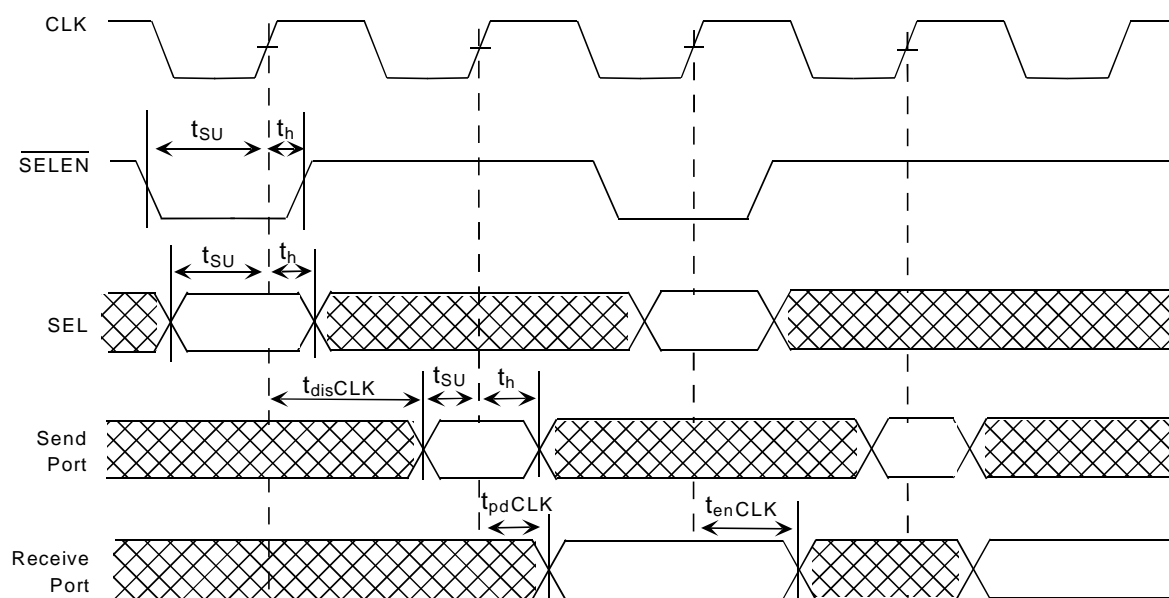
SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		120	—	120	—	120	—	MHz
t _{PLH} t _{PHL}	Propagation Delay CLK to xAx or xBx	1.5	6	—	5.7	1.5	5.1	ns
t _{PZH} t _{PZL}	Output Enable Time CLK to xAx or xBx	2.4	6.9	—	6.3	2	5.7	ns
t _{PHZ} t _{PLZ}	Output Disable Time CLK to xAx or xBx	2.3	7.1	—	6	2	5.7	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{\text{PRE}}$ to xAx or xBx	2.8	7.5	—	6.5	2.5	6.1	ns
t _{SU}	Set-up Time, HIGH or LOW, xAx or xBx before CLK↑	1.9	—	1.9	—	1.4	—	ns
t _{SU}	Set-up Time, HIGH or LOW, SEL before CLK↑	5.1	—	4.2	—	3.5	—	ns
t _{SU}	Set-up Time, HIGH or LOW, $\overline{\text{SELEN}}$ before CLK↑	2.5	—	2.5	—	1.8	—	ns
t _{SU}	Set-up Time, HIGH or LOW, $\overline{\text{PRE}}$ before CLK↑	1	—	1	—	0.7	—	ns
t _H	Hold Time, HIGH or LOW, xAx or xBx after CLK↑	0.8	—	0.8	—	1	—	ns
t _H	Hold Time, HIGH or LOW, SEL after CLK↑	0	—	0	—	0	—	ns
t _H	Hold Time, HIGH or LOW, $\overline{\text{SELEN}}$ after CLK↑	0.5	—	0.5	—	0.8	—	ns
t _W	Pulse Duration, CLK HIGH or LOW	4.2	—	4.2	—	3	—	ns
t _{sk(0)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

- See TEST CIRCUITS AND WAVEFORMS. T_A = - 40°C to + 85°C.
- Skew between any two outputs of the same package and switching in the same direction.

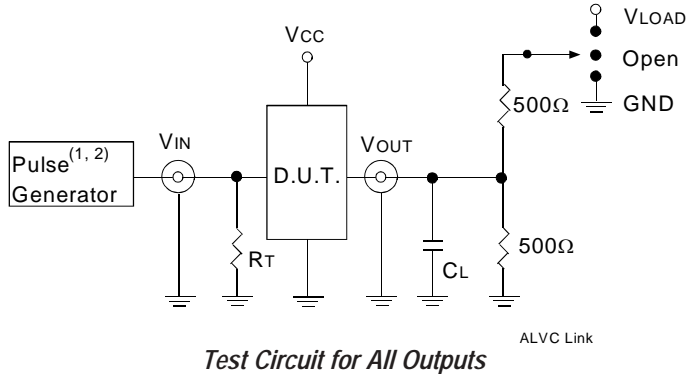
TIMING DIAGRAM



TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ =3.3V±0.3V	V _{CC} ⁽¹⁾ =2.7V	V _{CC} ⁽²⁾ =2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

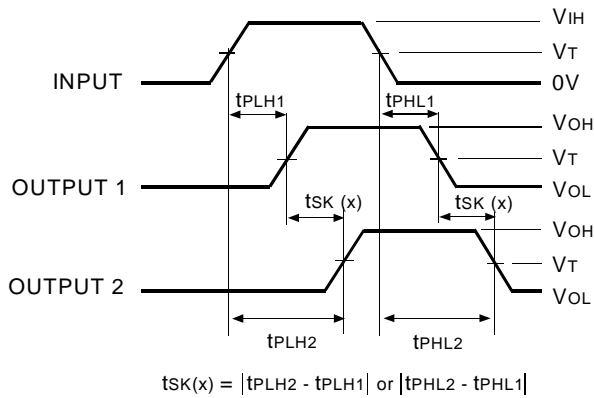
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open

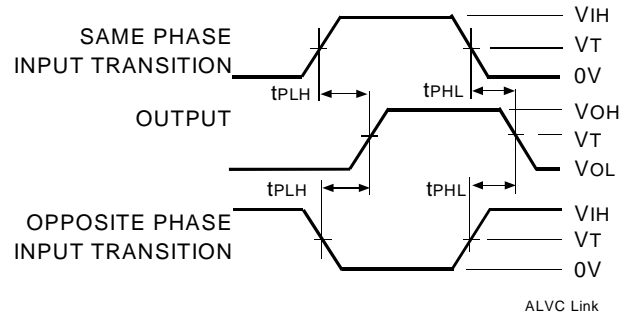


$$tsK(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

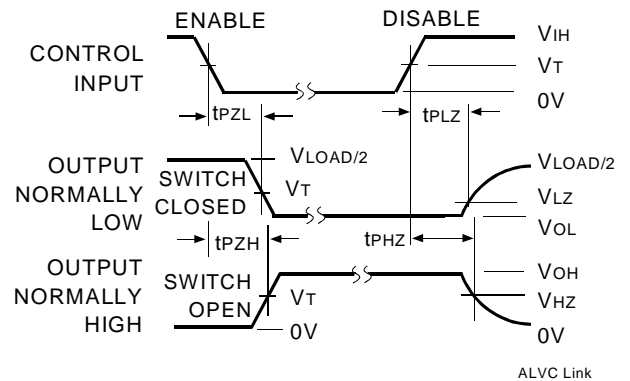
Output Skew - tsK(x)

NOTES:

1. For tsK(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsK(b) OUTPUT1 and OUTPUT2 are in the same bank.



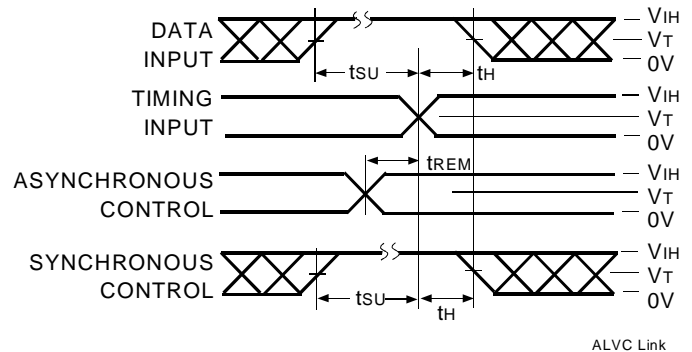
Propagation Delay



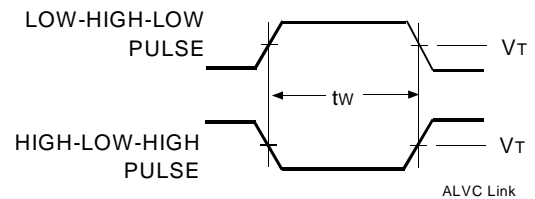
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION

IDT	XX	ALVC	X	XX	XXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package
						PA	Thin Shrink Small Outline Package
						PF	Thin Very Small Outline Package
						409	9-Bit, 4-Port Universal Bus Exchanger with 3-State Outputs
						R16	Double-Density, $\pm 12\text{mA}$
						H	Bus-Hold
						74	-40°C to $+85^{\circ}\text{C}$



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