



Integrated Device Technology, Inc.

## 4K x 36 BiCMOS DUAL-PORT STATIC RAM MODULE

IDT7M1014

### FEATURES

- High-density 4K x 36 BiCMOS Dual-Port Static RAM module
- Fast access times
  - Commercial: 15, 20ns
  - Military: 25, 30ns
- Fully asynchronous read/write operation from either port
- Surface mounted LCC packages allow through-hole module to fit on a ceramic PGA footprint
- Single 5V ( $\pm 10\%$ ) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

### DESCRIPTION

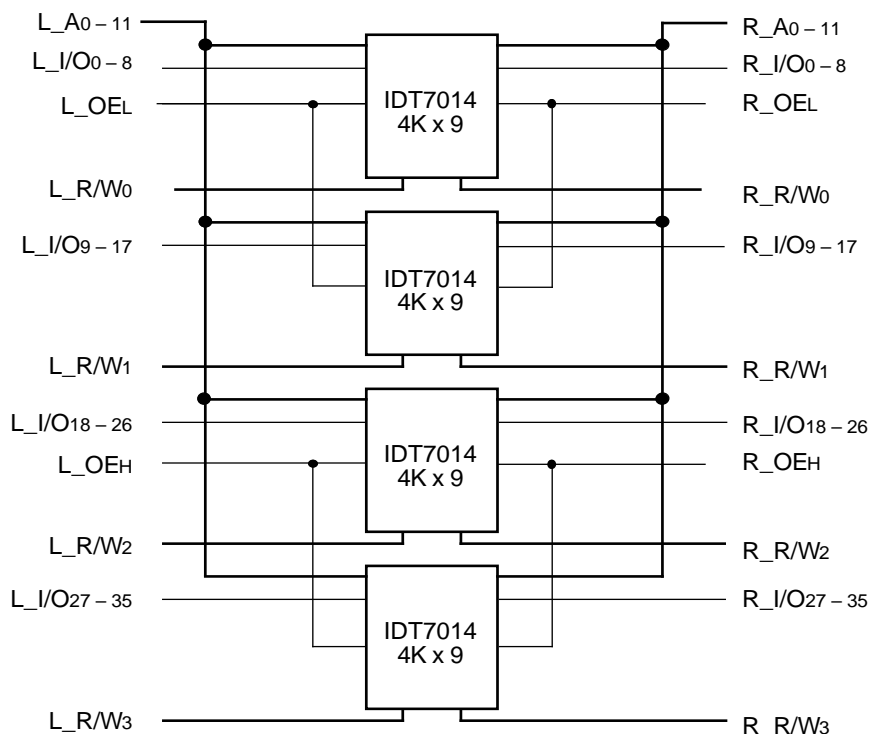
The IDT7M1014 is a 4K x 36 asynchronous high-speed BiCMOS Dual-Port static RAM module constructed on a co-fired ceramic substrate using 4 IDT7014 (4K x 9) asynchronous Dual-Port RAMs. The IDT7M1014 module is designed to be used as stand-alone 36-bit dual-port RAM.

This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory.

The IDT7M1014 module is packaged in a 142-lead ceramic PGA (Pin Grid Array). Maximum access times as fast as 15ns and 25ns are available over the commercial and military temperature ranges respectively.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

### FUNCTIONAL BLOCK DIAGRAM



2819 drw 01

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**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

**DECEMBER 1995**

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DSC-2819/4

## PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	GND	L_I/O3	L_I/O2	GND	L_I/O1	L_I/O0	GND	R_I/O0	R_I/O1	GND	R_I/O2	R_I/O3	GND	
B	L_I/O4	L_I/O5	L_I/O6	L_A2	L_A1	L_A0	N.C.	R_A0	R_A1	R_A2	R_I/O6	R_I/O5	R_I/O4	
C	L_I/O8	Vcc	L_I/O7	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND	R_I/O7	Vcc	R_I/O8	
D	L_I/O9	L_I/O10	L_I/O11	L_A3	GND				GND	R_A3	R_A4	R_I/O11	R_I/O10	R_I/O9
E	L_I/O12	N.C.	N.C.	L_A4						R_A5	N.C.	N.C.	R_I/O12	
F	L_I/O13	L_OE L	L_OE H	L_A5						R_A6	R_OE H	R_OE L	R_I/O13	
G	GND	L_R/W0	L_R/W1	GND						GND	R_R/W1	R_R/W0	GND	
H	L_I/O14	L_R/W2	L_R/W3	L_A6						R_A7	R_R/W3	R_R/W2	R_I/O14	
J	L_I/O15	L_I/O16	L_I/O17	L_A7						R_A8	R_I/O17	R_I/O16	R_I/O15	
K	L_I/O20	L_I/O19	L_I/O18	GND						L_A10	L_A11	GND	R_A11	R_A10
L	L_I/O21	Vcc	L_I/O22	L_A8	L_A9	L_I/O31	R_I/O35	R_I/O34	R_I/O30	R_A9	R_I/O22	Vcc	R_I/O21	
M	L_I/O23	L_I/O24	L_I/O25	L_I/O29	L_I/O30	L_I/O32	L_I/O35	R_I/O33	R_I/O31	R_I/O29	R_I/O25	R_I/O24	R_I/O23	
N	GND	L_I/O26	L_I/O27	L_I/O28	GND	L_I/O33	L_I/O34	R_I/O32	GND	R_I/O28	R_I/O27	R_I/O26	GND	

2819 drw 02

## PIN NAMES

Left Port	Right Port	Names
L_R/W 0-3	R_R/W 0-3	Byte Read/Write Enables
L_OE L, H	R_OE L, H	Word Output Enables
L_A 0-11	R_A 0-11	Address Inputs
L_I/O 0-35	R_I/O 0-35	Data Input/Outputs
Vcc		Power
GND		Ground

2819 tbl 01

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Commercial	Military	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage	−0.5 to +7.0	−0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	−55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	−10 to +85	−65 to +135	°C
T <sub>STG</sub>	Storage Temperature	−55 to +125	−65 to +150	°C
I <sub>OUT</sub>	DC Output Current	50	50	mA

### NOTES:

2819 tbl 02

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Inputs and V<sub>CC</sub> terminals only.
- I/O terminals only.

## RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input HIGH Voltage	2.2	—	6.0	V
V <sub>IL</sub>	Input LOW Voltage	−0.5 <sup>(1)</sup>	—	0.8	V

### NOTE:

2819 tbl 03

- V<sub>IL</sub> ≥ −3.0V for pulse width less than 20ns.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V <sub>CC</sub>
Military	−55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2819 tbl 04

## CAPACITANCE TABLE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub> (1)	Input Capacitance (Address)	V <sub>IN</sub> = 0V	50	pF
C <sub>IN</sub> (2)	Input Capacitance (Data, R/ $\overline{W}$ )	V <sub>IN</sub> = 0V	15	pF
C <sub>IN</sub> (3)	Input Capacitance ( $\overline{OE}$ )	V <sub>IN</sub> = 0V	25	pF
C <sub>OUT</sub>	Output Capacitance (Data)	V <sub>OUT</sub> = 0V	15	pF

### NOTE:

2819 tbl 05

- This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = -55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
ILI	Input Leakage VIN = GND to VCC	VCC = Max.	—	40	μA
ILO	Output Leakage OE ≥ VIH, VOUT = GND to VCC	VCC = Max.	—	10	μA
VoL	Output LOW Voltage	VCC = Min. IoL = 4mA	—	0.4	V
VoH	Output HIGH Voltage	VCC = Min. IoH = -4mA	2.4	—	V

2819 tbl 06

DC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = -55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Icc	Operating Current	VCC = Max., Outputs Open, f = fMAX <sup>(1)</sup>	—	1040	mA

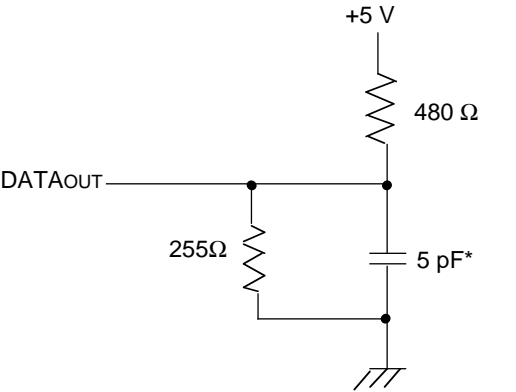
NOTE: 2819 tbl 07

1. At f=fMAX, address and data inputs (except OE) are cycling at the maximum frequency of read cycle of 1/tRC, and using “AC TEST CONDITIONS” of input levels of GND to 3V.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-3

2819 tbl 08

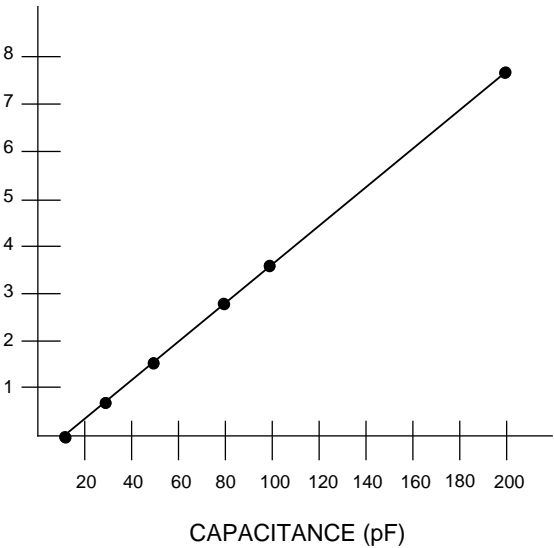


2819 drw 03

\*Including scope and jig.

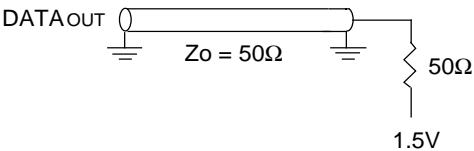
Figure 1. Output Load  
(For tCHZ, tCLZ, tOHZ, tOLZ, tWHZ, tOW)

ΔTAA  
(Typical, ns)



2819 drw 04b

Figure 3. Alternate Lumped Capacitive Load,  
Typical Derating



2819 drw 04a

Figure 2. Alternate Output Load

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = 5V \pm 10\%$ ,  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  or  $0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

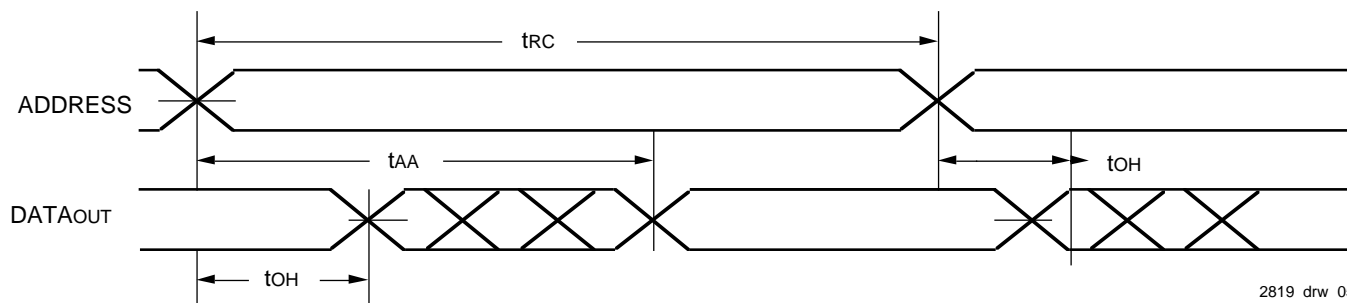
Symbol	Parameter	7M1014SxxG				7M1014SxxGB				
		-15		-20		-25		-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	15	—	20	—	25	—	30	—	ns
tAA	Address Access Time	—	15	—	20	—	25	—	30	ns
tOE	Output Enable Access Time	—	8	—	10	—	12	—	15	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tOLZ <sup>(1)</sup>	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
tOHZ <sup>(1)</sup>	Output Disable to Output in Hi-Z	—	7	—	9	—	11	—	13	ns
Write Cycle										
tWC	Write Cycle Time	15	—	20	—	25	—	30	—	ns
tAW	Address Valid to End of Write	14	—	15	—	20	—	25	—	ns
tAS	Address Set-Up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	15	—	20	—	25	—	ns
tWR	Write Recovery Time	1	—	2	—	2	—	2	—	ns
tDW	Data Valid to End of Write	10	—	12	—	15	—	20	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWHZ <sup>(1)</sup>	Write Enable to Output in Hi-Z	—	7	—	9	—	11	—	13	ns
tOW <sup>(1)</sup>	Output Active from End of Write	0	—	0	—	0	—	0	—	ns
tWDD	Write Pulse to Data Delay	—	30	—	40	—	45	—	50	ns
tDDP <sup>(1)</sup>	Write Data Valid to Read Data Delay	—	25	—	30	—	35	—	40	ns

### NOTES:

1. This parameter is guaranteed by design but not tested.
2. Port-to-Port delay through the RAM cells from the writing port to the reading port.

2819 tbl 09

## TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE) <sup>(1,2)</sup>



2819 drw 05

### NOTES:

1.  $R/\overline{W}$  is HIGH for Read Cycles.
2.  $\overline{OE} \leq V_{IL}$ .

2819 drw 06

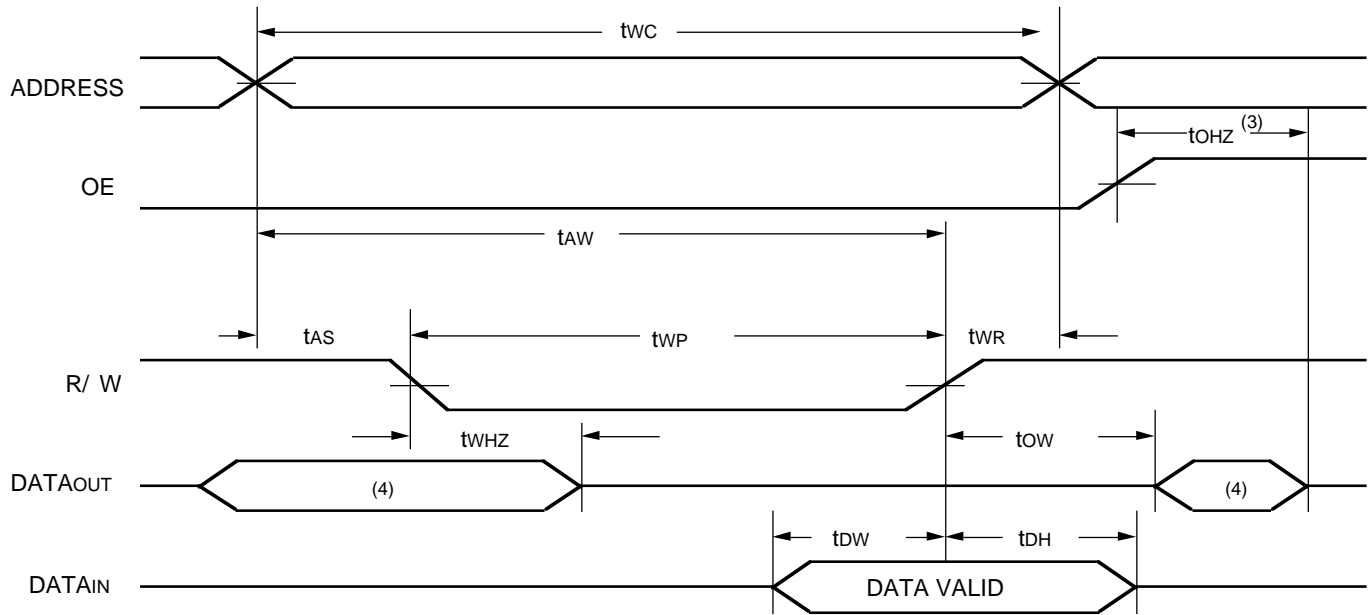
The diagram illustrates the timing for the 74VHC163 4-bit counter. It shows the relationship between the ADDRESS, DATA, and R/W signals. Key timing parameters are labeled:

- $t_{WC}$ : Write Cycle
- $t_{WP}$ : Write Pulse
- $t_{DW}$ : Data Valid
- $t_{WDD}$ : Write Data Delay
- $t_{DDD}$ : Data Delay
- $t_{WDD}$ : Read Data Delay
- $t_{DDD}$ : Data Delay

2819 drw 07

1.  $R/\overline{W}$  is HIGH for Read Cycles.
2. Address valid prior to  $\overline{OE}$  transition LOW.
3. This parameter is guaranteed by design but not tested.

## TIMING WAVEFORM OF WRITE CYCLE (EITHER SIDE) (1,2)

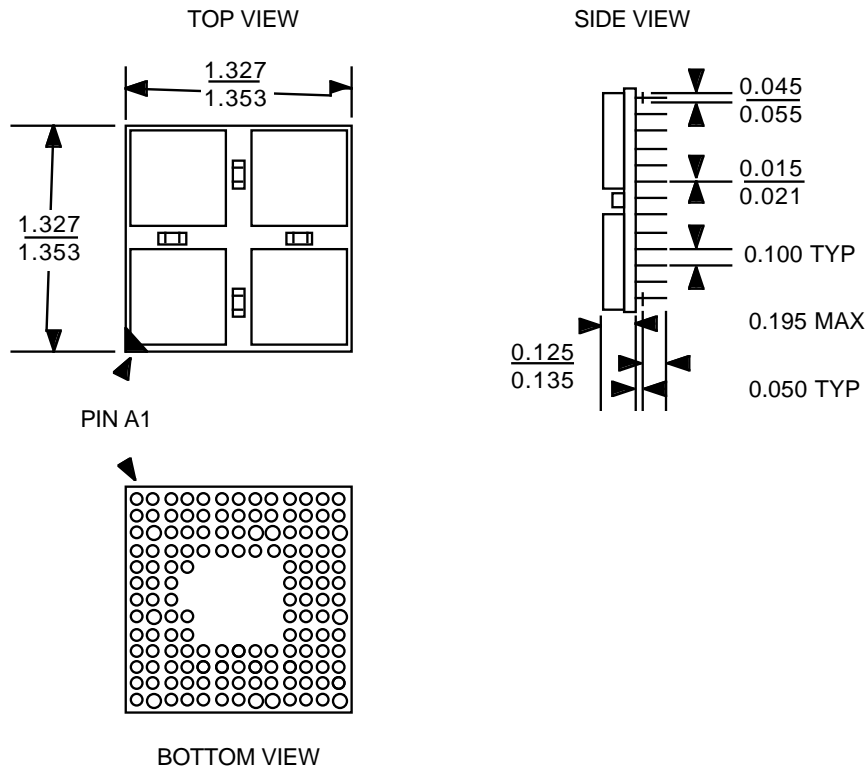


2819 drw 08

### NOTES:

1.  $\overline{R/\overline{W}}$  is HIGH during all address transitions.
2. If  $\overline{OE}$  is LOW during the write cycle, the write pulse width must be the larger of  $tWP$  or  $(tWZ + tOW)$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $tOW$ . If  $\overline{OE}$  is HIGH, this requirement does not apply, and the write pulse can be as short as the specified  $tWP$ .
3. This parameter is guaranteed by design but not tested.
4. During this period, the I/O pins are in the output state and input signals must not be applied.

PACKAGE DIMENSIONS



2819 drw 10

ORDERING INFORMATION

IDT	XXXX	A	999	A	A	
	Device Type	Power	Speed	Package	Process/ Temperature Range	
					BLANK	Commercial (0°C to +70°C)
					B	Military (–55°C to +125°C) Semiconductor Components compliant to MIL-STD883, Class B
					G	Ceramic PGA (Pin Grid Array)
					15	(Commercial Only)
					20	(Commercial Only)
					25	(Military Only)
					30	(Military Only)
					S	Standard Power
					7M1014	4K x 36 BiCMOS Dual-Port static RAM Module

2819 drw 10