



Integrated Device Technology, Inc.

## 256K x 32 CMOS STATIC RAM MODULE

**IDT7MP4045**  
**IDT7MP4145**

- High density 1 megabyte static RAM module (IDT7MP4145 upgradeable to 4 megabyte, IDT7MP4120)
- Low profile 64 pin ZIP (Zig-zag In-line vertical Package) or 64 pin SIMM (Single In-line Memory Module) for IDT7MP4045 and 72 pin SIMM (Single In-line Memory Module) for IDT7MP4145
- Very fast access time: 15ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V ( $\pm 10\%$ ) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

### PIN CONFIGURATION – 7MP4045<sup>(1)</sup>

PD <sub>0</sub>	2	1	GND	PD <sub>1</sub>	3	PD <sub>0</sub> – GND
I/O <sub>0</sub>	4	5	I/O <sub>8</sub>	PD <sub>1</sub> – GND	5	
I/O <sub>1</sub>	6	7	I/O <sub>9</sub>		7	
I/O <sub>2</sub>	8	9	I/O <sub>10</sub>		9	
I/O <sub>3</sub>	10	11	I/O <sub>11</sub>		11	
VCC	12	13	A <sub>0</sub>		13	
A <sub>7</sub>	14	15	A <sub>1</sub>		15	
A <sub>8</sub>	16	17	A <sub>2</sub>		17	
A <sub>9</sub>	18	19	I/O <sub>12</sub>		19	
I/O <sub>4</sub>	20	21	I/O <sub>13</sub>		21	
I/O <sub>5</sub>	22	23	I/O <sub>14</sub>		23	
I/O <sub>6</sub>	24	25	I/O <sub>15</sub>		25	
I/O <sub>7</sub>	26	27	GND		27	
$\overline{WE}$	28	29	A <sub>15</sub>		29	
A <sub>14</sub>	30	31	$\overline{CS}_2$		31	
$\overline{CS}_1$	32	<b>ZIP, SIMM TOP VIEW</b>				
$\overline{CS}_3$	34	33	$\overline{CS}_4$		33	
A <sub>16</sub>	36	35	A <sub>17</sub>		35	
GND	38	37	$\overline{OE}$		37	
I/O <sub>16</sub>	40	39	I/O <sub>24</sub>		39	
I/O <sub>17</sub>	42	41	I/O <sub>25</sub>		41	
I/O <sub>18</sub>	44	43	I/O <sub>26</sub>		43	
I/O <sub>19</sub>	46	45	I/O <sub>27</sub>		45	
A <sub>10</sub>	48	47	A <sub>3</sub>		47	
A <sub>11</sub>	50	49	A <sub>4</sub>		49	
A <sub>12</sub>	52	51	A <sub>5</sub>		51	
A <sub>13</sub>	54	53	VCC		53	
I/O <sub>20</sub>	56	55	A <sub>6</sub>		55	
I/O <sub>21</sub>	58	57	I/O <sub>28</sub>		57	
I/O <sub>22</sub>	60	59	I/O <sub>29</sub>		59	
I/O <sub>23</sub>	62	61	I/O <sub>30</sub>		61	
GND	64	63	I/O <sub>31</sub>		63	

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#### NOTE:

1. Pins 2 and 3 (PD<sub>0</sub> and PD<sub>1</sub>) are read by the user to determine the density of the module. If PD<sub>0</sub> reads GND and PD<sub>1</sub> reads GND, then the module has a 256K depth.

### DESCRIPTION:

The IDT7MP4045/4145 is a 256K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. The IDT7MP4045 is available with access time as fast as 10ns with minimal power consumption.

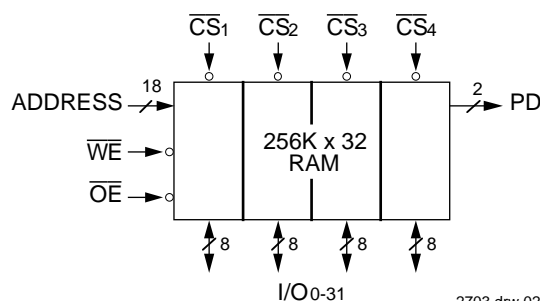
The IDT7MP4045 is packaged in a 64 pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 64 pin SIMM (Single In-line Memory Module) where as the 7MP4145 is packaged in a 72 pin SIMM (Single In-line Memory Module). The 4045 ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.365 inches wide. The 7MP4045 ZIP is only 0.585 inches high, this low profile package is ideal for systems with minimum board spacing while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4045/4145 are TTL-compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Identification pins are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD pins to determine a 256K depth.

The contact pins are plated with 100 micro-inches of nickel covered by 30 micro-inches minimum of selective gold.

### FUNCTIONAL BLOCK DIAGRAM



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### PIN NAMES

I/O <sub>0</sub> –31	Data Inputs/Outputs
A <sub>0</sub> –17	Addresses
$\overline{CS}_1$ –4	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD <sub>0</sub> –1	Depth Identification
VCC	Power
GND	Ground
NC	No Connect

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### COMMERCIAL TEMPERATURE RANGE

SEPTEMBER 1996

## CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
CIN(C)	Input Capacitance (CS)	V(IN) = 0V	20	pF
CIN(A)	Input Capacitance (Address & Control)	V(IN) = 0V	70	pF
CIO	I/O Capacitance	V(OUT) = 0V	12	pF

### NOTE:

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- This parameter is guaranteed by design but not tested.

## RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

### NOTE:

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- VIL (min) = -1.5V for pulse width less than 10ns.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

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## TRUTH TABLE

Mode	CS	OE	WE	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DATAOUT	Active
Write	L	X	L	DATAIN	Active
Read	L	H	H	High-Z	Active

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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-10 to +85	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

### NOTE:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## PIN CONFIGURATION – 7MP4145<sup>(1)</sup>

NC	2	1	NC	PD0 - GND
PD3	4	3	PD2	PD1 - GND
PD0	6	5	GND	PD2 - OPEN
I/O0	8	7	PD1	PD3 - OPEN
I/O1	10	9	I/O8	
I/O2	12	11	I/O9	
I/O3	14	13	I/O10	
VCC	16	15	I/O11	
A7	18	17	A0	
A8	20	19	A1	
A9	22	21	A2	
I/O4	24	23	I/O12	
I/O5	26	25	I/O13	
I/O6	28	27	I/O14	
I/O7	30	29	I/O15	
WE	32	31	GND	
A14	34	33	A15	
CS1	36	35	CS2	
CS3	38	37	CS4	
A16	40	39	A17	
GND	42	41	OE	
I/O16	44	43	I/O24	
I/O17	46	45	I/O25	
I/O18	48	47	I/O26	
I/O19	50	49	I/O27	
A10	52	51	A3	
A11	54	53	A4	
A12	56	55	A5	
A13	58	57	VCC	
I/O20	60	59	A6	
I/O21	62	61	I/O28	
I/O22	64	63	I/O29	
I/O23	66	65	I/O30	
GND	68	67	I/O31	
NC	70	69	NC	
NC	72	71	NC	

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SIMM  
TOP VIEW

### NOTE:

- Pins 3,4,6, and 7 (PD0-3) are read by the user to determine the density of the module. If PD0, PD1 read GND and PD2, PD3 read OPEN, then the module has a 256K depth.

DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ±10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
ILI	Input Leakage (Address and Control)	VCC = Max.; VIN = GND to VCC	—	80	μA
ILI	Input Leakage (Data)	VCC = Max.; VIN = GND to VCC	—	10	μA
ILO	Output Leakage	VCC = Max.; CS = VIH, VOUT = GND to VCC	—	10	μA
VOL	Output LOW	VCC = Min., IOL = 8mA	—	0.4	V
VOH	Output HIGH	VCC = Min., IOH = −4mA	2.4	—	V

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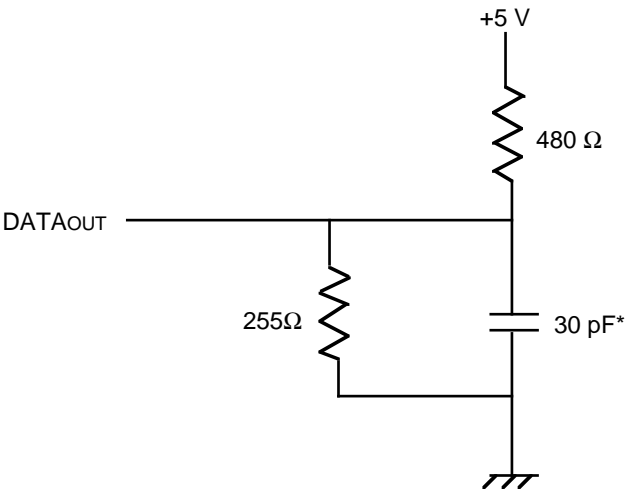
Symbol	Parameter	Test Conditions	Max.	Unit
ICC	Dynamic Operating Current	f = fMAX; CS = VIL VCC = Max.; Output Open	1360	mA
ISB	Standby Supply Current	CS ≥ VIH, VCC = Max. Outputs Open, f = fMAX	480	mA
ISB1	Full Standby Supply Current	CS ≥ VCC − 0.2V; f = 0 VIN > VCC − 0.2V or < 0.2V	120	mA

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

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\*Includes scope and jig.  
Figure 1. Output Load

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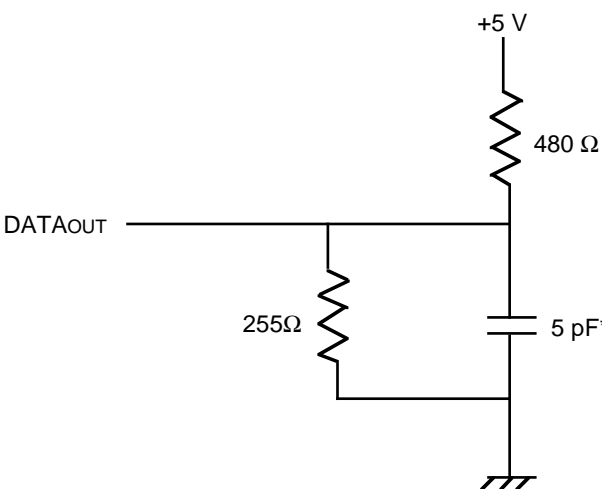


Figure 2. Output Load  
(for tOLZ,tOHZ, tCHZ, tCLZ, tWHZ, tOW)

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## AC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 5V ±10%, T<sub>A</sub> = 0°C to +70°C)

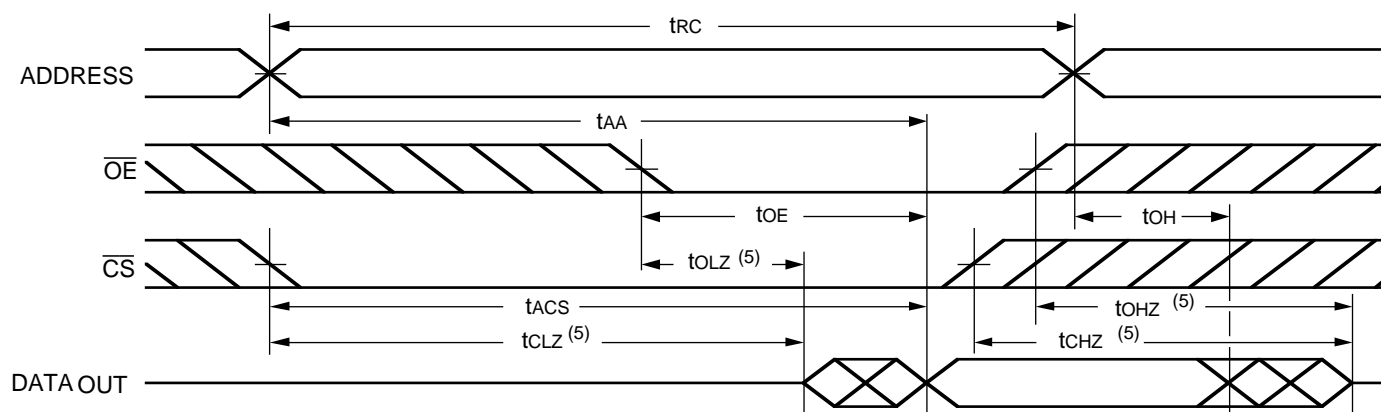
Symbol	Parameter	'4045SxxZ, '4045/4145SxxM				Unit
		-15		-20		
		Min.	Max.	Min.	Max.	
Read Cycle						
tRC	Read Cycle Time	15	—	20	—	ns
tAA	Address Access Time	—	15	—	20	ns
tACS	Chip Select Access Time	—	15	—	20	ns
tCLZ <sup>(1)</sup>	Chip Select to Output in Low-Z	3	—	5	—	ns
tOE	Output Enable to Output Valid	—	8	—	10	ns
tOLZ <sup>(1)</sup>	Output Enable to Output in Low-Z	0	—	0	—	ns
tCHZ <sup>(1)</sup>	Chip Deselect to Output in High-Z	—	8	—	10	ns
tOHZ <sup>(1)</sup>	Output Disable to Output in High-Z	—	8	—	10	ns
tOH	Output Hold from Address Change	3	—	3	—	ns
tPU <sup>(1)</sup>	Chip Select to Power-Up Time	0	—	0	—	ns
tPD <sup>(1)</sup>	Chip Deselect to Power-Down Time	—	15	—	20	ns
Write Cycle						
tWC	Write Cycle Time	15	—	20	—	ns
tCW	Chip Select to End-of-Write	12	—	15	—	ns
tAW	Address Valid to End-of-Write	12	—	15	—	ns
tAS	Address Set-up Time	0	—	0	—	ns
tWP	Write Pulse Width	12	—	15	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tWHZ <sup>(1)</sup>	Write Enable to Output in High-Z	—	8	—	13	ns
tDW	Data to Write Time Overlap	10	—	12	—	ns
tDH	Data Hold from Write Time	0	—	0	—	ns
tOW <sup>(1)</sup>	Output Active from End-of-Write	0	—	0	—	ns

**NOTE:**

1. This parameter is guaranteed by design but not tested.

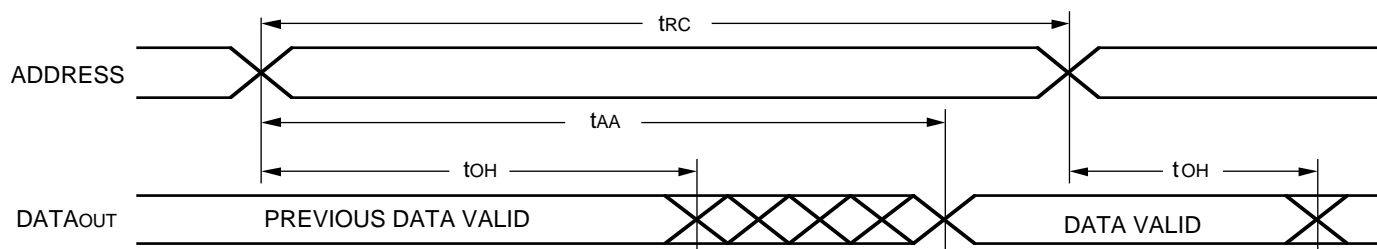
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## TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>



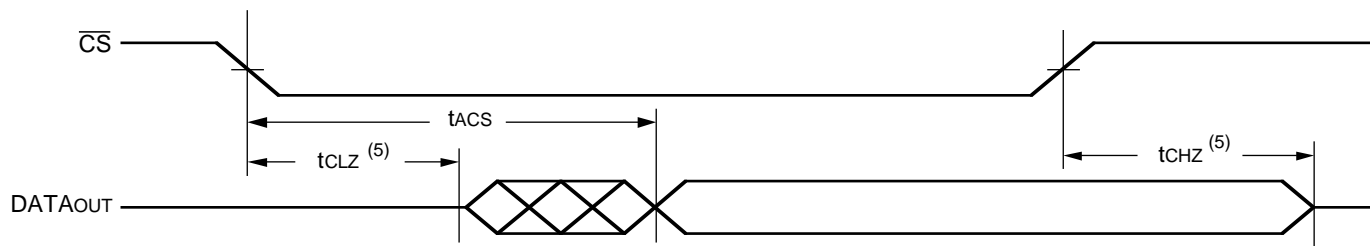
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## TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1,2,4)</sup>



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## TIMING WAVEFORM OF READ CYCLE NO. 3<sup>(1,3,4)</sup>

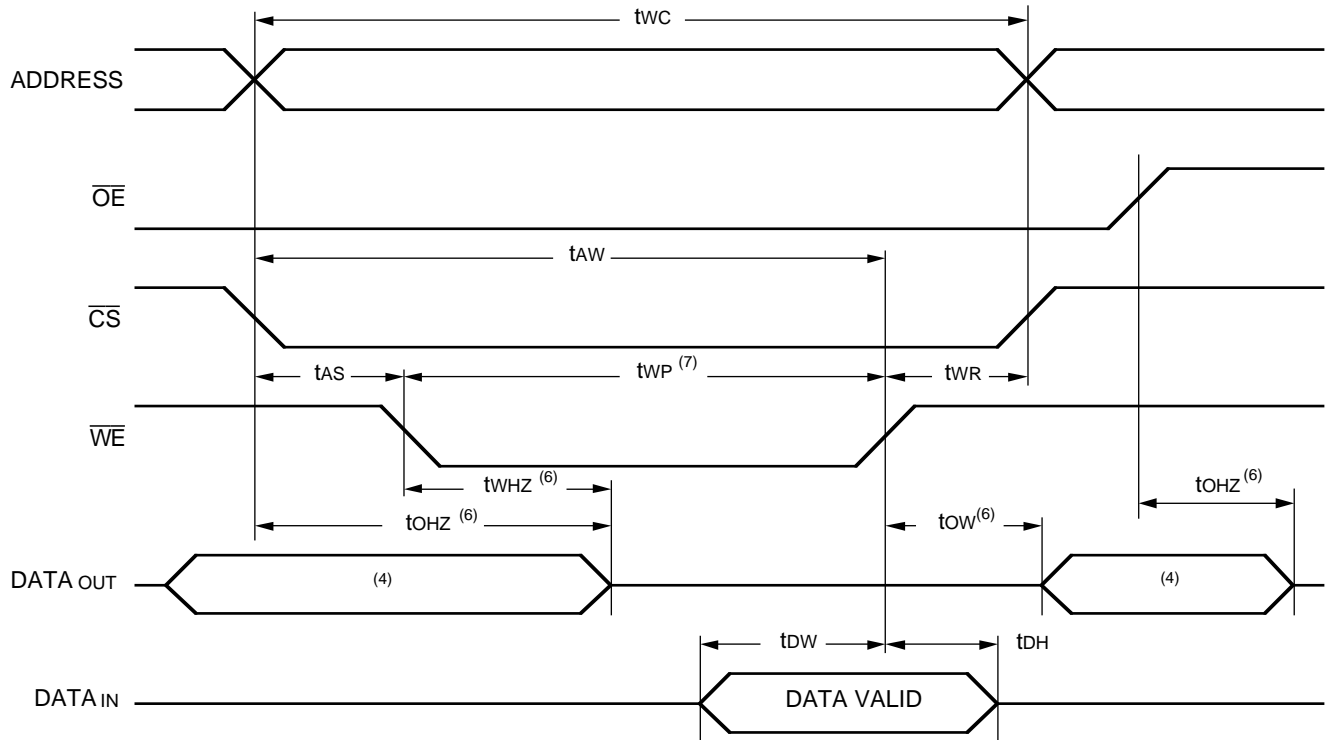


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### NOTES:

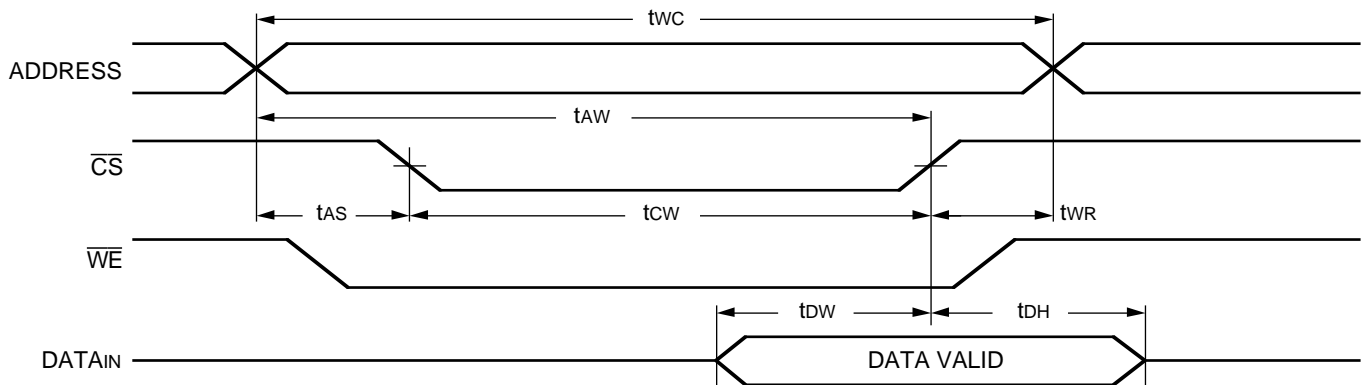
1.  $\overline{WE}$  is HIGH for Read Cycle.
2. Device is continuously selected.  $\overline{CS} = V_{IL}$ .
3. Address valid prior to or coincident with  $\overline{CS}$  transition LOW.
4.  $\overline{OE} = V_{IL}$ .
5. Transition is measured  $\pm 200\text{mV}$  from steady state. This parameter is guaranteed by design, but not tested.

## TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$ CONTROLLED) (1, 2, 3, 7)



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## TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}$ CONTROLLED) (1, 2, 3, 5)



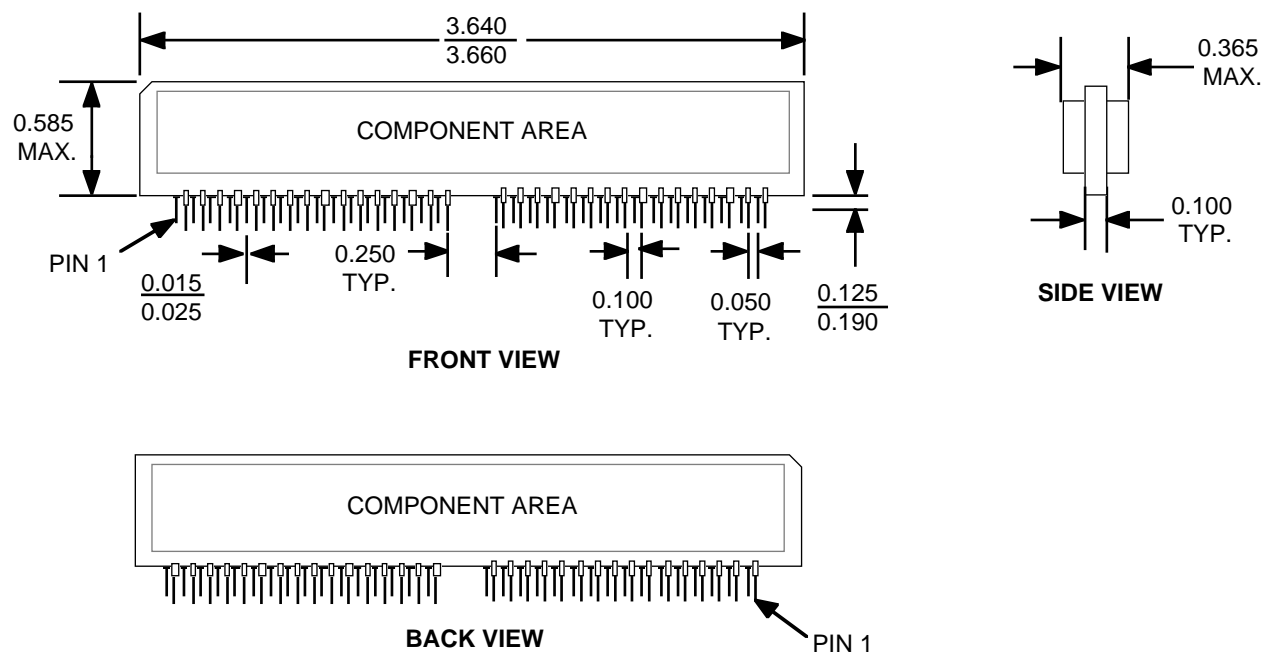
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### NOTES:

1.  $\overline{WE}$  or  $\overline{CS}$  must be HIGH during all address transitions.
2. A write occurs during the overlap ( $t_{WP}$ ) of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured  $\pm 200\text{mV}$  from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If  $\overline{OE}$  is LOW during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or  $(t_{WHZ} + t_{DW})$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{DW}$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .

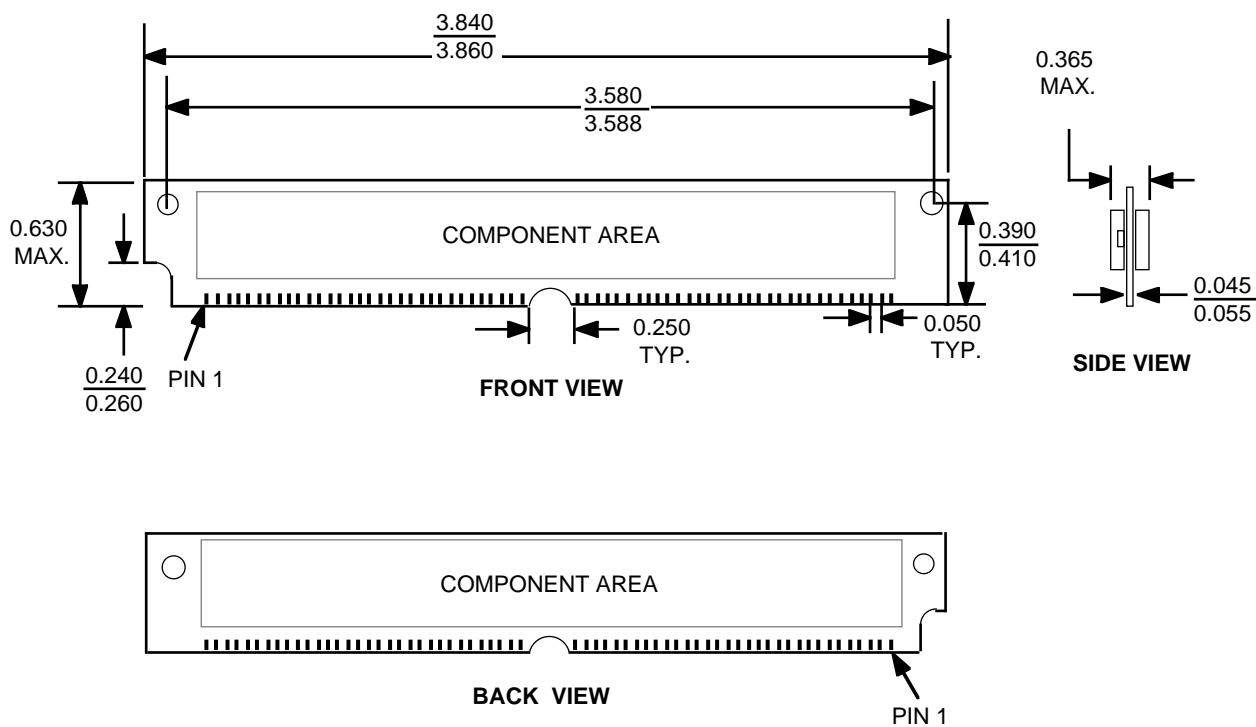
## PACKAGE DIMENSIONS

### 7MP4045 ZIP VERSION



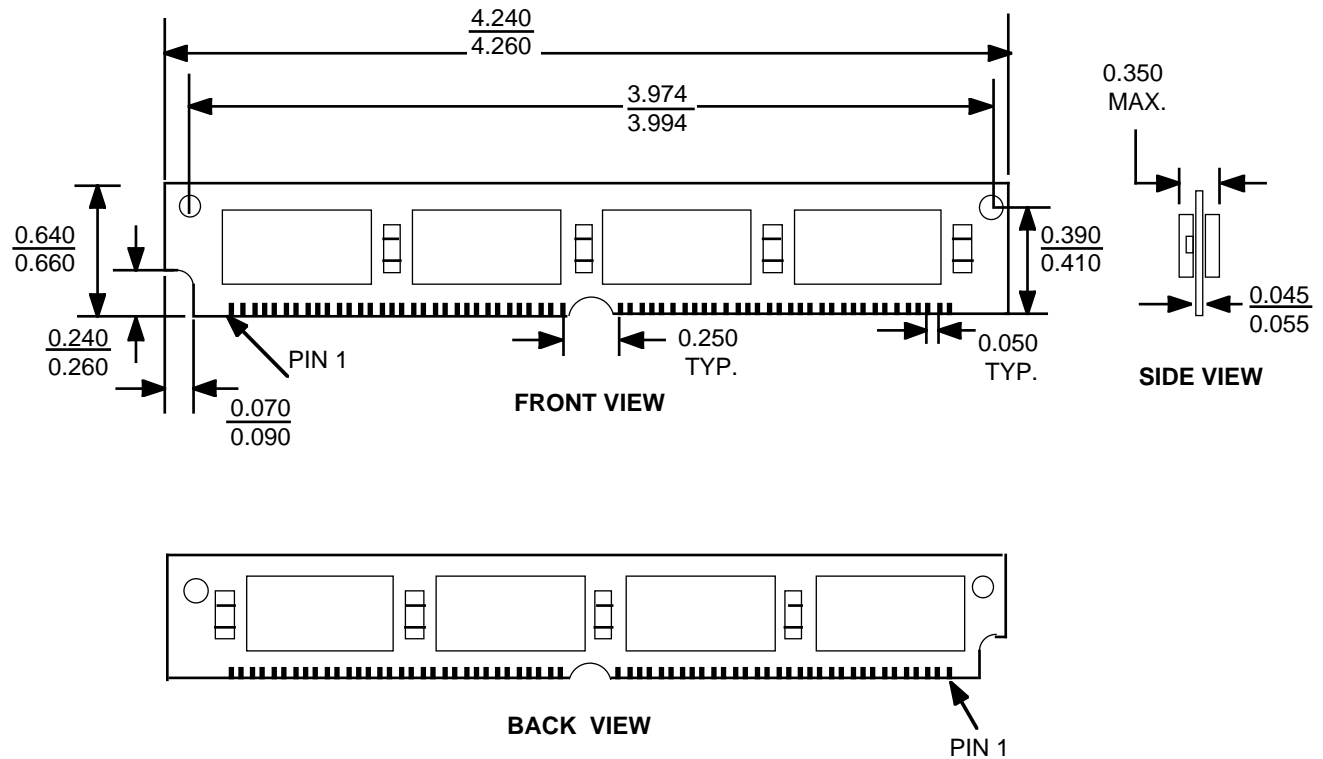
### 7MP4045 SIMM VERSION

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7MP4145 SIMM VERSION



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ORDERING INFORMATION

IDT	XXXXX	X	X	X	X	
	Device Type	Power	Speed	Package	Process/ Temperature Range	
					Blank	Commercial (0°C to +70°C)
					Z	FR-4 ZIP (Zig-Zag In-line vertical Package, 7MP4045 only)
					M	FR-4 SIMM (Single In-line Memory Module)
					15 } 20 }	Speed in Nanoseconds
					S	Standard Power
					7MP4045	256K x 32 Static RAM Module
					7MP4145	256K x 32 Static RAM Module

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