



Integrated Device Technology, Inc.

128K x 32 CMOS STATIC RAM MODULES

IDT7MP4060
IDT7MP4095

FEATURES:

- High density 4 megabit static RAM modules
- Low profile 64-pin ZIP (Zig-zag In-line vertical Package), 64-lead, 72-lead SIMMs (Single In-line Memory Modules)
- Fast access time: 15ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V ($\pm 10\%$) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible
- Gold plated fingers on the SIMM version

PIN CONFIGURATION – 7MP4095

PD ₀	2	1	GND	PD ₀ - OPEN
I/O ₀	4	3	PD ₁	PD ₁ - OPEN
I/O ₁	6	5	I/O ₈	
I/O ₂	8	7	I/O ₉	
I/O ₃	10	9	I/O ₁₀	
V _{CC}	12	11	I/O ₁₁	
A ₇	14	13	A ₀	
A ₈	16	15	A ₁	
A ₉	18	17	A ₂	
I/O ₄	20	19	I/O ₁₂	
I/O ₅	22	21	I/O ₁₃	
I/O ₆	24	23	I/O ₁₄	
I/O ₇	26	25	I/O ₁₅	
\overline{WE}	28	27	GND	
A ₁₄	30	29	A ₁₅	
\overline{CS}_1	32	31	\overline{CS}_2	
\overline{CS}_3	34	33	\overline{CS}_4	
A ₁₆	36	35	NC	
GND	38	37	\overline{OE}	
I/O ₁₆	40	39	I/O ₂₄	
I/O ₁₇	42	41	I/O ₂₅	
I/O ₁₈	44	43	I/O ₂₆	
I/O ₁₉	46	45	I/O ₂₇	
A ₁₀	48	47	A ₃	
A ₁₁	50	49	A ₄	
A ₁₂	52	51	A ₅	
A ₁₃	54	53	V _{CC}	
I/O ₂₀	56	55	A ₆	
I/O ₂₁	58	57	I/O ₂₈	
I/O ₂₂	60	59	I/O ₂₉	
I/O ₂₃	62	61	I/O ₃₀	
GND	64	63	I/O ₃₁	

**ZIP, SIMM
TOP VIEW**

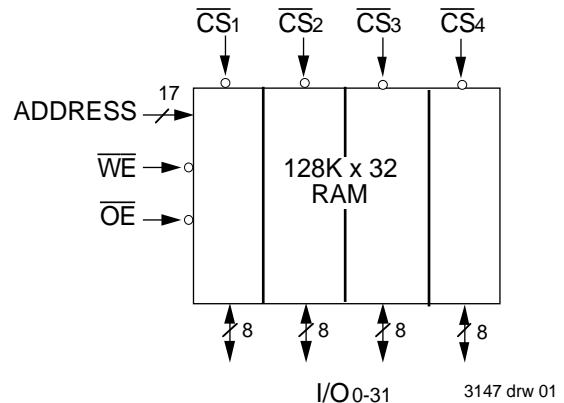
DESCRIPTION:

The IDT7MP4095/7MP4060 are 128K x 32 static RAM modules constructed on an epoxy laminate (FR-4) substrate using four 128K x 8 static RAMs in plastic SOJ packages. The IDT7MP4095/7MP4060 are available with access times as fast as 15ns with minimal power consumption.

The IDT7MP4095 is packaged in a 64-pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 64-lead SIMM (Single In-line Memory Module). The IDT7MP4060 is packaged in a 72-lead SIMM. The ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.21 inches thick. At only 0.60 inches high, this low-profile package is ideal for systems with minimum board spacing, while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4095/7MP4060 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

I/O ₀ –31	Data Inputs/Outputs
A ₀ –16	Addresses
\overline{CS}_1 –4	Chip Selects
\overline{WE}	Write Enable
\overline{OE}	Output Enable
V _{CC}	Power
GND	Ground
NC	No Connect

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COMMERCIAL TEMPERATURE RANGE

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DSC-3147/7

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PIN CONFIGURATION – 7MP4060

NC	2	1	NC	PD ₀ - OPEN
PD ₃	4	3	PD ₂	PD ₁ - OPEN
PD ₀	6	5	GND	PD ₂ - OPEN
I/O ₀	8	7	PD ₁	PD ₃ - GND
I/O ₁	10	9	I/O ₈	
I/O ₂	12	11	I/O ₉	
I/O ₃	14	13	I/O ₁₀	
V _{CC}	16	15	I/O ₁₁	
A ₇	18	17	A ₀	
A ₈	20	19	A ₁	
A ₉	22	21	A ₂	
I/O ₄	24	23	I/O ₁₂	
I/O ₅	26	25	I/O ₁₃	
I/O ₆	28	27	I/O ₁₄	
I/O ₇	30	29	I/O ₁₅	
WE	32	31	GND	
A ₁₄	34	33	A ₁₅	
CS ₁	36	35	CS ₂	
CS ₃	38	37	CS ₄	
A ₁₆	40	39	NC	
GND	42	41	OE	
I/O ₁₆	44	43	I/O ₂₄	
I/O ₁₇	46	45	I/O ₂₅	
I/O ₁₈	48	47	I/O ₂₆	
I/O ₁₉	50	49	I/O ₂₇	
A ₁₀	52	51	A ₃	
A ₁₁	54	53	A ₄	
A ₁₂	56	55	A ₅	
A ₁₃	58	57	V _{CC}	
I/O ₂₀	60	59	A ₆	
I/O ₂₁	62	61	I/O ₂₈	
I/O ₂₂	64	63	I/O ₂₉	
I/O ₂₃	66	65	I/O ₃₀	
GND	68	67	I/O ₃₁	
NC	70	69	NC	
NC	72	71	NC	

SIMM
TOP VIEW

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CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN(D)}	Input Capacitance (Data and CS)	V _(IN) = 0V	12	pF
C _{IN(A)}	Input Capacitance (Address, WE, OE)	V _(IN) = 0V	40	pF
C _{OUT}	Output Capacitance	V _(OUT) = 0V	12	pF

NOTE:

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1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	5.8	V
V _{IL}	Input Low Voltage	−0.5 ⁽¹⁾	—	0.8	V

NOTE:

3147 tbl 05

1. V_{IL} (min) = −3.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V _{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

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TRUTH TABLE

Mode	CS	OE	WE	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DATA _{OUT}	Active
Write	L	X	L	DATA _{IN}	Active
Read	L	H	H	High-Z	Active

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	°C
T _{BIAS}	Temperature Under Bias	−10 to +85	°C
T _{STG}	Storage Temperature	−55 to +125	°C
I _{OUT}	DC Output Current	50	mA

NOTES:

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1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ±10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
ILI	Input Leakage (Data and \overline{CS})	VCC = Max.; VIN = GND to VCC	—	10	μA
ILI	Input Leakage (Address, \overline{WE} , and \overline{OE})	VCC = Max.; VIN = GND to VCC	—	40	μA
ILO	Output Leakage	VCC = Max.; \overline{CS} = VIH, VOUT = GND to VCC	—	10	μA
VOL	Output Low	VCC = Min., IOL = 8mA	—	0.4	V
VOH	Output High	VCC = Min., IOH = −4mA	2.4	—	V

Symbol	Parameter	Test Conditions	Max.	Unit
ICC	Dymanic Operating Current	f = fMAX; \overline{CS} = VIL VCC = Max.; Output Open	760	mA
ISB	Standby Supply Current	$\overline{CS} \geq V_{IH}$, VCC = Max. Outputs Open, f = fMAX	160	mA
ISB1	Full Standby Supply Current	$\overline{CS} \geq V_{CC} - 0.2V$; f = 0 VIN > VCC − 0.2V or < 0.2V	60	mA

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

3147 tbl 08

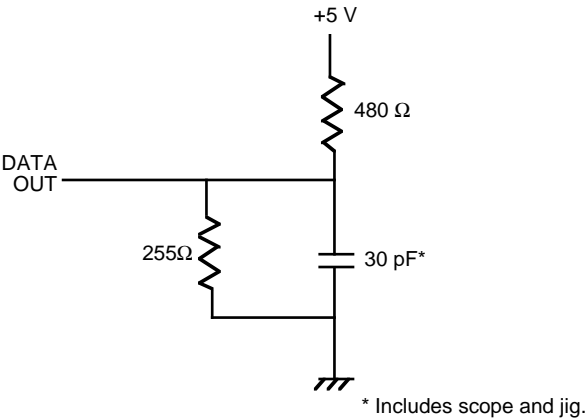


Figure 1. Output Load

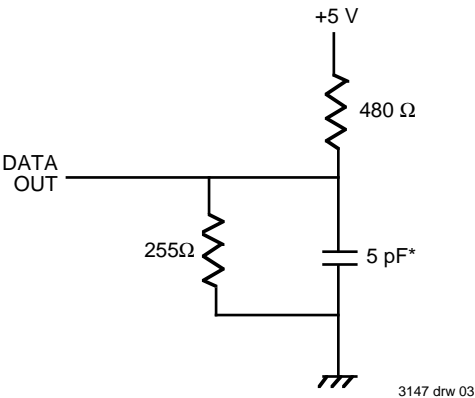


Figure 2. Output Load
(for tOLZ, tOHZ, tCHZ, tCLZ, tWHZ, tOW)

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

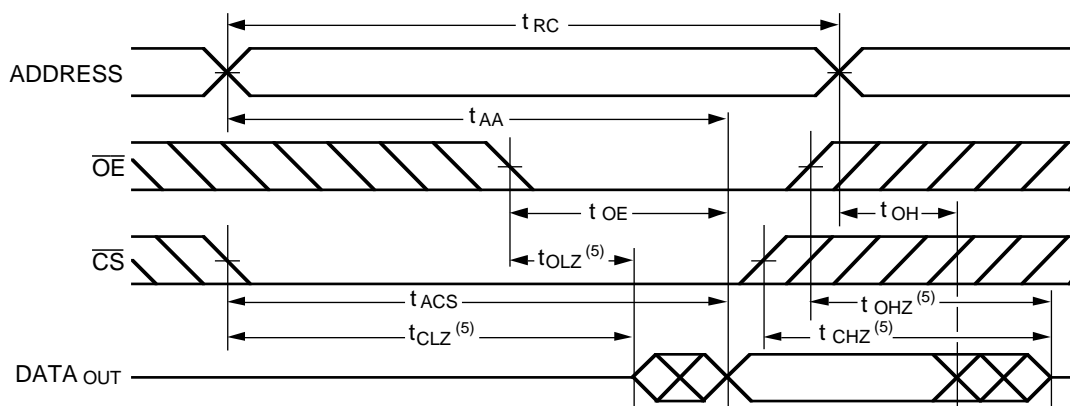
Symbol	Parameter	-15		-20		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
tRC	Read Cycle Time	15	—	20	—	ns
tAA	Address Access Time	—	15	—	20	ns
tACS	Chip Select Access Time	—	15	—	20	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low Z	3	—	3	—	ns
tOE	Output Enable to Output Valid	—	8	—	10	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low Z	0	—	0	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High Z	—	8	—	12	ns
tOHZ ⁽¹⁾	Output Disable to Output in High Z	—	8	—	12	ns
tOH	Output Hold from Address Change	3	—	3	—	ns
tPU ⁽¹⁾	Chip Select to Power-Up Time	0	—	0	—	ns
tPD ⁽¹⁾	Chip Deselect to Power-Down Time	—	15	—	20	ns
Write Cycle						
tWC	Write Cycle Time	15	—	20	—	ns
tCW	Chip Select to End of Write	12	—	18	—	ns
tAW	Address Valid to End of Write	12	—	18	—	ns
tAS	Address Set-up Time	0	—	0	—	ns
tWP	Write Pulse Width	12	—	18	—	ns
tWR	Write Recovery Time	0	—	3	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High Z	—	8	—	13	ns
tDW	Data to Write Time Overlap	10	—	12	—	ns
tDH	Data Hold from Write Time	0	—	0	—	ns
tOW ⁽¹⁾	Output Active from End of Write	3	—	3	—	ns

NOTE:

1. This parameter is guaranteed by design, but not tested.

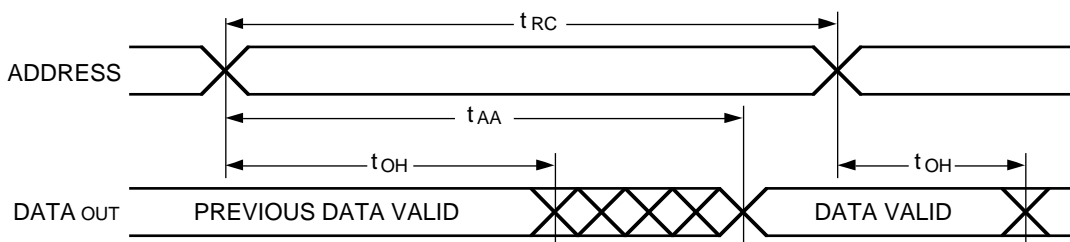
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TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



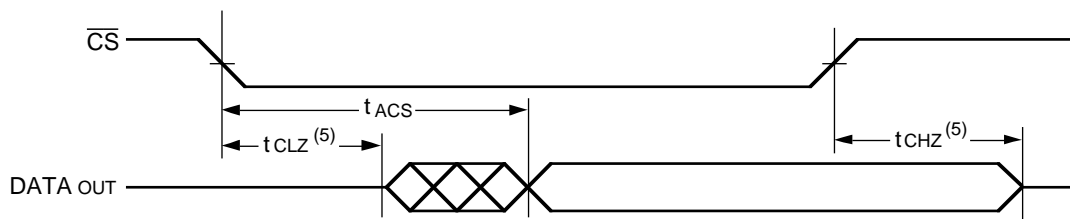
3147 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2^(1,2,4)



3147 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 3^(1,3,4)

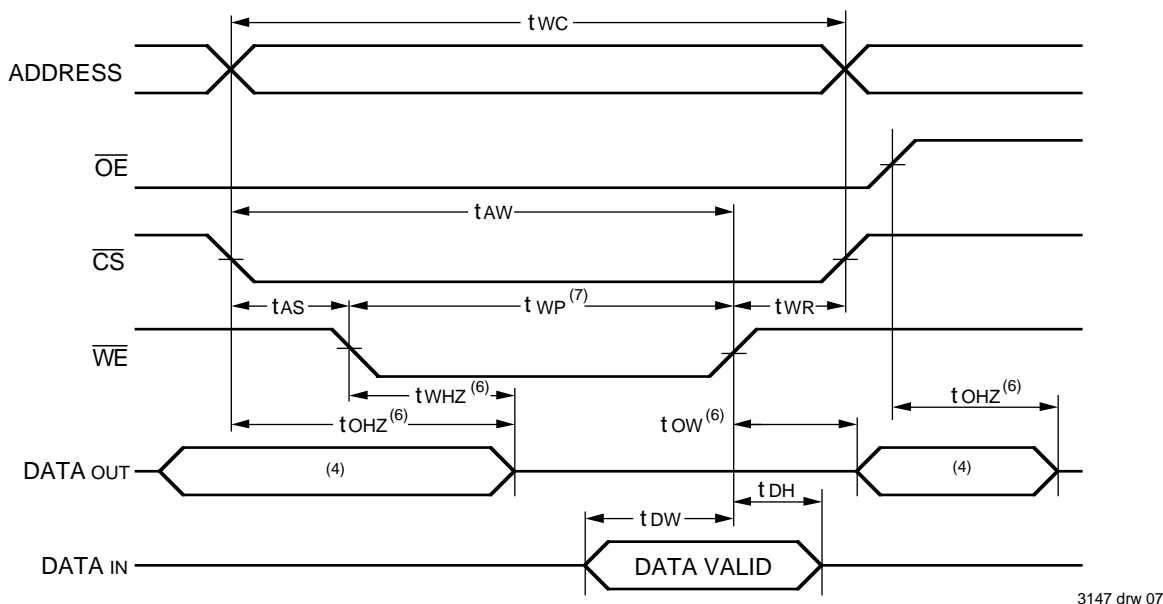


3147 drw 06

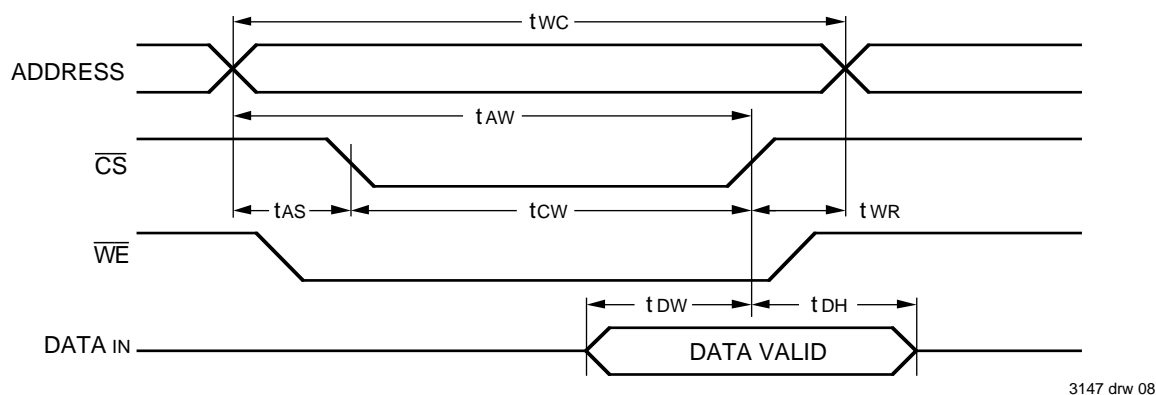
NOTES:

1. \overline{WE} is High for Read Cycle.
2. Device is continuously selected. $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with \overline{CS} transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 200\text{mV}$ from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED TIMING)^(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED TIMING)^(1, 2, 3, 5)

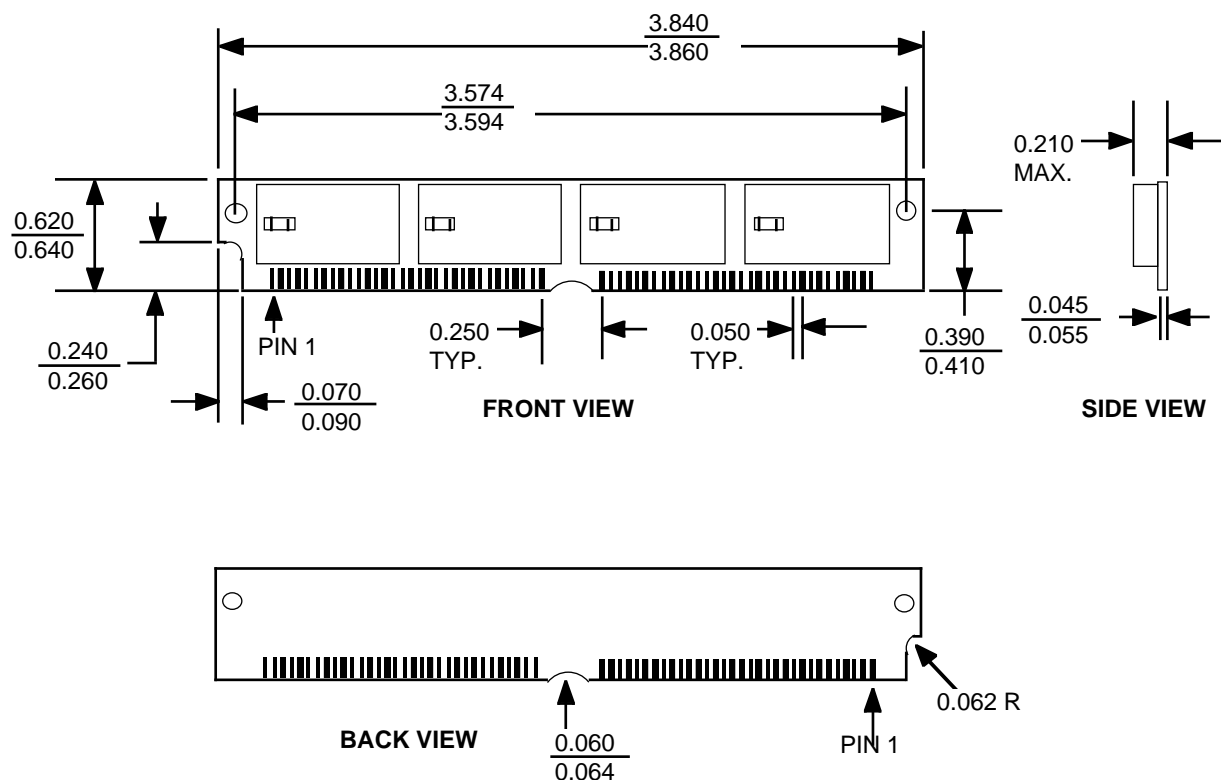


NOTES:

1. \overline{WE} or \overline{CS} must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
3. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CS} low transition occurs simultaneously with or after the \overline{WE} low transition, the outputs remain in a high impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If \overline{OE} is low during a \overline{WE} controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WHZ} + t_{DW}$).

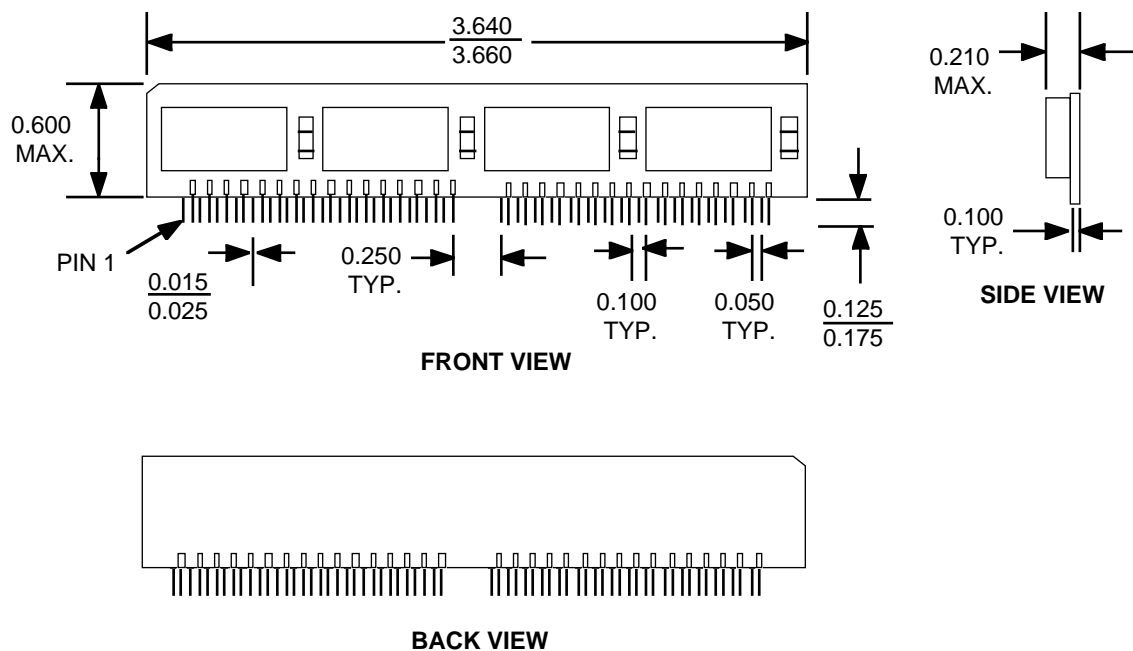
PACKAGE DIMENSIONS – IDT7MP4095

SIMM VERSION



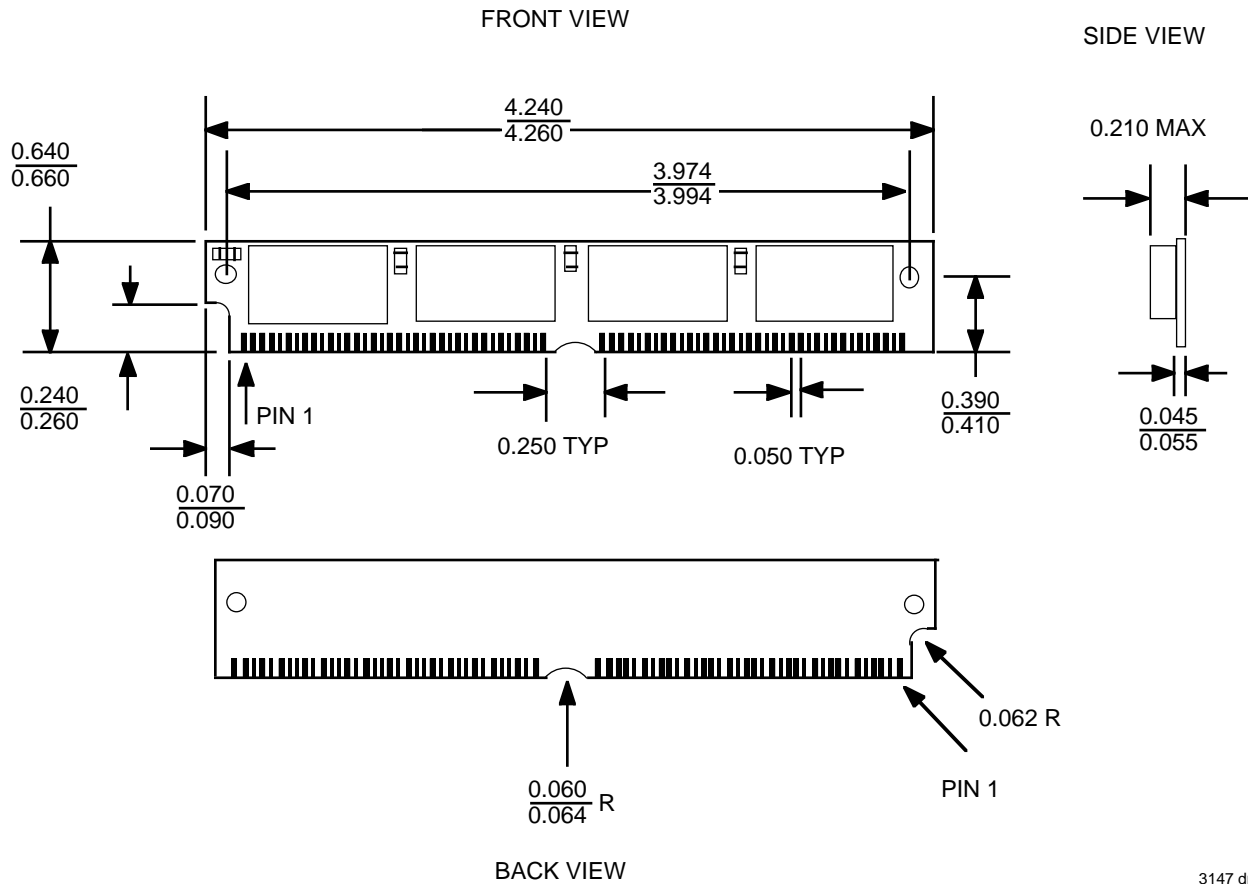
3147 drw 09

ZIP VERSION



3147 drw 10

PACKAGE DIMENSIONS – IDT7MP4060



3147 drw 11

ORDERING INFORMATION

IDT	XXXXX	X	X	X	X	
	Device Type	Power	Speed	Package	Process/ Temperature Range	
					Blank	Commercial (0°C to +70°C)
					M Z	FR-4 SIMM (Single In-line Memory Module) FR-4 ZIP (Zig-zag In-line Package)
			15 20			} Speed in Nanoseconds
			S			Standard Power
					IDT7MP4060 IDT7MP4095	128K x 32 Static RAM Module (SIMM only) 128K x 32 Static RAM Module

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