



Integrated Device Technology, Inc.

# 1M x 32 CMOS STATIC RAM MODULE

IDT7MP4120

## FEATURES

- High-density 4MB Static RAM module
- Low profile 72-pin ZIP (Zig-zag In-line vertical Package) or 72-pin SIMM (Single In-line Memory Module)
- Fast access time: 20ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V ( $\pm 10\%$ ) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

## PIN CONFIGURATION<sup>(1)</sup>

NC	2	1	NC	PD <sub>0</sub> - GND
PD <sub>3</sub>	4	3	PD <sub>2</sub>	PD <sub>1</sub> - NC
PD <sub>0</sub>	6	5	GND	PD <sub>2</sub> - GND
I/O <sub>0</sub>	8	7	PD <sub>1</sub>	PD <sub>3</sub> - NC
I/O <sub>1</sub>	10	9	I/O <sub>8</sub>	
I/O <sub>2</sub>	12	11	I/O <sub>9</sub>	
I/O <sub>3</sub>	14	13	I/O <sub>10</sub>	
V <sub>CC</sub>	16	15	I/O <sub>11</sub>	
A <sub>7</sub>	18	17	A <sub>0</sub>	
A <sub>8</sub>	20	19	A <sub>1</sub>	
A <sub>9</sub>	22	21	A <sub>2</sub>	
I/O <sub>4</sub>	24	23	I/O <sub>12</sub>	
I/O <sub>5</sub>	26	25	I/O <sub>13</sub>	
I/O <sub>6</sub>	28	27	I/O <sub>14</sub>	
I/O <sub>7</sub>	30	29	I/O <sub>15</sub>	
WE	32	31	GND	
A <sub>14</sub>	34	33	A <sub>15</sub>	
CS <sub>1</sub>	36	35	CS <sub>2</sub>	
CS <sub>3</sub>	38	37	CS <sub>4</sub>	
A <sub>16</sub>	40	39	A <sub>17</sub>	
GND	42	41	OE	
I/O <sub>16</sub>	44	43	I/O <sub>24</sub>	
I/O <sub>17</sub>	46	45	I/O <sub>25</sub>	
I/O <sub>18</sub>	48	47	I/O <sub>26</sub>	
I/O <sub>19</sub>	50	49	I/O <sub>27</sub>	
A <sub>10</sub>	52	51	A <sub>3</sub>	
A <sub>11</sub>	54	53	A <sub>4</sub>	
A <sub>12</sub>	56	55	A <sub>5</sub>	
A <sub>13</sub>	58	57	V <sub>CC</sub>	
I/O <sub>20</sub>	60	59	A <sub>6</sub>	
I/O <sub>21</sub>	62	61	I/O <sub>28</sub>	
I/O <sub>22</sub>	64	63	I/O <sub>29</sub>	
I/O <sub>23</sub>	66	65	I/O <sub>30</sub>	
GND	68	67	I/O <sub>31</sub>	
A <sub>19</sub>	70	69	A <sub>18</sub>	
NC	72	71	NC	

ZIP, SIMM  
TOP VIEW

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### NOTE:

1. Pins 3, 4, 6 and 7 (PD<sub>0</sub>, PD<sub>1</sub>, PD<sub>2</sub> and PD<sub>3</sub> respectively) are read by the user to determine the density of the module. If PD<sub>0</sub> reads GND, PD<sub>1</sub> reads NC, PD<sub>2</sub> reads GND and PD<sub>3</sub> reads NC, then the module has a 1M depth.

## DESCRIPTION

The IDT7MP4120 is a 1M x 32 Static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 1M x 4 Static RAMs in plastic packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. The IDT7MP4120 is available with access time as fast as 20ns with minimal power consumption.

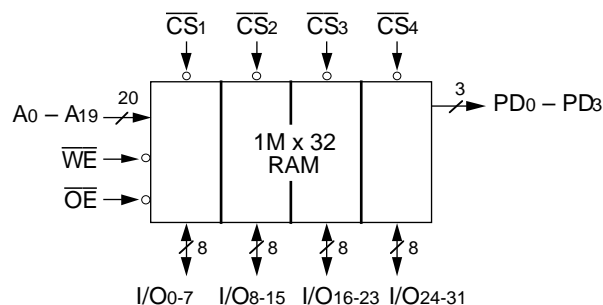
The IDT7MP4120 is packaged in a 72-pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 72-pin SIMM (Single In-line Memory Module). The ZIP configuration allows 72 pins to be placed on a package 4.05" long and 0.365" wide. At only 0.60" high, this low-profile package is ideal for systems with minimum board spacing while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4120 are TTL-compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Four identification pins (PD<sub>0</sub>, PD<sub>1</sub>, PD<sub>2</sub> and PD<sub>3</sub>) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD<sub>0</sub>, PD<sub>1</sub>, PD<sub>2</sub> and PD<sub>3</sub> to determine a 1M depth.

The contact pins are plated with 100 micro-inches of nickel covered by 30 micro-inches minimum of selective gold.

## FUNCTIONAL BLOCK DIAGRAM



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## PIN NAMES

I/O <sub>0</sub> –I/O <sub>31</sub>	Data Inputs/Outputs
A <sub>0</sub> –A <sub>19</sub>	Addresses
CS <sub>1</sub> –CS <sub>4</sub>	Chip Selects
WE	Write Enable
OE	Output Enable
PD <sub>0</sub> –PD <sub>3</sub>	Depth Identification
V <sub>CC</sub>	Power
GND	Ground
NC	No Connect

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

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## COMMERCIAL TEMPERATURE RANGE

SEPTEMBER 1996

**CAPACITANCE** ( $T_A = +25^\circ\text{C}$ ,  $F = 1.0\text{MHz}$ )

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>I/O</sub>	Data I/O Capacitance	$V_{(IN)} = 0\text{V}$	15	pF
C <sub>IN1</sub>	Input Capacitance (Address)	$V_{(IN)} = 0\text{V}$	60	pF
C <sub>IN2</sub>	Input Capacitance ( $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	$V_{(IN)} = 0\text{V}$	75	pF
C <sub>IN3</sub>	Input Capacitance ( $\overline{\text{CS}}$ )	$V_{(IN)} = 0\text{V}$	20	pF

**NOTE:**

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1. This parameter is guaranteed by design but not tested.

**RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	6.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

**NOTE:**

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1.  $V_{IL}(\text{min}) = -1.5\text{V}$  for pulse width less than 10ns.

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Ambient Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +70°C	0V	5.0V $\pm$ 10%

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**DC ELECTRICAL CHARACTERISTICS**( $V_{CC} = 5.0\text{V} \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I <sub>LI</sub>	Input Leakage (Address and Control)	$V_{CC} = \text{Max.}; V_{IN} = \text{GND to } V_{CC}$	—	80	$\mu\text{A}$
I <sub>LI</sub>	Input Leakage (Data)	$V_{CC} = \text{Max.}; V_{IN} = \text{GND to } V_{CC}$	—	10	$\mu\text{A}$
I <sub>LO</sub>	Output Leakage	$V_{CC} = \text{Max.}; \overline{\text{CS}} = V_{IH}, V_{OUT} = \text{GND to } V_{CC}$	—	10	$\mu\text{A}$
V <sub>OL</sub>	Output LOW	$V_{CC} = \text{Min.}, I_{OL} = 8\text{mA}$	—	0.4	V
V <sub>OH</sub>	Output HIGH	$V_{CC} = \text{Min.}, I_{OH} = -4\text{mA}$	2.4	—	V

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Symbol	Parameter	Test Conditions	7MP4120 Max.	Unit
I <sub>CC</sub>	Dynamic Operating Current	$f = f_{\text{MAX}}; \overline{\text{CS}} = V_{IL}$ $V_{CC} = \text{Max.}; \text{Output Open}$	1280	mA
I <sub>SB</sub>	Standby Supply Current	$\overline{\text{CS}} \geq V_{IH}, V_{CC} = \text{Max.}$ Outputs Open, $f = f_{\text{MAX}}$	480	mA
I <sub>SB1</sub>	Full Standby Supply Current	$\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}; f = 0$ $V_{IN} > V_{CC} - 0.2\text{V}$ or $< 0.2\text{V}$	120	mA

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**TRUTH TABLE**

Mode	$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DATA <sub>OUT</sub>	Active
Write	L	X	L	DATA <sub>IN</sub>	Active
Read	L	H	H	High-Z	Active

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**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	°C
T <sub>BIAS</sub>	Temperature Under Bias	-10 to +85	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
I <sub>OUT</sub>	DC Output Current	50	mA

**NOTE:**

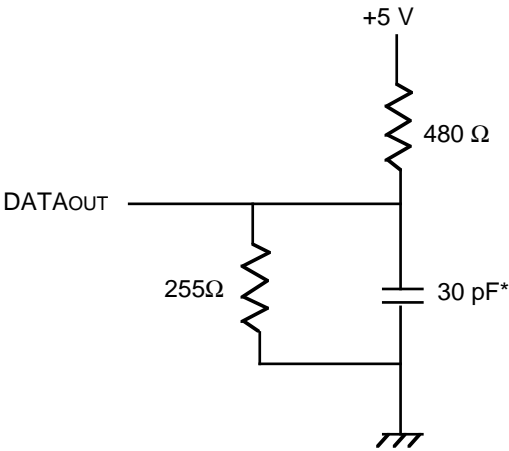
3019 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

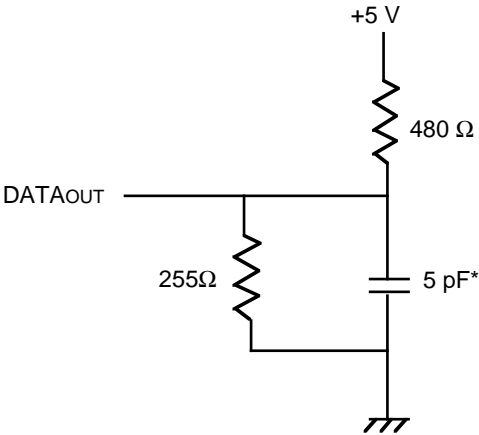
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\*Includes scope and jig.

Figure 1. Output Load



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Figure 2. Output Load  
(for tOLZ,tOHZ, tCHZ, tCLZ, tWHZ, tOW)

## AC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 5V ±10%, T<sub>A</sub> = 0°C to +70°C)

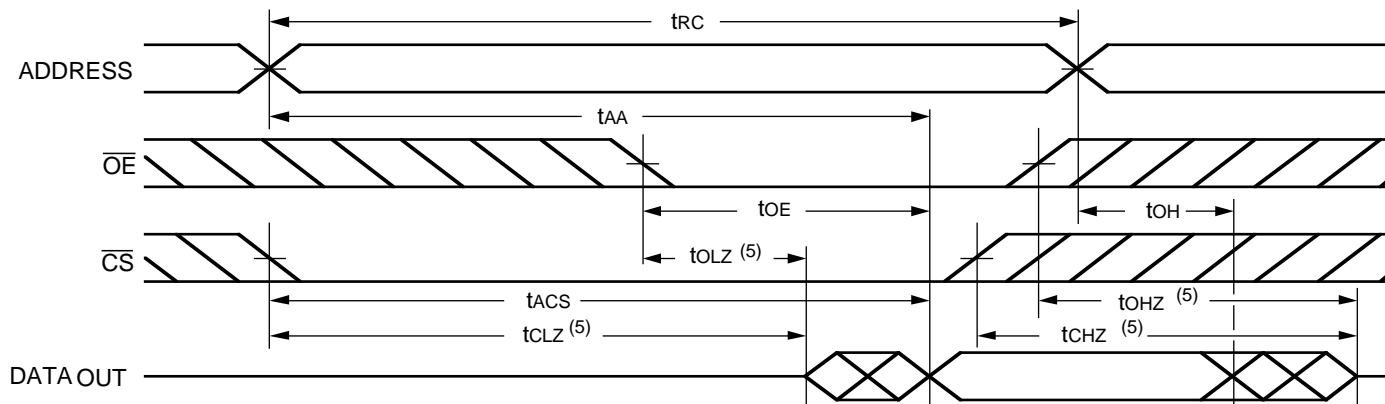
Symbol	Parameter	7MP4120SxxZ/M				Unit
		-20		-25		
		Min.	Max.	Min.	Max.	
Read Cycle						
tRC	Read Cycle Time	20	—	25	—	ns
tAA	Address Access Time	—	20	—	25	ns
tACS	Chip Select Access Time	—	20	—	25	ns
tCLZ <sup>(1)</sup>	Chip Select to Output in Low-Z	3	—	3	—	ns
tOE	Output Enable to Output Valid	—	12	—	15	ns
tOLZ <sup>(1)</sup>	Output Enable to Output in Low-Z	0	—	0	—	ns
tCHZ <sup>(1)</sup>	Chip Deselect to Output in High-Z	—	10	—	12	ns
tOHZ <sup>(1)</sup>	Output Disable to Output in High-Z	—	10	—	12	ns
tOH	Output Hold from Address Change	3	—	3	—	ns
tPU <sup>(1)</sup>	Chip Select to Power-Up Time	0	—	0	—	ns
tPD <sup>(1)</sup>	Chip Deselect to Power-Down Time	—	20	—	25	ns
Write Cycle						
tWC	Write Cycle Time	20	—	25	—	ns
tCW	Chip Select to End-of-Write	17	—	20	—	ns
tAW	Address Valid to End-of-Write	17	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	ns
tWR	Write Recovery Time	3	—	3	—	ns
tWHZ <sup>(1)</sup>	Write Enable to Output in High-Z	—	10	—	15	ns
tdW	Data to Write Time Overlap	12	—	15	—	ns
tdH	Data Hold from Write Time	0	—	0	—	ns
tOW <sup>(1)</sup>	Output Active from End-of-Write	0	—	0	—	ns

**NOTE:**

1. This parameter is guaranteed by design, but not tested.

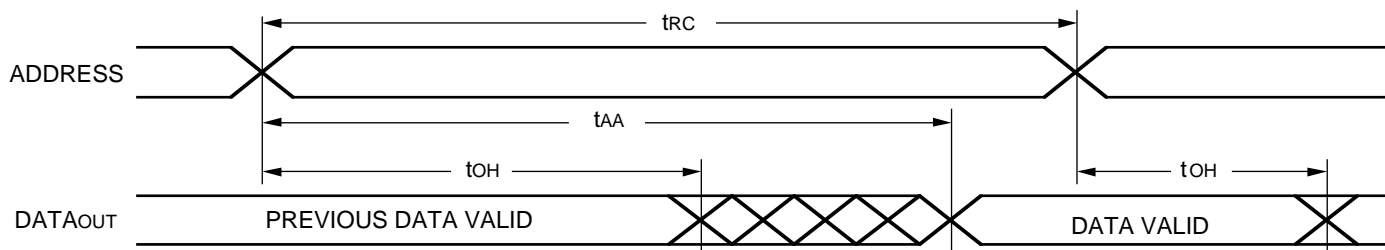
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## TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>



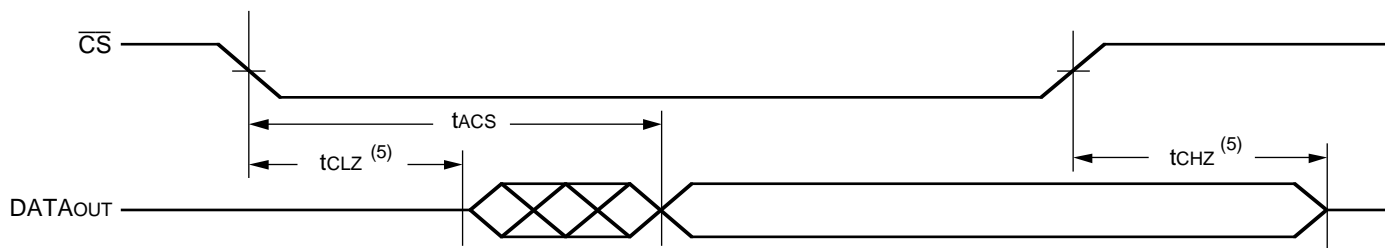
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## TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1,2,4)</sup>



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## TIMING WAVEFORM OF READ CYCLE NO. 3<sup>(1,3,4)</sup>

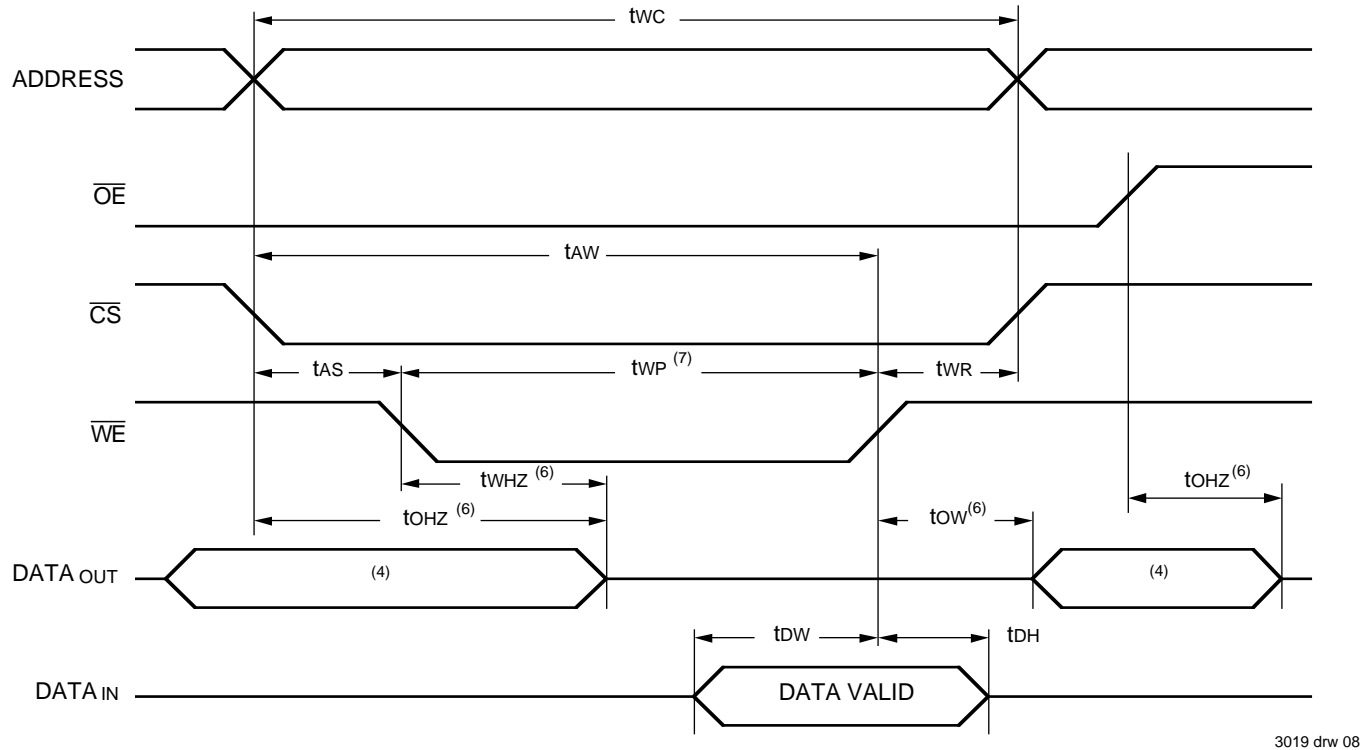


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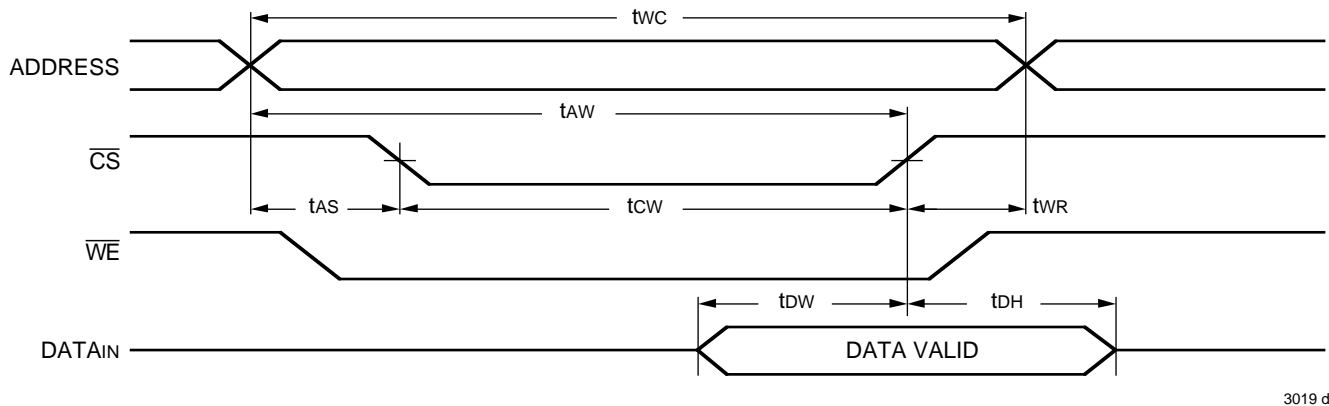
### NOTES:

1.  $\overline{WE}$  is HIGH for Read Cycle.
2. Device is continuously selected.  $\overline{CS} = V_{IL}$ .
3. Address valid prior to or coincident with  $\overline{CS}$  transition LOW.
4.  $\overline{OE} = V_{IL}$ .
5. Transition is measured  $\pm 200\text{mV}$  from steady state. This parameter is guaranteed by design, but not tested.

## TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$ CONTROLLED) (1, 2, 3, 7)



## TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}$ CONTROLLED) (1, 2, 3, 5)

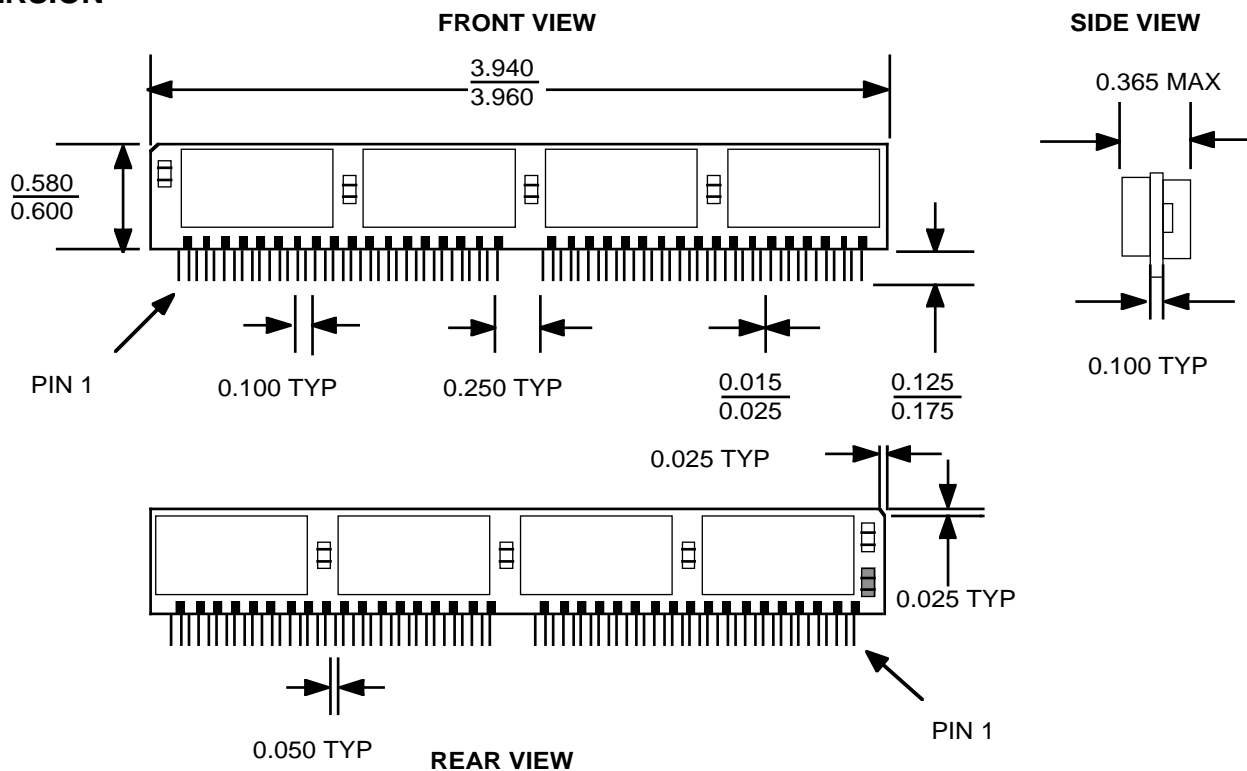


### NOTES:

1.  $\overline{WE}$  or  $\overline{CS}$  must be HIGH during all address transitions.
2. A write occurs during the overlap ( $t_{WP}$ ) of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured  $\pm 200\text{mV}$  from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If  $\overline{OE}$  is LOW during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or ( $t_{WHZ} + t_{DW}$ ) to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{DW}$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .

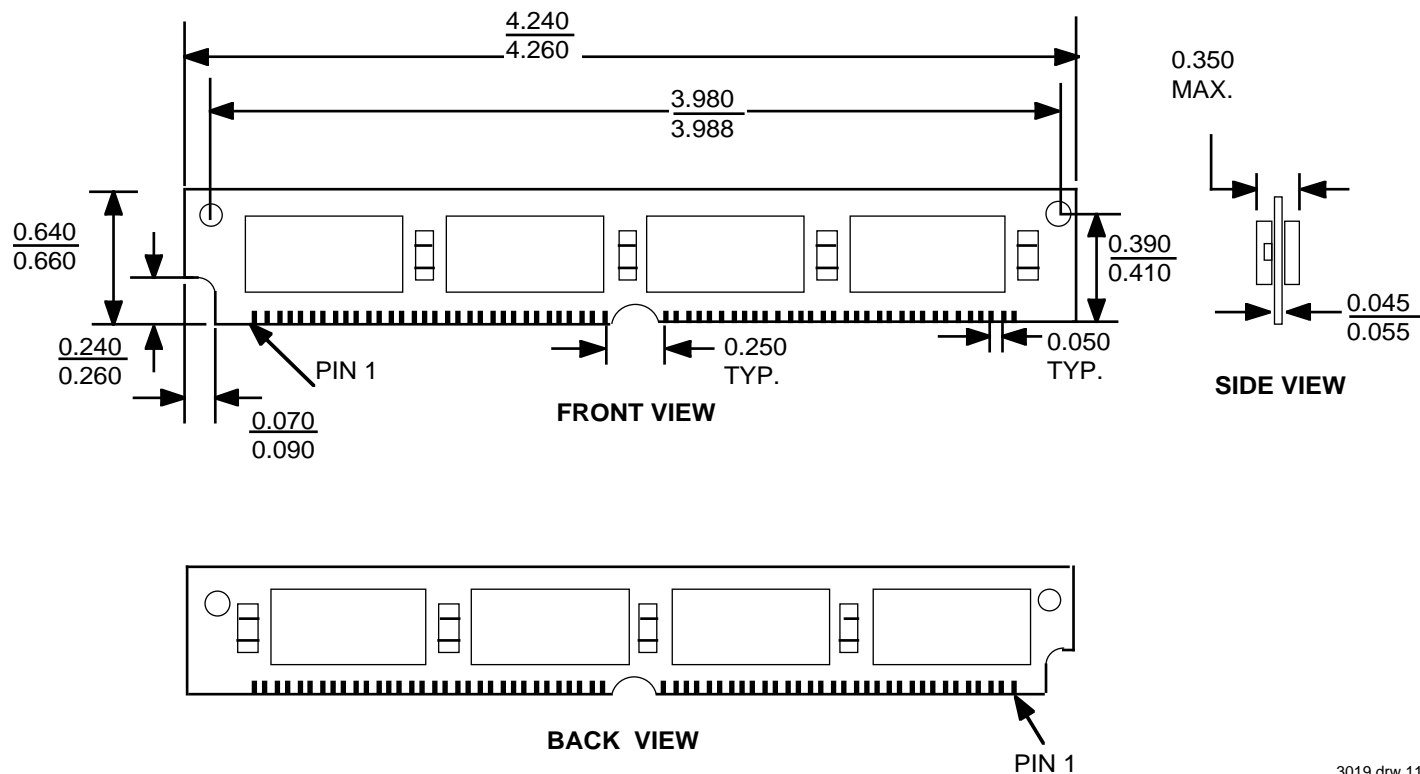
## PACKAGE DIMENSIONS

### ZIP VERSION



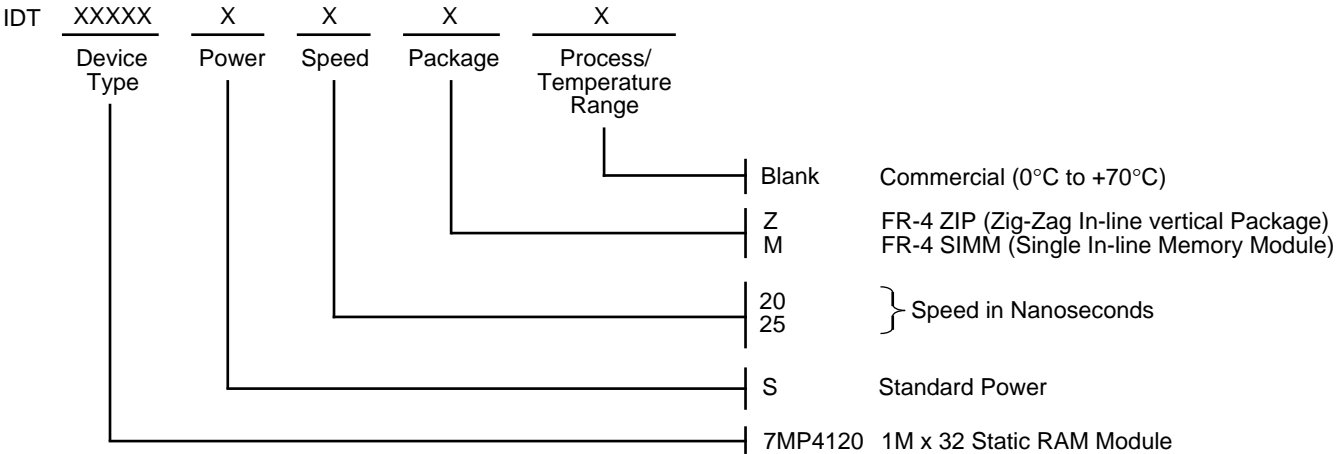
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### SIMM VERSION



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ORDERING INFORMATION



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