



# 256K x 32 CMOS Static RAM Module

**IDT7MP4045**  
**IDT7MP4145**

## Features

- ♦ High density 1 megabyte static RAM module (IDT7MP4145 upgradeable to 4 megabyte, IDT7MP4120)
- ♦ Low profile 64 pin ZIP (Zig-zag In-line vertical Package) or 64 pin SIMM (Single In-line Memory Module) for IDT7MP4045 and 72 pin SIMM (Single In-line Memory Module) for IDT7MP4145
- ♦ Very fast access time: 15ns (max.)
- ♦ Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- ♦ Single 5V ( $\pm 10\%$ ) power supply
- ♦ Multiple GND pins and decoupling capacitors for maximum noise immunity
- ♦ Inputs/outputs directly TTL-compatible

## Pin Configuration 7MP4045<sup>(1)</sup>

PD <sub>0</sub>	2	1	GND	PD <sub>0</sub> - GND
I/O <sub>0</sub>	4	3	PD <sub>1</sub>	PD <sub>1</sub> - GND
I/O <sub>1</sub>	6	5	I/O <sub>8</sub>	
I/O <sub>2</sub>	8	7	I/O <sub>9</sub>	
I/O <sub>3</sub>	10	9	I/O <sub>10</sub>	
V <sub>CC</sub>	12	11	I/O <sub>11</sub>	
A <sub>7</sub>	14	13	A <sub>0</sub>	
A <sub>8</sub>	16	15	A <sub>1</sub>	
A <sub>9</sub>	18	17	A <sub>2</sub>	
I/O <sub>4</sub>	20	19	I/O <sub>12</sub>	
I/O <sub>5</sub>	22	21	I/O <sub>13</sub>	
I/O <sub>6</sub>	24	23	I/O <sub>14</sub>	
I/O <sub>7</sub>	26	25	I/O <sub>15</sub>	
WE	28	27	GND	
A <sub>14</sub>	30	29	A <sub>15</sub>	
CS <sub>1</sub>	32	31	CS <sub>2</sub>	
CS <sub>3</sub>	34	33	CS <sub>4</sub>	
A <sub>16</sub>	36	35	A <sub>17</sub>	
GND	38	37	OE	
I/O <sub>16</sub>	40	39	I/O <sub>24</sub>	
I/O <sub>17</sub>	42	41	I/O <sub>25</sub>	
I/O <sub>18</sub>	44	43	I/O <sub>26</sub>	
I/O <sub>19</sub>	46	45	I/O <sub>27</sub>	
A <sub>10</sub>	48	47	A <sub>3</sub>	
A <sub>11</sub>	50	49	A <sub>4</sub>	
A <sub>12</sub>	52	51	A <sub>5</sub>	
A <sub>13</sub>	54	53	V <sub>CC</sub>	
I/O <sub>20</sub>	56	55	A <sub>6</sub>	
I/O <sub>21</sub>	58	57	I/O <sub>28</sub>	
I/O <sub>22</sub>	60	59	I/O <sub>29</sub>	
I/O <sub>23</sub>	62	61	I/O <sub>30</sub>	
GND	64	63	I/O <sub>31</sub>	

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## ZIP, SIMM Top View

### NOTE:

1. Pins 2 and 3 (PD<sub>0</sub> and PD<sub>1</sub>) are read by the user to determine the density of the module. If PD<sub>0</sub> reads GND and PD<sub>1</sub> reads GND, then the module has a 256K depth.

## Description

The IDT7MP4045/4145 is a 256K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. The IDT7MP4045 is available with access time as fast as 10ns with minimal power consumption.

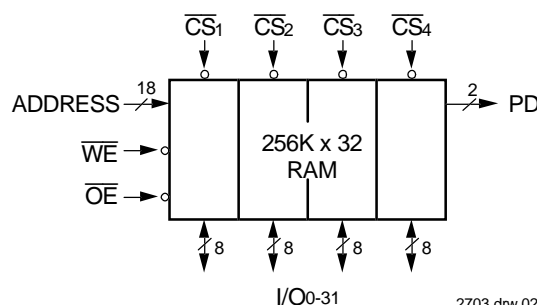
The IDT7MP4045 is packaged in a 64 pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 64 pin SIMM (Single In-line Memory Module) where as the 7MP4145 is packaged in a 72 pin SIMM (Single In-line Memory Module). The 4045 ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.365 inches wide. The 7MP4045 ZIP is only 0.585 inches high, this low profile package is ideal for systems with minimum board spacing while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4045/4145 are TTL-compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Identification pins are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD pins to determine a 256K depth.

The contact pins are plated with 100 micro-inches of nickel covered by 30 micro-inches minimum of selective gold.

## Functional Block Diagram



**DECEMBER 1999**

## Pin Names

I/O <sub>0-31</sub>	Data Inputs/Outputs
A <sub>0-17</sub>	Addresses
$\overline{CS}_{1-4}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD <sub>0-1</sub>	Depth Identification
V <sub>CC</sub>	Power
GND	Ground
NC	No Connect

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## Capacitance (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C <sub>IN(C)</sub>	Input Capacitance ( $\overline{CS}$ )	V <sub>IN</sub> = 0V	20	pF
C <sub>IN(A)</sub>	Input Capacitance (Address & Control)	V <sub>IN</sub> = 0V	70	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	12	pF

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### NOTE:

1. This parameter is guaranteed by design but not tested.

## Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	6.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

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### NOTE:

1. V<sub>IL</sub> (min) = -1.5V for pulse width less than 10ns.

## Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +70°C	0V	5V ± 10%

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## Pin Configuration 7MP4145<sup>(1)</sup>

NC	2	1	NC	PD <sub>0</sub> - GND
PD <sub>3</sub>	4	3	PD <sub>2</sub>	PD <sub>1</sub> - GND
PD <sub>0</sub>	6	5	GND	PD <sub>2</sub> - OPEN
I/O <sub>0</sub>	8	7	PD <sub>1</sub>	PD <sub>3</sub> - OPEN
I/O <sub>1</sub>	10	9	I/O <sub>8</sub>	
I/O <sub>2</sub>	12	11	I/O <sub>9</sub>	
I/O <sub>3</sub>	14	13	I/O <sub>10</sub>	
V <sub>CC</sub>	16	15	I/O <sub>11</sub>	
A <sub>7</sub>	18	17	A <sub>0</sub>	
A <sub>8</sub>	20	19	A <sub>1</sub>	
A <sub>9</sub>	22	21	A <sub>2</sub>	
I/O <sub>4</sub>	24	23	I/O <sub>12</sub>	
I/O <sub>5</sub>	26	25	I/O <sub>13</sub>	
I/O <sub>6</sub>	28	27	I/O <sub>14</sub>	
I/O <sub>7</sub>	30	29	I/O <sub>15</sub>	
$\overline{WE}$	32	31	GND	
A <sub>14</sub>	34	33	A <sub>15</sub>	
$\overline{CS}_1$	36	35	$\overline{CS}_2$	
$\overline{CS}_3$	38	37	$\overline{CS}_4$	
A <sub>16</sub>	40	39	A <sub>17</sub>	
GND	42	41	$\overline{OE}$	
I/O <sub>16</sub>	44	43	I/O <sub>24</sub>	
I/O <sub>17</sub>	46	45	I/O <sub>25</sub>	
I/O <sub>18</sub>	48	47	I/O <sub>26</sub>	
I/O <sub>19</sub>	50	49	I/O <sub>27</sub>	
A <sub>10</sub>	52	51	A <sub>3</sub>	
A <sub>11</sub>	54	53	A <sub>4</sub>	
A <sub>12</sub>	56	55	A <sub>5</sub>	
A <sub>13</sub>	58	57	V <sub>CC</sub>	
I/O <sub>20</sub>	60	59	A <sub>6</sub>	
I/O <sub>21</sub>	62	61	I/O <sub>28</sub>	
I/O <sub>22</sub>	64	63	I/O <sub>29</sub>	
I/O <sub>23</sub>	66	65	I/O <sub>30</sub>	
GND	68	67	I/O <sub>31</sub>	
NC	70	69	NC	
NC	72	71	NC	

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## SIMM Top View

### NOTE:

1. Pins 3,4,6, and 7 (PD<sub>0-3</sub>) are read by the user to determine the density of the module. If PD<sub>0</sub>, PD<sub>1</sub> read GND and PD<sub>2</sub>, PD<sub>3</sub> read OPEN, then the module has a 256K depth.

## Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

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## Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Commercial	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
$T_A$	Operating Temperature	0 to +70	°C
$T_{BIAS}$	Temperature Under Bias	-10 to +85	°C
$T_{STG}$	Storage Temperature	-55 to +125	°C
$I_{OUT}$	DC Output Current	50	mA

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### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC Electrical Characteristics

( $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ )

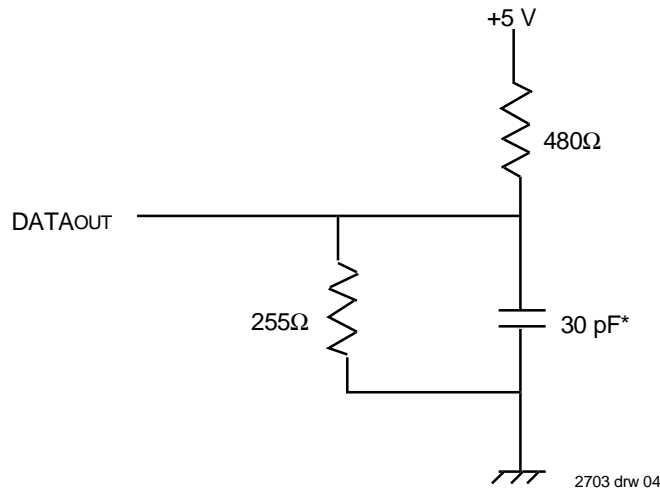
Symbol	Parameter	Test Condition	Min.	Max.	Unit
$I_{LIL}$	Input Leakage Current (Address and Control)	$V_{CC} = \text{Max.}, V_{IN} = \text{GND to } V_{CC}$	—	80	$\mu A$
$I_{LIL}$	Input Leakage Current (Data)	$V_{CC} = \text{Max.}, V_{IN} = \text{GND to } V_{CC}$	—	10	$\mu A$
$I_{LOL}$	Output Leakage Current	$V_{CC} = \text{Max.}, \overline{CS} = V_{IH}, V_{OUT} = 0V \text{ to } V_{CC}$	—	10	$\mu A$
$V_{OL}$	Output Low Voltage	$I_{OL} = 8mA, V_{CC} = \text{Min.}$	—	0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -4mA, V_{CC} = \text{Min.}$	2.4	—	V
$I_{CC}$	Dynamic Operating Current	$V_{CC} = \text{Max.}, \overline{CS} = V_{IL}, f = f_{MAX}, \text{Outputs Open}$	—	1360	mA
$I_{SB}$	Standby Supply Current	$V_{CC} = \text{Max.}, \overline{CS} \geq V_{IH}, f = f_{MAX}, \text{Outputs Open}$	—	480	mA
$I_{SB1}$	Full Standby Supply Current	$\overline{CS} \geq V_{CC} - 0.2V, f = 0$ $V_{IN} > V_{CC} - 0.2V \text{ or } < 0.2V$	—	120	mA

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## AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

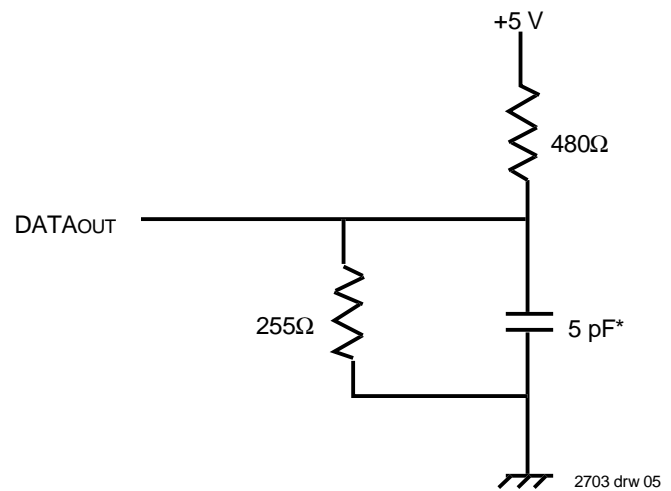
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Figure 1. Output Load

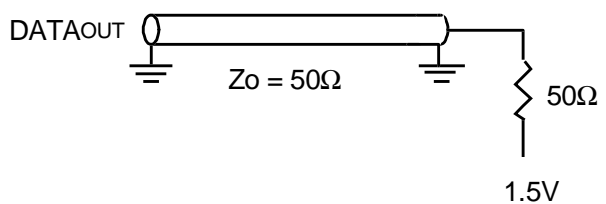
\*Includes scope and jig.



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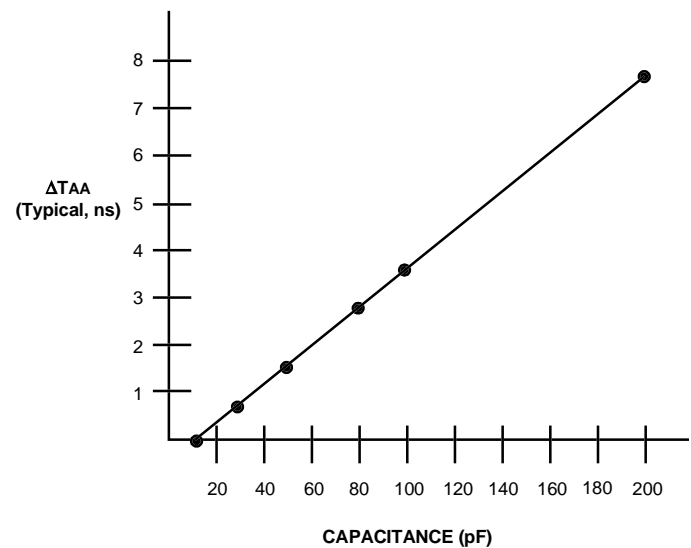
Figure 2. Output Load

(for tOLZ, tOHZ, tCHZ, tCLZ, tWHZ, tOW)



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Figure 3. Alternate Output Load



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Figure 4. Alternate Lumped Capacitive Load, Typical Derating

## AC Electrical Characteristics

(V<sub>CC</sub> = 5V ±10%, T<sub>A</sub> = 0°C to +70°C)

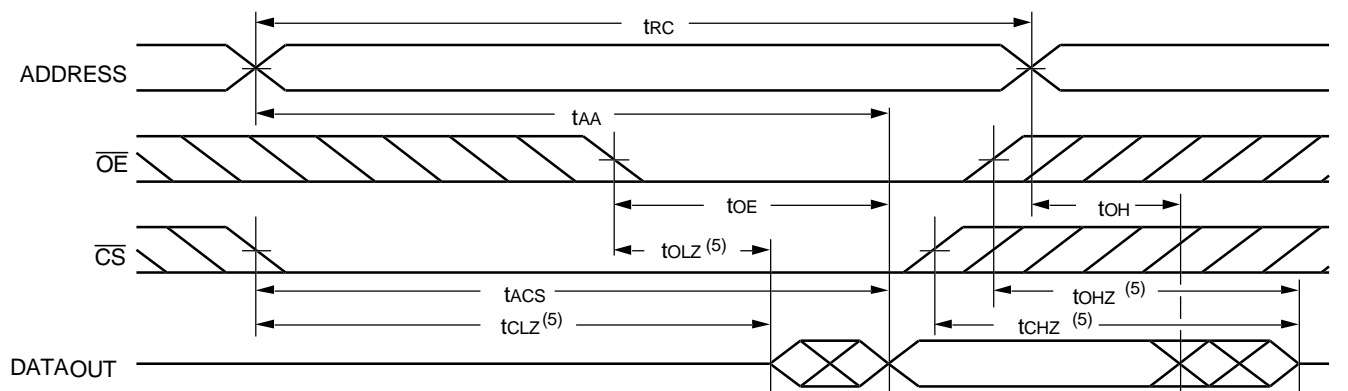
Symbol	Parameter	7MP4045SxxZ, 7MP4045/4145SxxM						Unit
		-15		-20		-25		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t <sub>RC</sub>	Read Cycle Time	15	—	20	—	25	—	ns
t <sub>AA</sub>	Address Access Time	—	15	—	20	—	25	ns
t <sub>ACS</sub>	Chip Select Access Time	—	15	—	20	—	25	ns
t <sub>CLZ</sub> <sup>(1)</sup>	Chip Select to Output in Low-Z	3	—	5	—	5	—	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	8	—	10	—	12	ns
t <sub>OLZ</sub> <sup>(1)</sup>	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t <sub>CHZ</sub> <sup>(1)</sup>	Chip Deselect to Output in High-Z	—	8	—	10	—	12	ns
t <sub>OHZ</sub> <sup>(1)</sup>	Output Disable to Output in High-Z	—	8	—	10	—	10	ns
t <sub>OH</sub>	Output Hold from Address Change	3	—	3	—	3	—	ns
t <sub>PU</sub> <sup>(1)</sup>	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t <sub>PD</sub> <sup>(1)</sup>	Chip Deselect to Power-Down Time	—	15	—	20	—	25	ns
Write Cycle								
t <sub>WC</sub>	Write Cycle Time	15	—	20	—	25	—	ns
t <sub>CW</sub>	Chip Select to End-of-Write	12	—	15	—	20	—	ns
t <sub>AW</sub>	Address Valid to End-of-Write	12	—	15	—	20	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	12	—	15	—	20	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	ns
t <sub>WHZ</sub> <sup>(1)</sup>	Write Enable to Output in High-Z	—	8	—	13	—	15	ns
t <sub>DW</sub>	Data to Write Time Overlap	10	—	12	—	15	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	ns
t <sub>OW</sub> <sup>(1)</sup>	Output Active from End-of-Write	0	—	0	—	0	—	ns

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**NOTE:**

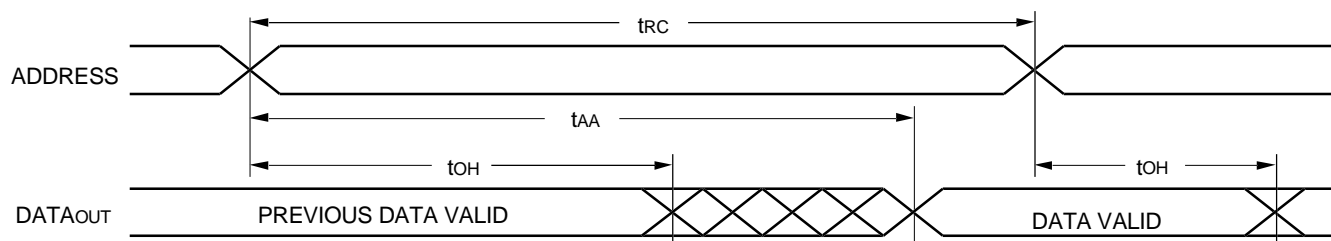
1. This parameter is guaranteed by design but not tested.

## Timing Waveform of Read Cycle No. 1<sup>(1)</sup>



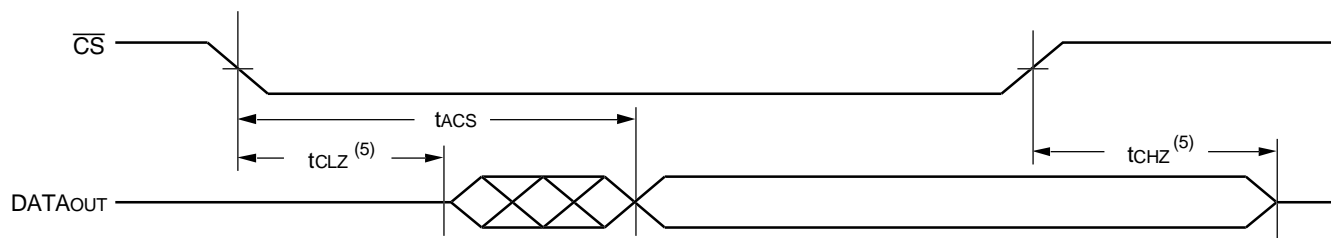
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## Timing Waveform of Read Cycle No. 2<sup>(1,2,4)</sup>



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## Timing Waveform of Read Cycle No. 3<sup>(1,3,4)</sup>

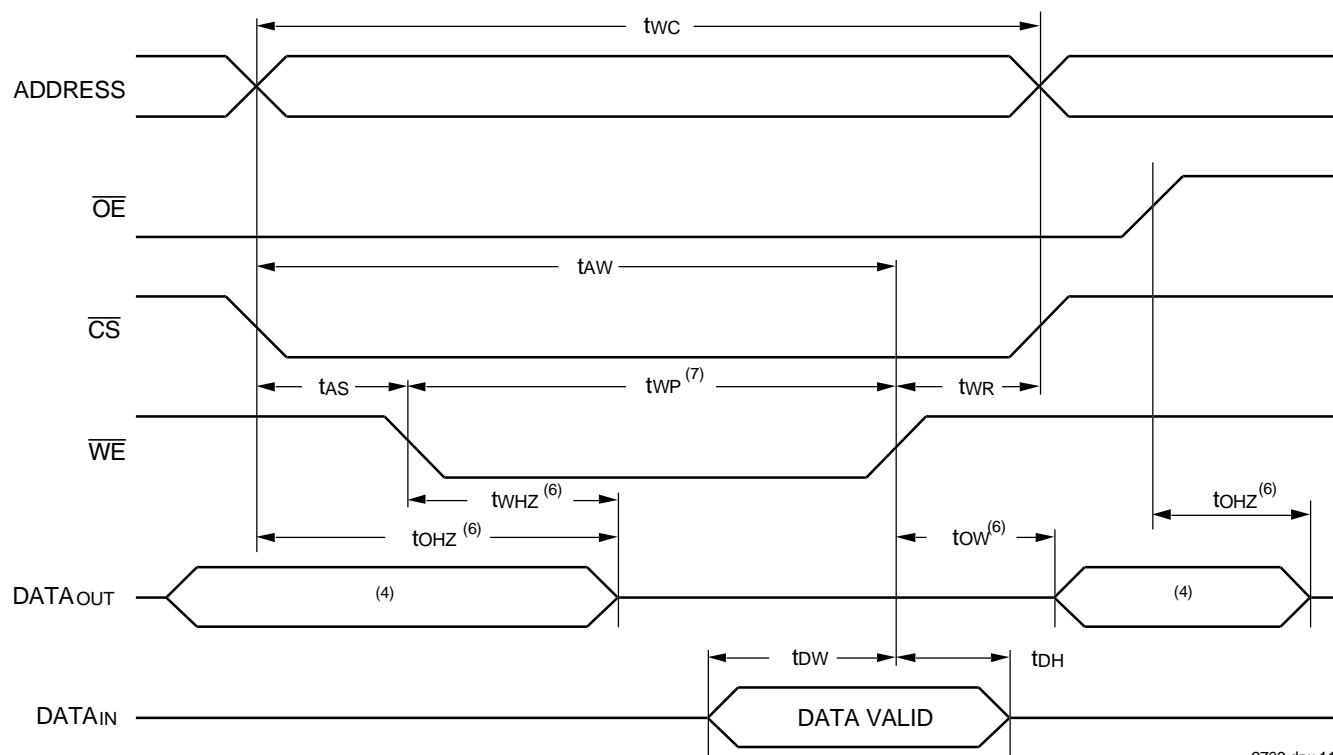


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### NOTES:

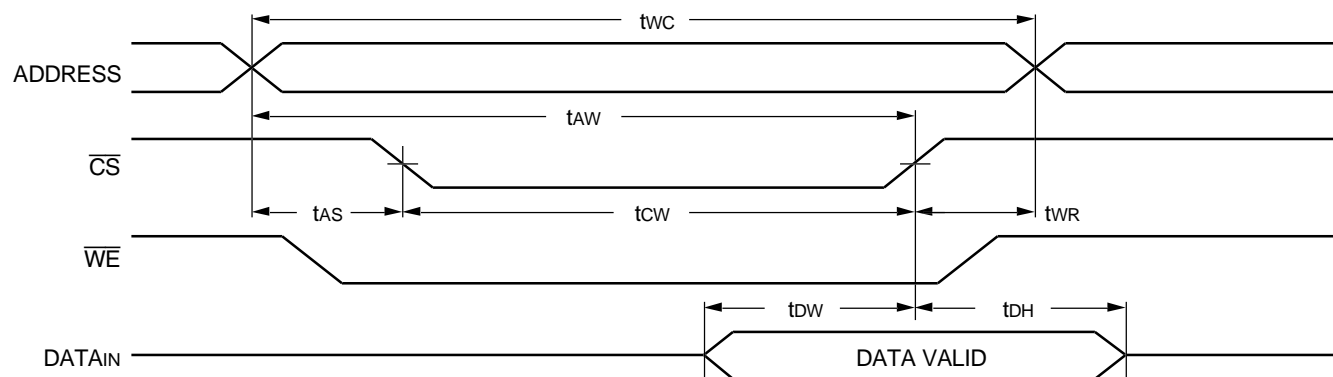
1.  $\overline{WE}$  is HIGH for Read Cycle.
2. Device is continuously selected.  $\overline{CS} = V_{IL}$ .
3. Address valid prior to or coincident with  $\overline{CS}$  transition LOW.
4.  $\overline{OE} = V_{IL}$ .
5. Transition is measured  $\pm 200\text{mV}$  from steady state. This parameter is guaranteed by design, but not tested.

## Timing Waveform of Write Cycle No. 1 ( $\overline{WE}$ Controlled) (1,2,3,7)



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## Timing Waveform of Write Cycle No. 2 ( $\overline{CS}$ Controlled) (1,2,3,5)



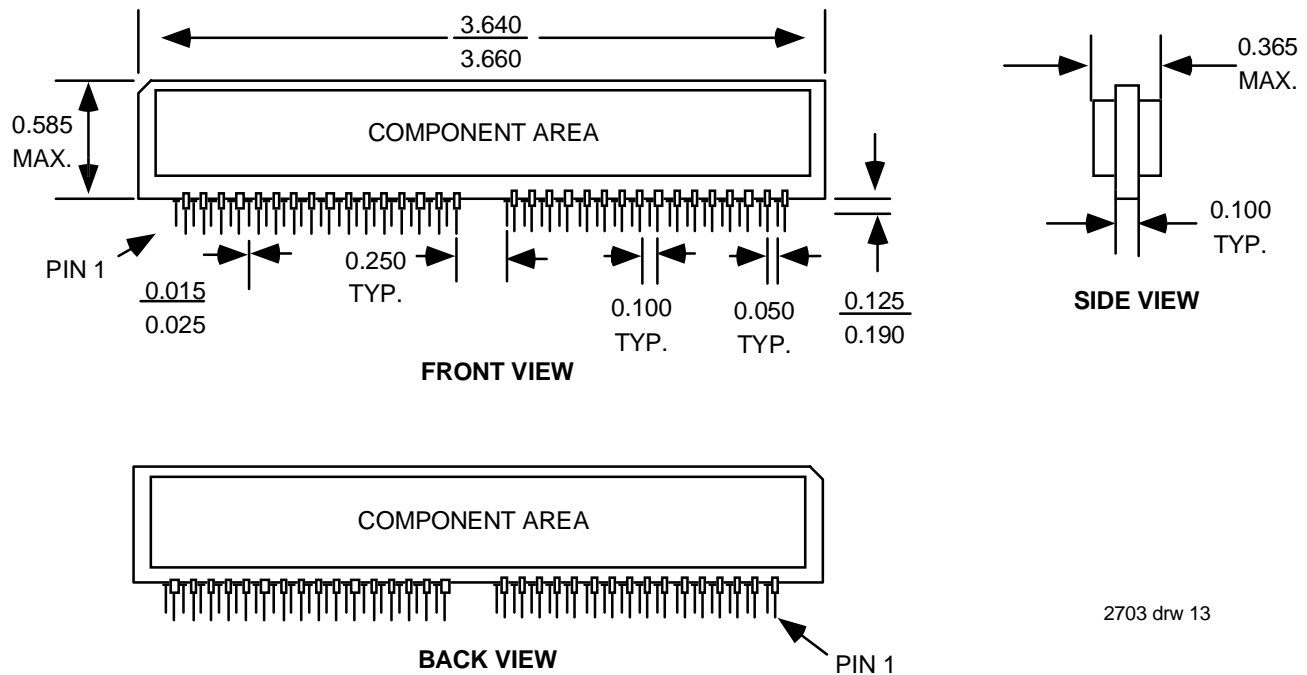
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### NOTES:

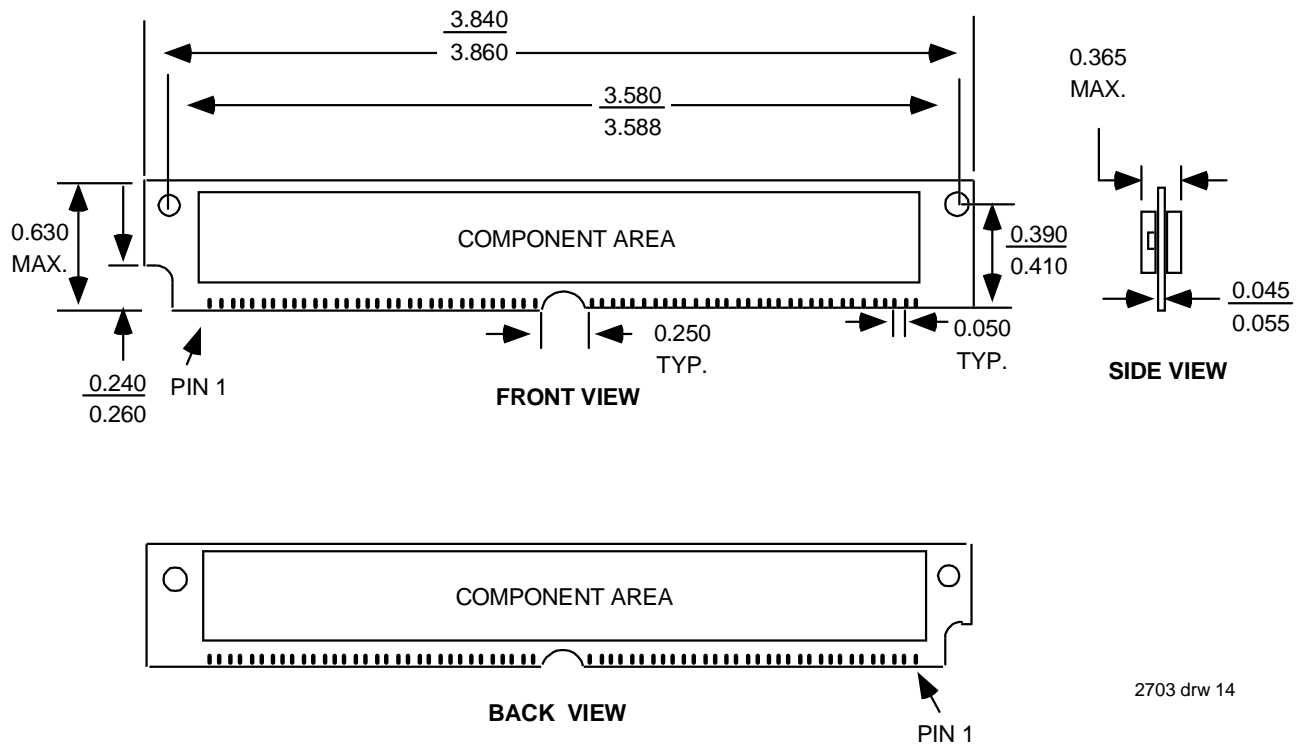
1.  $\overline{WE}$  or  $\overline{CS}$  must be HIGH during all address transitions.
2. A write occurs during the overlap ( $t_{WP}$ ) of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured  $\pm 200\text{mV}$  from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If  $\overline{OE}$  is LOW during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or ( $t_{WHZ} + t_{OW}$ ) to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{OW}$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .

## Package Dimensions

### 7MP4045 ZIP VERSION

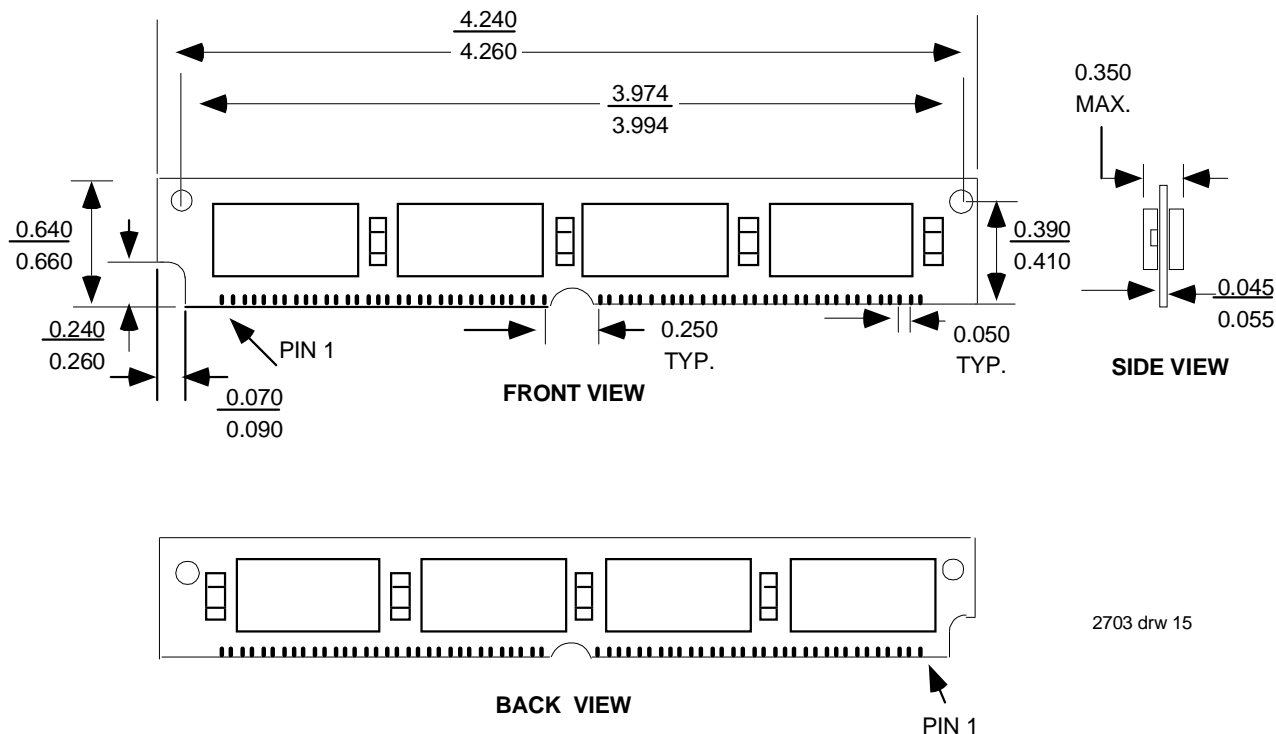


### 7MP4045 SIMM VERSION





## 7MP4145 SIMM VERSION



## Ordering Information

IDT	XXXXX	X	X	X	X	
	Device Type	Power	Speed	Package	Process/ Temperature Range	
					Blank	Commercial (0°C to +70°C)
					Z	FR-4 ZIP (Zig-Zag In-line vertical Package, 4045 only)
					M	FR-4 SIMM (Single In-line Memory Module)
			15			} Speed in Nanoseconds
			20			
			25			
					S	Standard Power
					7MP4045	256K x 32 Static RAM Module
					7MP4145	256K x 32 Static RAM Module

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