



Integrated Device Technology, Inc.

256KB AND 512KB SECONDARY CACHE MODULES FOR THE PowerPC™

**IDT7MPV6253
IDT7MPV6255/56**

FEATURES

- For CHRP based PowerPC™ systems.
- Asynchronous and pipelined burst SRAM options in the same module pinout
- Low-cost, low-profile card edge module with 178 leads
- Uses Burndy Computerbus™ connector, part number ELF182KSC-3Z50
- Operates with external PowerPC CPU speeds up to 66MHz
- Separate 5V ($\pm 5\%$) and 3.3V ($+10\%/ -5\%$) power supplies
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Presence Detect output pins allow the system to determine the particular cache configuration.

x 8 asynchronous static RAMs and the IDT7MPV6255/56 use IDT's 71V432 32K x 32 pipelined synchronous burst static RAMs in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board. In addition, each of the modules uses the IDT 71216 16K x 15 Cache-Tag static RAM and IDT FCT logic. Extremely high speeds are achieved using IDT's high-reliability, low cost CMOS technology.

The low profile card edge package allows 178 signal leads to be placed on a package 5.06" long, a maximum of 0.250" thick and a maximum of 1.08" tall. The module space savings versus discrete components allows the OEM to design additional functions onto the system or to shrink the size of the motherboard for reduced cost.

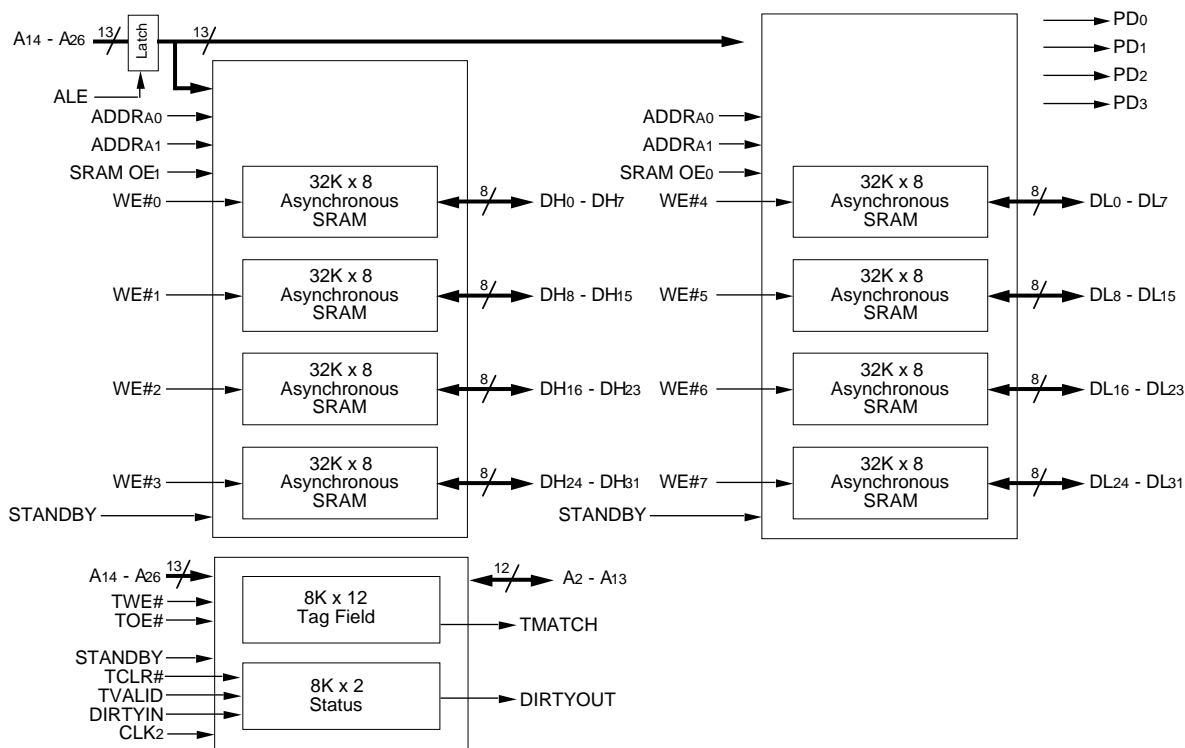
All inputs and outputs are LVTTTL-compatible, and operate from separate 5V ($\pm 5\%$) and 3.3V ($+10\%/ -5\%$) power supplies. Multiple GND pins and on-board decoupling capacitors ensure maximum protection from noise.

DESCRIPTION

The IDT7MPV6253/55/56 modules belong to a family of secondary caches intended for use with PowerPC CPU-based systems. The IDT7MPV6253 uses IDT's 71V256 32K

FUNCTIONAL BLOCK DIAGRAM

IDT7MPV6253 – 256KB ASYNCHRONOUS VERSION



drw 01

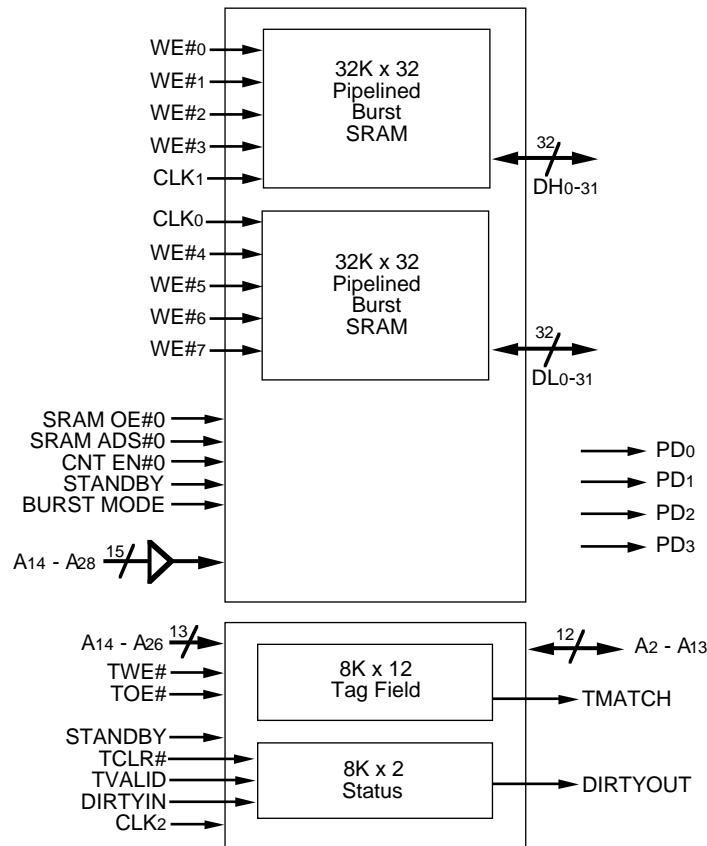
The IDT logo is a registered trademark of Integrated Device Technology, Inc. PowerPC is a trademark of IBM. Computerbus is trademark of Burndy.

COMMERCIAL TEMPERATURE RANGE

JUNE 1996

FUNCTIONAL BLOCK DIAGRAM

IDT7MPV6255 – 256KB PIPELINED BURST VERSION



drw 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC3	Supply Voltage	3.14	3.3	3.6	V
VCC5	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
V _{IH}	Input High Voltage	2.2	—	VCC + 0.3	V
V _{IL}	Input Low Voltage	−0.5 ⁽¹⁾	—	0.8	V

NOTE:

1. V_{IL} = −1.0V for pulse width less than 5ns, once per cycle.

tbl 01

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Power Plane	Ambient Temperature	GND	Vcc
VCC3	0°C to +70°C	0V	3.3V +10/-5%
VCC5	0°C to +70°C	0V	5.0V ± 5%

tbl 02

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V _{TERM} for VCC3	Terminal Voltage with Respect to GND	−0.5 to +4.6	V
T _A	Operating Temperature	0 to +70	°C
T _{BIAS}	Temperature Under Bias	−10 to +85	°C
T _{STG}	Storage Temperature	−55 to +125	°C
I _{OUT}	DC Output Current	50	mA

NOTE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

tbl 03

SRAM ACCESS TIMES

Module Speed	Asych	Burst ⁽¹⁾	Tag
66MHz	15ns	8.5ns	10ns

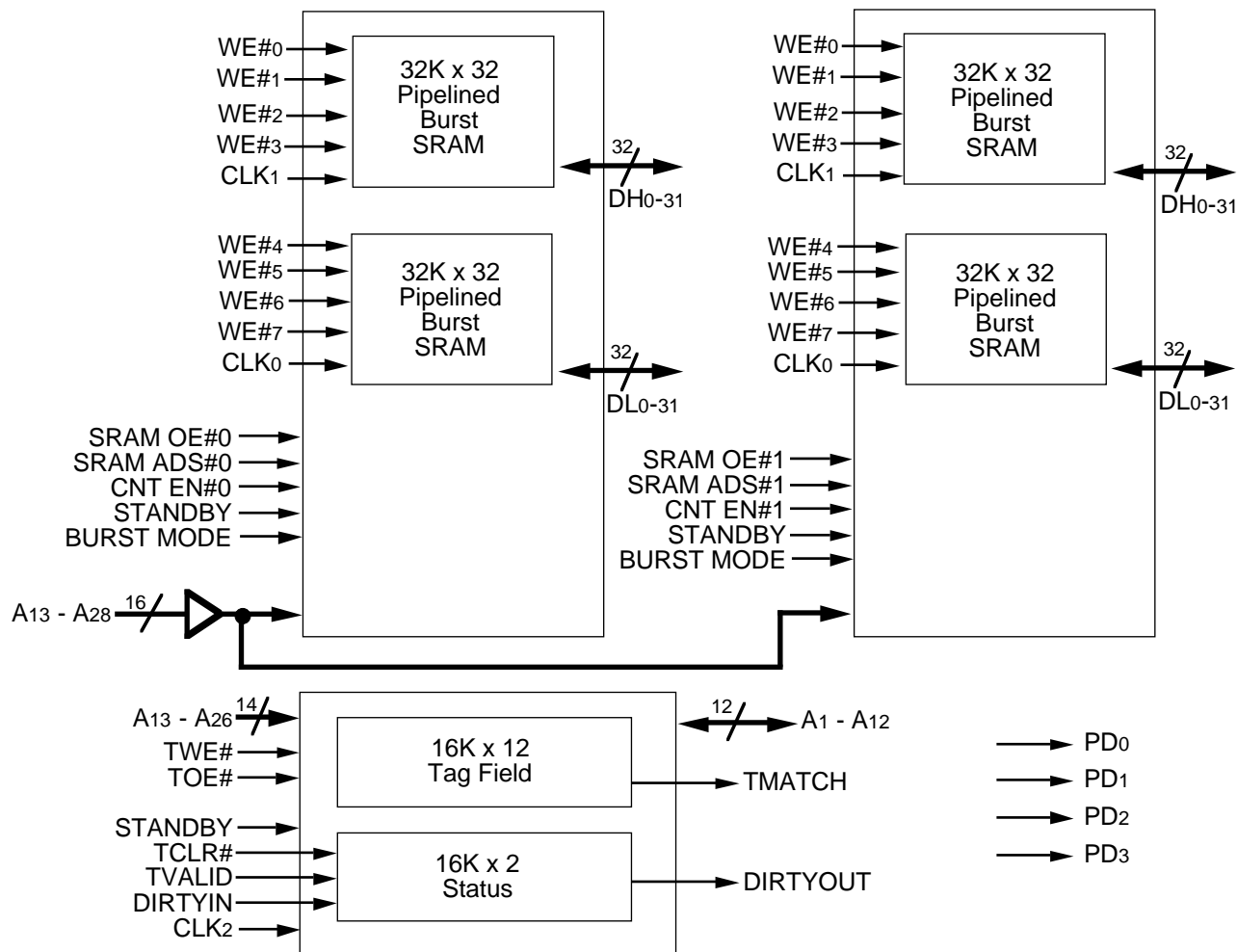
NOTE:

1. Burst SRAMs are measured by Clock to Data Out (t_{CD}).

tbl 04

FUNCTIONAL BLOCK DIAGRAM

IDT7MPV6256 – 512KB PIPELINED BURST VERSION



drw 03

CAPACITANCE (IDT7MPV6253)⁽¹⁾

(TA = +25°C, f = 1.0 MHz)

Symbol	Parameter ⁽¹⁾	Condition	Max.	Unit
CIN1	Input Capacitance (Address)	VIN = 0V	15	pF
CIN2	Input Capacitance (ADDR0-1)	VIN = 0V	25	pF
CIN3	Input Capacitance (OE#)	VIN = 0V	45	pF
CIN4	Input Capacitance (WE#, TWE#)	VIN = 0V	8	pF
C/I/O	I/O Capacitance	VOU = 0V	10	pF

NOTES:

1. These parameters are guaranteed by design but not tested.

tbl 05

CAPACITANCE (IDT7MPV6255/56)⁽¹⁾

(TA = +25°C, f = 1.0 MHz)

Symbol	Parameter ⁽¹⁾	Condition	Max.	Unit
CIN1	Input Capacitance (Address)	VIN = 0V	20	pF
CIN2	Input Capacitance (ADDR0-1)	VIN = 0V	—	pF
CIN3	Input Capacitance (OE#)	VIN = 0V	15	pF
CIN4	Input Capacitance (WE#, TWE#)	VIN = 0V	8	pF
C/I/O	I/O Capacitance	VOU = 0V	10/20	pF

NOTES:

1. These parameters are guaranteed by design but not tested.

tbl 06

PIN CONFIGURATION⁽¹⁾

GND	90	1	GND
PD ₁	91	2	PD ₀
PD ₃	92	3	PD ₂
DH ₃₁	93	4	DH ₃₀
DH ₂₉	94	5	DH ₂₈
DH ₂₇	95	6	DH ₂₆
DH ₂₅	96	7	DH ₂₄
VCC ₃	97	8	VCC ₃ ⁽¹⁾
SRAM WE ₃	98	9	DP ₃ ⁽¹⁾
DH ₂₃	99	10	DH ₂₂
DH ₂₁	100	11	DH ₂₀
DH ₁₈	101	12	DH ₁₉
GND	102	13	GND
DH ₁₆	103	14	DH ₁₇
SRAM WE ₂	104	15	DP ₂ ⁽¹⁾
DH ₁₄	105	16	DH ₁₅
DH ₁₃	106	17	DH ₁₂
VCC ₅	107	18	VCC ₅
DH ₁₀	108	19	DH ₁₁
DH ₈	109	20	DH ₉
SRAM WE ₁	110	21	DP ₁ ⁽¹⁾
DH ₆	111	22	DH ₇
VCC ₃	112	23	VCC ₃
DH ₄	113	24	DH ₅
GND	114	25	DH ₃
CLK ₀	115	26	DH ₂
GND	116	27	DH ₀
DH ₁	117	28	DP ₀ ⁽¹⁾
SRAM WE ₀	118	29	GND
DL ₃₁	119	30	CLK ₁
DL ₃₀	120	31	GND
GND	121	32	DL ₂₈
DL ₂₉	122	33	DL ₂₆
DL ₂₇	123	34	DL ₂₄
DL ₂₅	124	35	DP ₇ ⁽¹⁾
VCC ₅	125	36	VCC ₅
SRAM WE ₇	126	37	DL ₂₂
DL ₂₃	127	38	DL ₂₀
DL ₂₁	128	39	DL ₁₈
DL ₁₉	129	40	DL ₁₆
GND	130	41	GND
DL ₁₇	131	42	DP ₆ ⁽¹⁾
SRAM WE ₆	132	43	DL ₁₄
DL ₁₅	133	44	DL ₁₂
DL ₁₃	134	45	DL ₁₁
GND	135	46	GND
DL ₁₀	136	47	DL ₉
DL ₈	137	48	DP ₅ ⁽¹⁾
SRAM WE ₅	138	49	DL ₇
DL ₆	139	50	DL ₄
VCC ₃	140	51	VCC ₃
DL ₅	141	52	DL ₃
DL ₂	142	53	DL ₁
GND	143	54	DL ₀
⁽¹⁾ CLK ₃	144	55	GND
GND	145	56	CLK ₂ (TAG)
⁽¹⁾ CLK ₄	146	57	GND
GND	147	58	DP ₄ ⁽¹⁾
SRAM WE ₄	148	59	SRAM OE ₀
^(3,4) SRAM ALE	149	60	SRAM OE ₁ ⁽³⁾
VCC ₃	150	61	VCC ₃
^(3,4) ADDR ₁	151	62	ADDR ₀ ^(3,4)
⁽¹⁾ RSVD	152	63	RSVD ⁽¹⁾
⁽²⁾ SRAM CNT EN ₀	153	64	SRAM ADS ₀ ⁽²⁾
^(2,3) SRAM CNT EN ₁	154	65	SRAM ADS ₁ ^(2,3)
A ₂₇	155	66	A ₂₈
A ₂₄	156	67	A ₂₆
A ₂₂	167	68	A ₂₅
A ₂₀	158	69	A ₂₃
GND	159	70	GND
A ₁₈	160	71	A ₂₁
A ₁₆	161	72	A ₁₉
A ₁₅	162	73	A ₁₇
A ₁₄	163	74	A ₁₃
VCC ₃	164	75	VCC ₃
A ₁₀	165	76	A ₁₂
A ₈	166	77	A ₁₁
A ₆	167	78	A ₉
GND	168	79	GND
A ₄	169	80	A ₇
A ₂	170	81	A ₅
^(2,3) A ₁	171	82	A ₃
BURST MODE	172	83	A ₀ ⁽¹⁾
VCC ₅	173	84	VCC ₅
TAG VALID	174	85	TAG CLR
TAG WE	175	86	TAG MATCH
STANDBY	176	87	TAG OE
DIRTYOUT	177	88	DIRTYIN
GND	178	89	GND

PIN NAMES

A ₀ – A ₂₈	Address Inputs
ADDR ₀ - ADDR ₁	Address Inputs (Asynchronous SRAMs only)
CLK ₀ - CLK ₄	Clock Inputs
DH ₀ - DH ₃₁	High Order Cache Data
DL ₀ - DL ₃₁	Low Order Cache Data
PD ₀ – PD ₃	Presence Detect Pins
SRAM ADS ₀ - SRAM ADS ₁	SRAM Address Strobe
SRAM ALE	SRAM Address Latch Enable
SRAM CNT EN ₀ - SRAM CNT EN ₁	SRAM Control Enable
SRAM OE ₀ - SRAM OE ₁	SRAM Output Enable
SRAM WE ₀ - SRAM WE ₁	SRAM Write Enable
BURST MODE	Burst Mode: 0=Linear, 1=Interleaved
TAG CLR	Tag Clear
TAG MATCH	Tag Match
TAG VALID	Tag Valid
TAG OE	Tag Output Enable
TAG WE	Tag Write Enable
DIRTYIN	Dirty Input Bit
DIRTYOUT	Dirty Output Bit
STANDBY	Stand By Mode
VCC ₃	3.3 Volt Power Supply
VCC ₅	5 Volt Power Supply
GND	Ground
NC	No Connect
RSVD	Reserved

tbl 07

PRESENCE DETECT TABLE

PD ₃	PD ₂	PD ₁	PD ₀	Module
NC	NC	NC	NC	No cache present
NC	GND	GND	GND	IDT7MPV6253
GND	GND	NC	NC	IDT7MPV6255
GND	NC	NC	NC	IDT7MPV6256

tbl 08

NOTES:

- These pins are NC (No Connect) on 7MPV6253/55/56.
- These pins are NC on 7MPV6253.
- These pins are NC on 7MPV5255.
- These pins are NC on 7MPV6256.

LOW PROFILE CARD EDGE MODULE TOP VIEW

drw 04

DC ELECTRICAL CHARACTERISTICS

($V_{CC5} = 5.0V \pm 5\%$, $V_{CC3} = 3.3V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$)

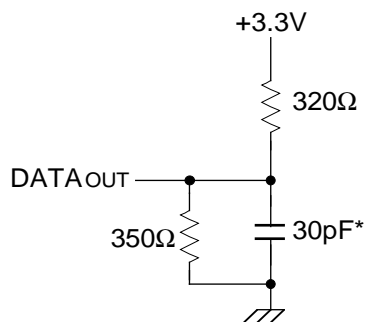
Symbol	Parameter	Test Condition	Min.	'53	'55	'56	Unit
				Max.	Max.	Max.	
I _{LI}	Input Leakage Current (Address)	$V_{CC5} = \text{Max}$, $V_{IN} = \text{GND to } V_{CC}$ $V_{CC3} = \text{Max}$	—	20	30	50	μA
I _{LI}	Input Leakage Current (Data and Control)	$V_{CC5} = \text{Max}$, $V_{IN} = \text{GND to } V_{CC}$ $V_{CC3} = \text{Max}$	—	10	10	20	μA
I _{LO}	Output Leakage Current	$V_{OUT} = 0V$ to V_{CC3} , $V_{CC3} = \text{Max}$.	—	10	10	20	μA
V _{OL}	Output Low Voltage	$I_{OL} = 8mA$, $V_{CC3} = \text{Min}$.	—	0.4	0.4	0.4	V
V _{OH}	Output High Voltage	$I_{OH} = -4mA$, $V_{CC3} = \text{Min}$.	2.4	—	—	—	V
I _{CC3}	Operating 3.3V Power Supply Current	$V_{CC3} = \text{Max}$., $\text{STANDBY} \leq V_{IL}$, $f = f_{MAX}$, Outputs Open	—	1000	500	590	mA
I _{CC5}	Operating 5V Power Supply Current	$V_{CC5} = \text{Max}$., $\text{STANDBY} \leq V_{IL}$, $f = f_{MAX}$, Outputs Open	—	290	290	290	mA
I _{SB3}	Standby 3.3V Power Supply Current	$V_{CC3} = \text{Max}$., $\text{STANDBY} \geq V_{IH}$, $f = f_{MAX}$, Outputs Open	—	100	100	190	mA
I _{SB31}	Full Standby 3.3V Power Supply Current	$V_{CC3} = \text{Max}$., $\text{STANDBY} \geq V_{CC3} - 0.2V$, $f = 0$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC3} - 0.2V$, Outputs Open	—	30	30	50	mA
I _{SB5}	Standby 5V Power Supply Current	$V_{CC5} = \text{Max}$., $\text{STANDBY} \geq V_{IH}$ $f = f_{MAX}$, Outputs Open	—	30	30	30	mA

tbl 09

AC TEST CONDITIONS – 3.3V POWER SUPPLY

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

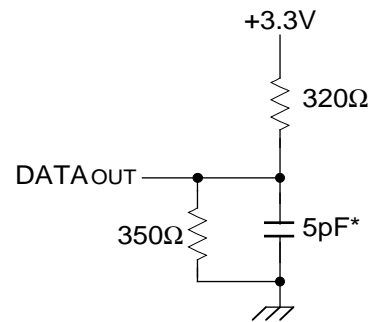
tbl 10



*including scope and jig capacitances

Figure 1. Output Load

drw 05

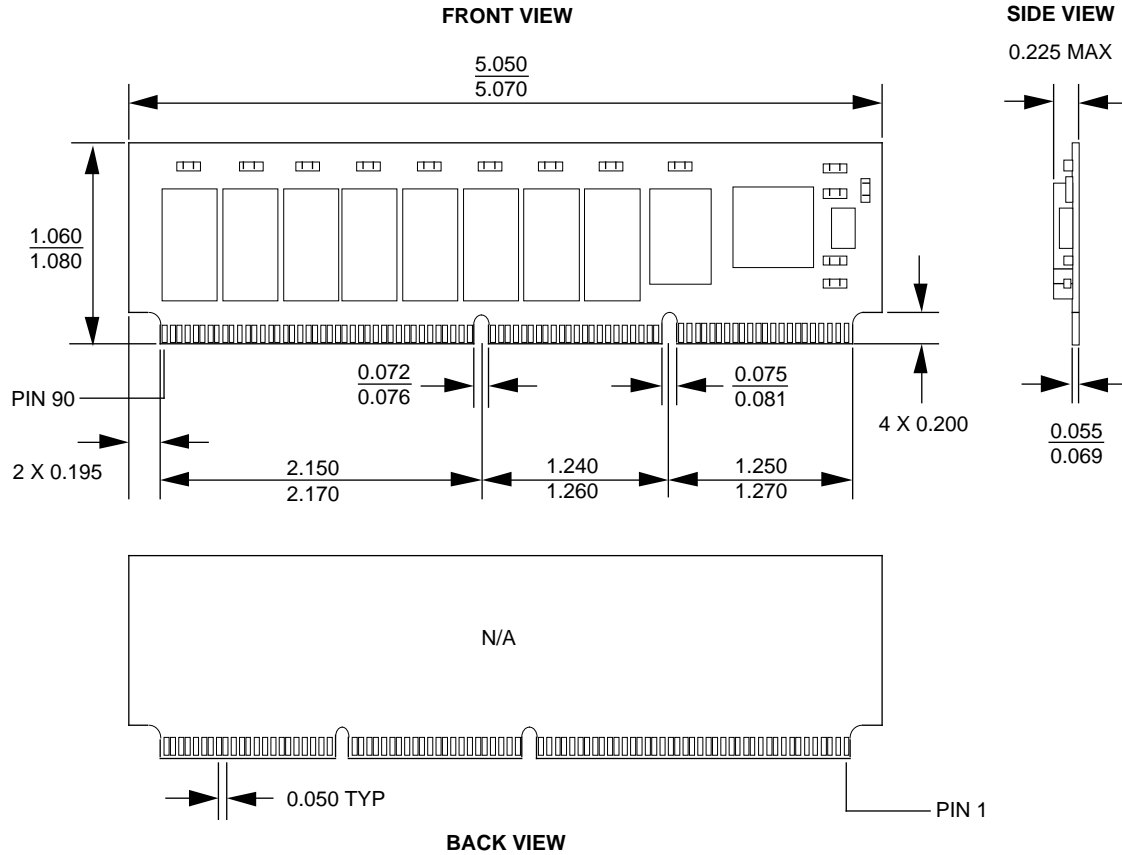


*including scope and jig capacitances

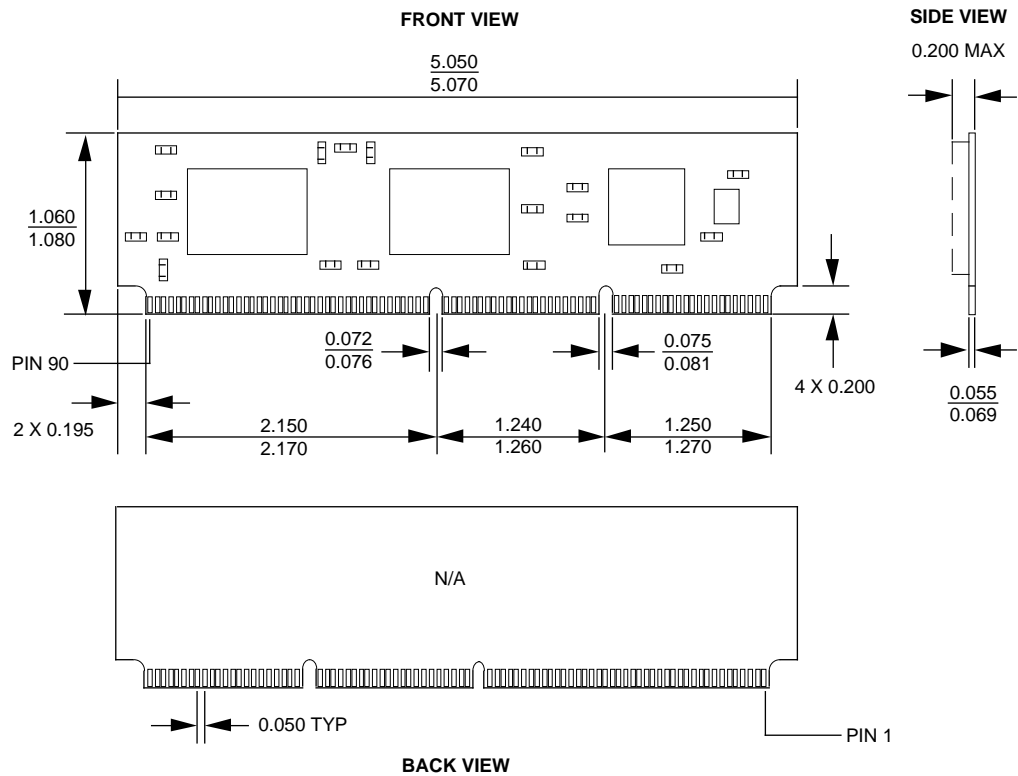
Figure 2. Output Load
(for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

drw 06

PACKAGE DIMENSIONS - IDT7MPV6253



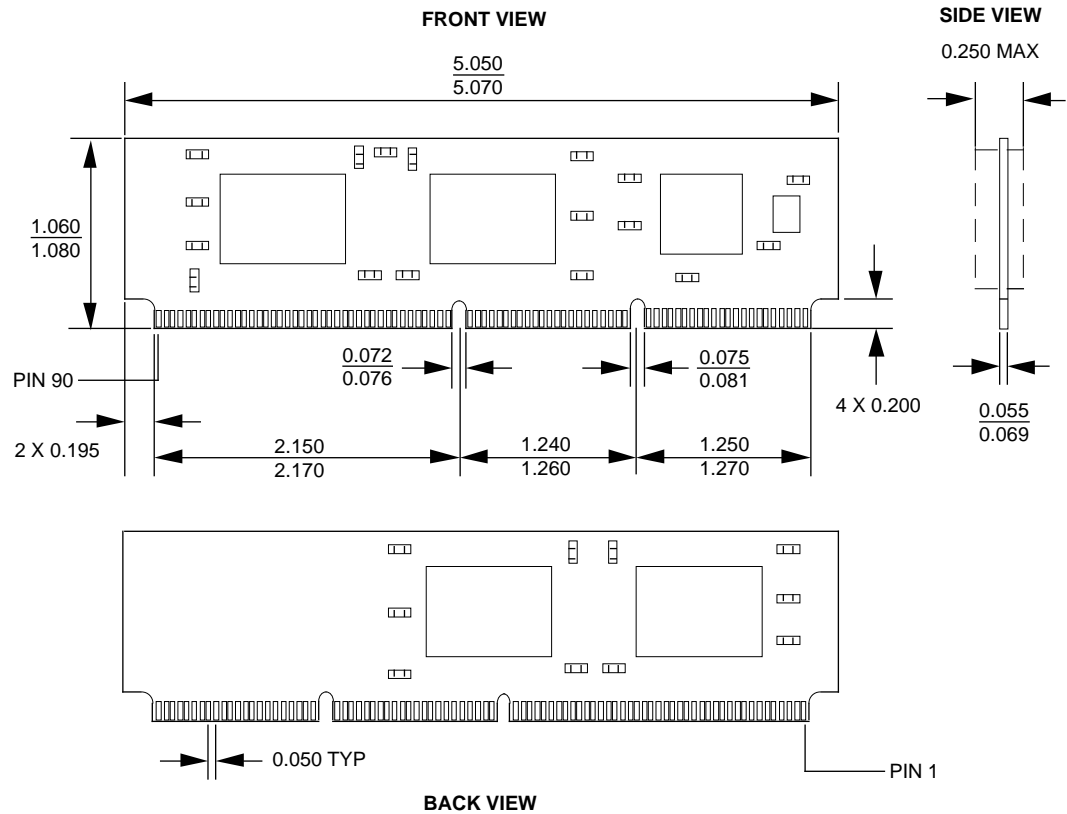
IDT7MPV6255



drw 07

drw 08

PACKAGE DIMENSIONS - IDT7MPV6256



drw 09

ORDERING INFORMATION

IDT	XXXXX Device Type	A Power	999 Speed	A Package	A Process/ Temperature Range	
					Blank	Commercial (0°C to +70°C)
					M	178 lead Module, Card Edge Low Profile (CELP)
			15 66			Speed in Nanoseconds (Asynchronous) Speed in Megahertz (Pipelined Burst)
		S				Standard Power
					7MPV6253	256KB Asynchronous Cache Module
					7MPV6255	256KB Pipelined Burst Cache Module
					7MPV6256	512KB Pipelined Burst Cache Module

drw 10