



GUARANTEED LOW SKEW CMOS CLOCK DRIVER/BUFFER

QS5805/A/B

FEATURES:

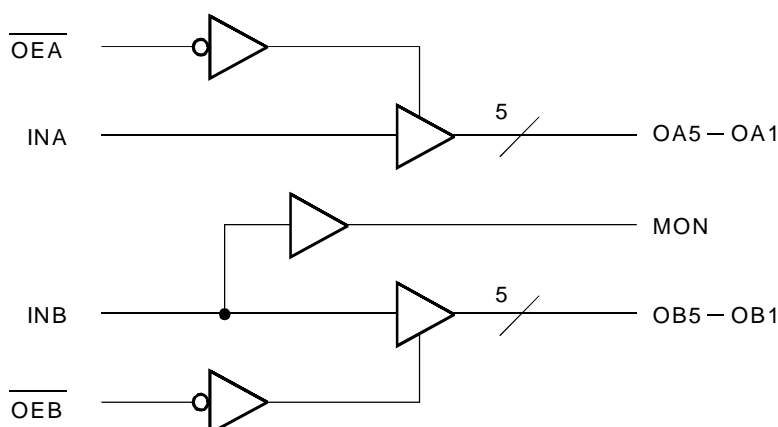
- 10 CMOS outputs
- Monitor output
- Rail-to-rail output voltage swing
- Input hysteresis for better noise margin
- Guaranteed low skew:
 - 0.7ns output skew (same bank)
 - 0.8ns output skew (different banks)
 - 1.2ns part-to-part skew
- Std., A, and B speed grades
- Available in QSOP and SOIC packages

DESCRIPTION

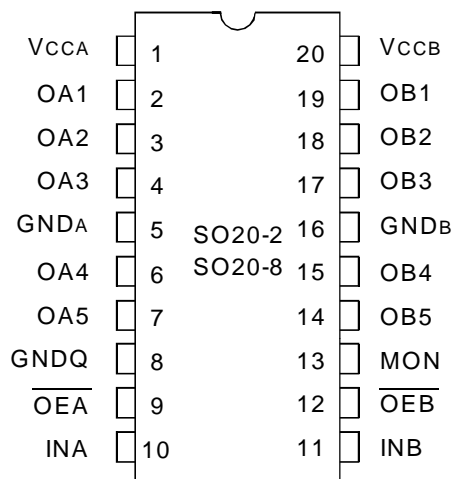
The QS5805 clock buffer/driver circuits can be used for clock buffering schemes where low skew is a key parameter. This device offers two banks of five non-inverting outputs. The QS5805 device provides low propagation delay buffering with on-chip skew of 0.7ns for same-transition, same-bank signals.

The QS5805 is characterized for operation at -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP/ SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Supply Voltage to Ground	- 0.5 to +7	V
	DC Output Voltage V _{OUT}	- 0.5 to +7	V
V _{TERM} ⁽³⁾	DC Input Voltage V _{IN}	- 0.5 to +7	V
V _{AC}	AC Input Voltage (pulse width ≤20ns)	-3	V
I _{OUT}	DC Output Current V _{IN} < 0	-20	mA
	DC Output Current Max. Sink Current/Pin	120	mA
T _{STG}	Storage Temperature	- 65 to +150	°C
T _J	Junction Temperature	150	°C

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{cc} Terminals.
- All terminals except V_{cc}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{IN} = 0V)

Pins	QSOP		SOIC		Unit
	Typ.	Max. ⁽¹⁾	Typ.	Max. ⁽¹⁾	
C _{IN}	4	6	5	7	pF
C _{OUT}	7	9	7	9	pF

NOTE:

- This parameter is guaranteed but not production tested.

PIN DESCRIPTION

Pin Names	I/O	Description
\overline{OEA} , \overline{OEB}	I	Output Enable Inputs
INA, INB	I	Clock Inputs
OAn, OBn	O	Clock Outputs
MON	O	Monitor Outputs (non-disable)

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$, $V_{HC} = V_{CC} - 0.2\text{V}$, $V_{LC} = 0.2\text{V}$

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for All Inputs	2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for All Inputs	—	—	0.8	V
V_{IC}	Clamp Diode Voltage ⁽³⁾	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OH} = -300\mu\text{A}$	V_{HC}	V_{CC}	—	V
		$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OH} = -15\text{mA}$	3.6	4.3	—	
		$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OH} = -24\text{mA}$	2.4	3.8	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OL} = 300\mu\text{A}$	—	GND	V_{LC}	V
		$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OL} = 64\text{mA}$	—	0.3	0.55	
I_{IN}	Input Leakage Current	$V_{CC} = \text{Max.}$, $V_{IN} = V_{CC}$ or GND	—	—	± 1	μA
I_{OZ}	Output Leakage Current	$V_{CC} = \text{Max.}$, $V_{OUT} = V_{CC}$ or GND	—	—	± 1	μA
I_{OFF}	Input Power Off Leakage	$V_{CC} = 0\text{V}$, $V_{IN} = V_{CC}$ or GND	—	—	± 1	μA
I_{OS}	Short Circuit Current ^(2,3)	$V_{CC} = \text{Max.}$, $V_{OUT} = \text{GND}$	-60	—	—	mA
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V

NOTES:

1. Typical values are at $V_{CC} = 5.0\text{V}$, $T_A = 25^{\circ}\text{C}$.
2. Not more than one output should be used to test this high power condition. Duration is less than one second.
3. Guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Typ. ⁽³⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}		0.005	0.5	mA
ΔI _{CC}	Supply Current per Input HIGH	V _{CC} = Max., V _{IN} = 3.4V		0.5	2.5	mA
I _{CCD}	Dynamic Power Supply Current per Output ⁽²⁾	V _{CC} = Max., $\overline{OE_A} = \overline{OE_B} = \text{GND}$ Outputs Enabled, 50% duty cycle		0.1	0.2	mA/MHz
I _C	Total Supply Current Examples ^(2,4)	V _{CC} = Max., $\overline{OE_A} = \overline{OE_B} = \text{GND}$ 50% duty cycle, f _i = 10MHz Five outputs toggling	V _{IN} = GND or V _{CC}	8.5	15.5	mA
			V _{IN} = GND or 3.4V	9	16.8	
		V _{CC} = Max., $\overline{OE_A} = \overline{OE_B} = \text{GND}$ 50% duty cycle, f _i = 2.5MHz All outputs toggling	V _{IN} = GND or V _{CC}	5	8.8	
			V _{IN} = GND or 3.4V	6	11.3	

NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Guaranteed by design but not tested. $C_L = 0\text{pF}$.
3. Typical values are for reference only. Conditions are $V_{CC} = 5.0\text{V}$, $T_A = 25^{\circ}\text{C}$.
4. $I_C = I_{CC} + (\Delta I_{CC})(D_H)(N_T) + I_{CCD}(f_o)(N_o)$
where:
 D_H = Input Duty Cycle
 N_T = Number of TTL HIGH inputs at D_H
 f_o = Output Frequency
 N_o = Number of outputs at f_o

SKEW CHARACTERISTICS OVER OPERATING RANGE

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

Symbol	Parameter ⁽¹⁾	QS5805		QS5805A		QS5805B		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tsk(01)	Skew between all outputs, same transition, same bank	—	0.7	—	0.7	—	0.7	ns
tsk(02)	Skew between outputs of all banks, same transition	—	0.8	—	0.8	—	0.8	ns
tsk(P)	Pulse Skew; skew between opposite transitions of the same output (tPHL - tPLH)	—	1	—	1	—	1	ns
tsk(T)	Part-to-part skew ⁽²⁾	—	1.5	—	1.5	—	1.2	ns

NOTES:

1. Skew parameters are guaranteed across temperature range, but not tested. Skew parameters are measured at 0.5Vcc.
2. tsk(T) only applies to devices of the same transition, part type, temperature, power supply voltage, loading, package, and speed grade.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

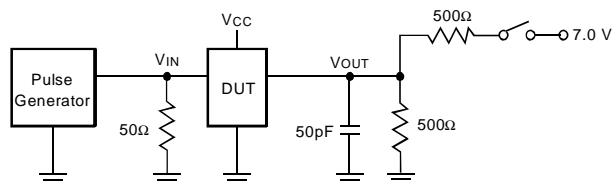
Symbol	Parameter ⁽¹⁾		QS5805		QS5805A		QS5805B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay ⁽²⁾ INA to OAn, INB to OBn		1.5	5.6	1.5	5.3	1.5	5	ns
tpZL tpZH	Output Enable Time		1.5	8	1.5	8	1.5	7	ns
tplZ tphZ	Output Disable Time		1.5	7	1.5	7	1.5	6	ns
tR	Output Rise Time	0.8V to 2V ⁽³⁾	—	1.5	—	1.5	—	1.5	ns
		0.2Vcc to 0.8Vcc	—	3	—	3	—	3	ns
tF	Output Fall Time	0.8V to 2V ⁽³⁾	—	1.5	—	1.5	—	1.5	ns
		0.2Vcc to 0.8Vcc	—	3	—	3	—	3	ns

NOTES:

1. Minimums guaranteed but not production tested. Timing parameters are measured at 0.5Vcc.
2. The propagation delay other range indicated by Min. and Max. specifications results from process and environmental variables. These propagation delays do not imply limit skew.
3. This parameter is guaranteed but not production tested.

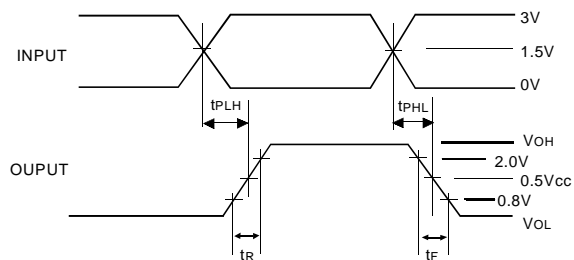
TEST CIRCUITS AND WAVEFORMS

Parameter Tested	Switch Position
t_{PLZ} , t_{PZL}	Closed
All Others	Open

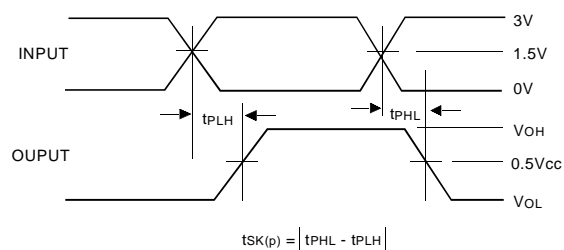


Pulse generator for all pulses: $f \leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$

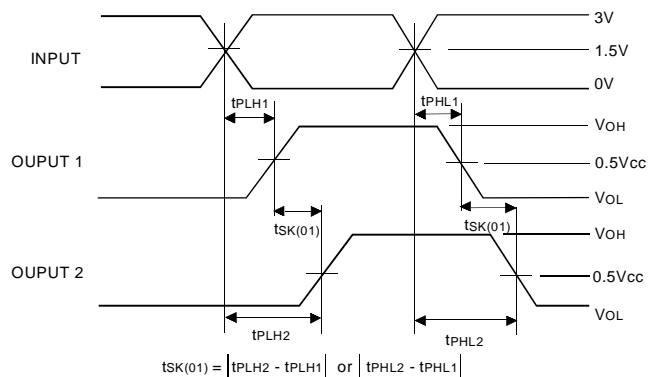
PROPAGATION DELAY



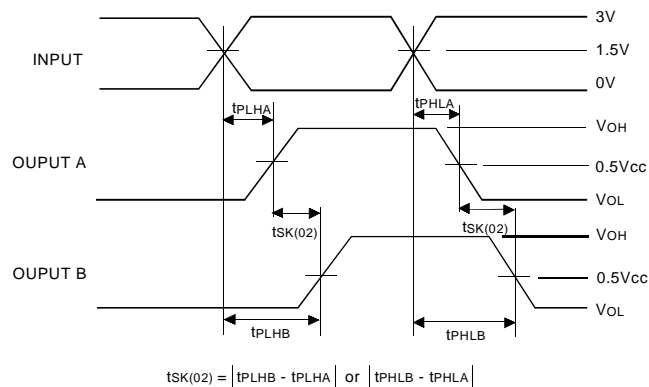
PULSE SKEW — $t_{sk}(P)$



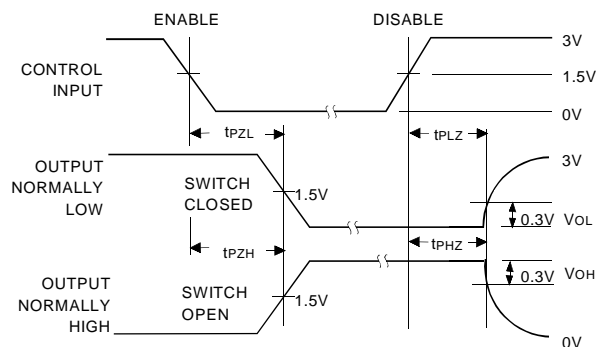
OUTPUT SKEW (SAME BANK) — $t_{sk}(01)$



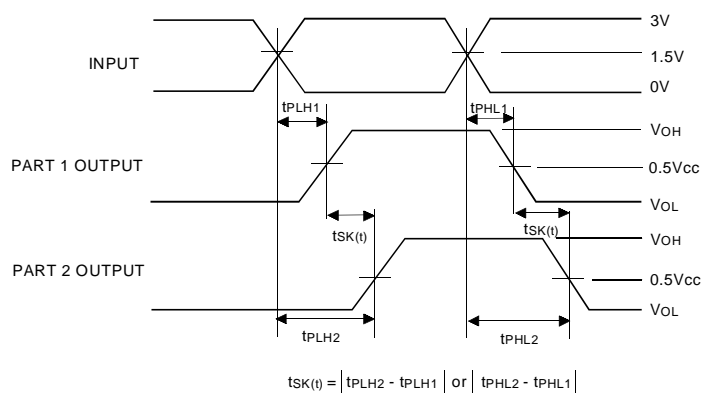
OUPUT SKEW (DIFFERENT BANKS) — $t_{sk}(02)$



ENABLE AND DISABLE TIMES



PART-TO-PART SKEW — $t_{sk}(I)$



QS XXXX XX
 Device Type Package

QS

XXXX

XX

Device Type

Package

Q

SO

Quarter Size Small Outline Pacakge (SO20-8)

Small Outline IC (SO20-2)

5805

5805A

5805B

Guaranteed Low Skew CMOS Clock Driver/Buffer



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