

Process C3017

CMOS 3 μ m

10 Volt Analog Mixed Mode

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	V_{T_N}	0.6	0.8	1.0	V	100x4 μ m
Body Factor	γ_N		0.6		$V^{1/2}$	100x4 μ m
Conduction Factor	β_N	42	47	52	$\mu A/V^2$	100x100 μ m
Effective Channel Length	L_{eff_N}	2.85	3.2	3.55	μ m	100x4 μ m
Width Encroachment	ΔW_N		0.7		μ m	Per side
Punch Through Voltage	$BVDSS_N$	12			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	12			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	V_{T_P}	-0.6	-0.8	-1.0	V	100x4 μ m
Body Factor	γ_P		0.55		$V^{1/2}$	100x4 μ m
Conduction Factor	β_P	13	15	19	$\mu A/V^2$	100x100 μ m
Effective Channel Length	L_{eff_P}	2.85	3.2	3.55	μ m	100x4 μ m
Width Encroachment	ΔW_P		0.9		μ m	Per side
Punch Through Voltage	$BVDSS_P$	-12			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	-12			V	

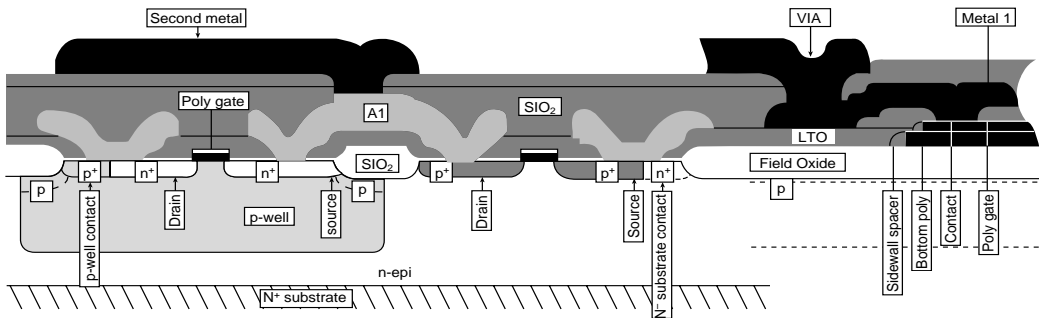
Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{P-well(f)}$	3.2	4.8	6.5	$K\Omega/\square$	P-well
N+ Sheet Resistance	ρ_{N+}	16	21	27	Ω/\square	
N+ Junction Depth	x_{jN+}		0.8		μ m	
P+ Sheet Resistance	ρ_{P+}	50	80	100	Ω/\square	
P+ Junction Depth	x_{jP+}		0.7		μ m	
Gate Oxide Thickness	T_{GOX}	44	48	52	nm	
Interpoly Oxide Thickness	T_{P1P2}		60		nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15	22	30	Ω/\square	
Bottom Poly Sheet Res.	ρ_{POLY2}	15	22	30	Ω/\square	
Metal-1 Sheet Resistance	ρ_{M1}		50		$m\Omega/\square$	
Metal-2 Sheet Resistance	ρ_{M2}		30		$m\Omega/\square$	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	0.66	0.72	0.78	fF/ μ m ²	
Metal-1 to Poly-1	C_{M1P}		0.0523		fF/ μ m ²	
Metal-1 to Silicon	C_{M1S}	0.26	0.30	0.34	fF/ μ m ²	
Metal-2 to Metal-1	C_{MM}	0.033	0.0384	0.041	fF/ μ m ²	
Poly-1 to Poly-2	C_{P1P2}	0.51	0.57	0.63	fF/ μ m ²	

Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	3.0 / 3.0 μ m
Starting Mat. Resistivity	15 - 25 Ω -cm	N+ To P+ Space	12 μ m
Typ. Operating Voltage	10V	Contact To Poly Space	2.5 μ m
Well Type	P-well	Contact Overlap Of Diffusion	1.5 μ m
Metal Layers	2	Contact Overlap Of Poly	1.0 μ m
Poly Layers	2	Metal-1 Overlap Of Contact	1.0 μ m
Contact Size	2.0x2.0 μ m	Metal-1 Overlap Of Via	1.75 μ m
Via Size	2.0x2.0 μ m	Metal-2 Overlap Of Via	1.5 μ m
Metal-1 Width/Space	3.5 / 2.5 μ m	Minimum Pad Opening	100x100 μ m
Metal-2 Width/Space	5.0 / 3.0 μ m	Minimum Pad-to-Pad Spacing	5.0 μ m
Gate Poly Width/Space	4.0 / 2.5 μ m	Minimum Pad Pitch	80.0 μ m

Special Feature of C3017 Process: P-well analog process with double metal CMOS 3.0 μ m technology.



Cross-sectional view of the C3017 process

