

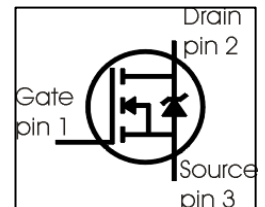
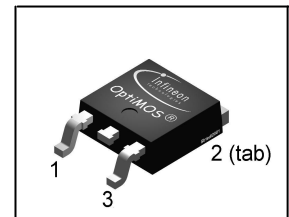
OptiMOS® Power-Transistor
Feature

- N-Channel
- Enhancement mode
- Logic Level
- High Current Rating
- Excellent Gate Charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- 175°C operating temperature
- Avalanche rated
- dv/dt rated

Product Summary

| | | |
|--------------|-----|----|
| V_{DS} | 30 | V |
| $R_{DS(on)}$ | 6.4 | mΩ |
| I_D | 50 | A |

P- TO252 -3-11



| Type | Package | Ordering Code | Marking |
|----------------|----------------|---------------|---------|
| SPD50N03S2L-06 | P- TO252 -3-11 | Q67042-S4084 | PN03L06 |

Maximum Ratings, at $T_j = 25^\circ\text{C}$, unless otherwise specified

| Parameter | Symbol | Value | Unit |
|--|----------------------|-------------|-------------------|
| Continuous drain current ¹⁾ $T_C=25^\circ\text{C}$ | I_D | 50 50 | A |
| Pulsed drain current $T_C=25^\circ\text{C}$ | $I_{D \text{ puls}}$ | 200 | |
| Avalanche energy, single pulse $I_D=50 \text{ A}$, $V_{DD}=25\text{V}$, $R_{GS}=25\Omega$ | E_{AS} | 250 | mJ |
| Repetitive avalanche energy, limited by $T_{jmax}^{2)}$ | E_{AR} | 13 | |
| Reverse diode dv/dt $I_S=50\text{A}$, $V_{DS}=24\text{V}$, $di/dt=200\text{A}/\mu\text{s}$, $T_{jmax}=175^\circ\text{C}$ | dv/dt | 6 | kV/ μs |
| Gate source voltage | V_{GS} | ± 20 | V |
| Power dissipation $T_C=25^\circ\text{C}$ | P_{tot} | 136 | W |
| Operating and storage temperature | T_j , T_{stg} | -55... +175 | $^\circ\text{C}$ |
| IEC climatic category; DIN IEC 68-1 | | 55/175/56 | |

Thermal Characteristics

| Parameter | Symbol | Values | | | Unit |
|--|------------|--------|------|------|------|
| | | min. | typ. | max. | |
| Characteristics | | | | | |
| Thermal resistance, junction - case | R_{thJC} | - | 0.7 | 1.1 | K/W |
| Thermal resistance, junction - ambient, leaded | R_{thJA} | - | - | 100 | |
| SMD version, device on PCB: | R_{thJA} | | | | |
| @ min. footprint | | - | - | 75 | |
| @ 6 cm ² cooling area ³⁾ | | - | - | 50 | |

Electrical Characteristics, at $T_j = 25^\circ\text{C}$, unless otherwise specified

| Parameter | Symbol | Values | | | Unit |
|--|---------------|--------|------------|----------|------------|
| | | min. | typ. | max. | |
| Static Characteristics | | | | | |
| Drain-source breakdown voltage $V_{GS}=0V, I_D=1mA$ | $V_{(BR)DSS}$ | 30 | - | - | V |
| Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D = 85 \mu A$ | $V_{GS(th)}$ | 1.2 | 1.6 | 2 | |
| Zero gate voltage drain current $V_{DS}=30V, V_{GS}=0V, T_j=25^{\circ}C$ $V_{DS}=30V, V_{GS}=0V, T_j=125^{\circ}C$ | I_{DSS} | - - | 0.01 10 | 1 100 | μA |
| Gate-source leakage current $V_{GS}=20V, V_{DS}=0V$ | I_{GSS} | - | 1 | 100 | |
| Drain-source on-state resistance $V_{GS}=4.5V, I_D=50A$ | $R_{DS(on)}$ | - | 6.8 | 9.2 | m Ω |
| Drain-source on-state resistance $V_{GS}=10V, I_D=50A$ | $R_{DS(on)}$ | - | 4.7 | 6.4 | |

¹Current limited by bondwire ; with an $R_{thJC} = 1.1K/W$ the chip is able to carry $I_D = 113A$ at 25°C , for detailed information see app.-note ANPS071E available at www.infineon.com/optimos

²Defined by design. Not subject to production test.

³Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air.

Electrical Characteristics

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Dynamic Characteristics

| | | | | | | |
|------------------------------|--------------|---|----|------|------|----|
| Transconductance | g_{fs} | $V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$, $I_D = 50A$ | 36 | 72 | - | S |
| Input capacitance | C_{iss} | $V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1MHz$ | - | 1900 | 2530 | pF |
| Output capacitance | C_{oss} | | - | 740 | 990 | |
| Reverse transfer capacitance | C_{rss} | | - | 180 | 270 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD} = 15V$, $V_{GS} = 10V$, $I_D = 50A$, $R_G = 3.6\Omega$ | - | 8 | 12 | ns |
| Rise time | t_r | | - | 19 | 29 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 35 | 53 | |
| Fall time | t_f | | - | 24 | 36 | |

Gate Charge Characteristics

| | | | | | | |
|-----------------------|-----------------|---|---|------|------|----|
| Gate to source charge | Q_{gs} | $V_{DD} = 24V$, $I_D = 50A$ | - | 6 | 8 | nC |
| Gate to drain charge | Q_{gd} | | - | 17.8 | 26.7 | |
| Gate charge total | Q_g | $V_{DD} = 24V$, $I_D = 50A$, $V_{GS} = 0$ to $10V$ | - | 52 | 68 | |
| Gate plateau voltage | $V_{(plateau)}$ | $V_{DD} = 24V$, $I_D = 50A$ | - | 3.2 | - | V |

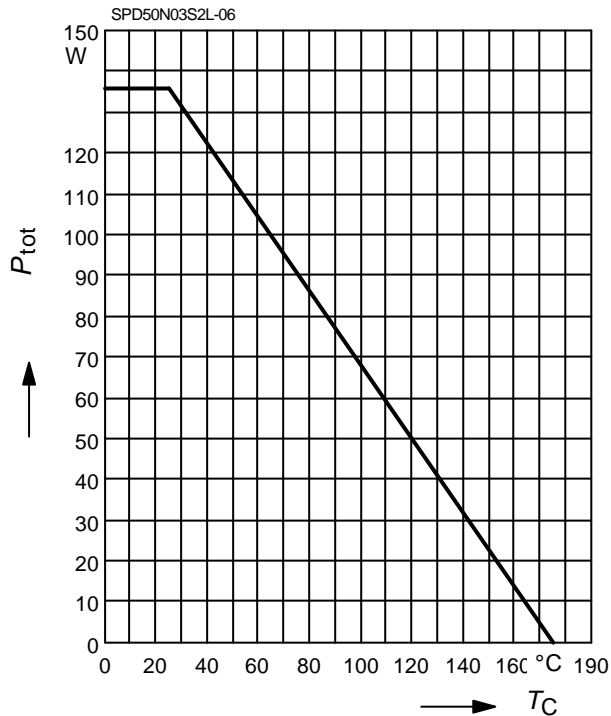
Reverse Diode

| | | | | | | |
|--|----------|---|---|-----|-----|----|
| Inverse diode continuous forward current | I_S | $T_C = 25^\circ C$ | - | - | 50 | A |
| Inv. diode direct current, pulsed | I_{SM} | | - | - | 200 | |
| Inverse diode forward voltage | V_{SD} | $V_{GS} = 0V$, $I_F = 50A$ | - | 0.9 | 1.3 | V |
| Reverse recovery time | t_{rr} | $V_R = 15V$, $I_F = I_S$, $di_F/dt = 100A/\mu s$ | - | 41 | 51 | ns |
| Reverse recovery charge | Q_{rr} | | - | 46 | 58 | nC |

1 Power dissipation

$$P_{\text{tot}} = f(T_C)$$

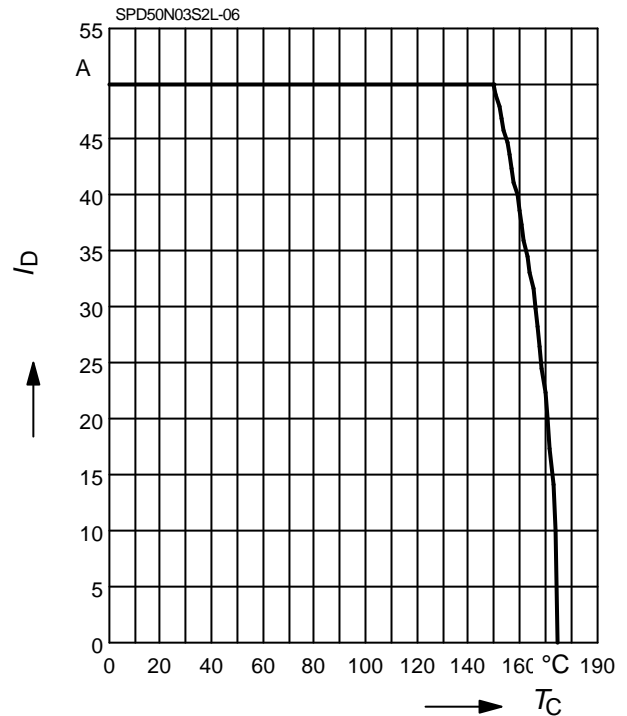
parameter: $V_{GS} \geq 4 \text{ V}$



2 Drain current

$$I_D = f(T_C)$$

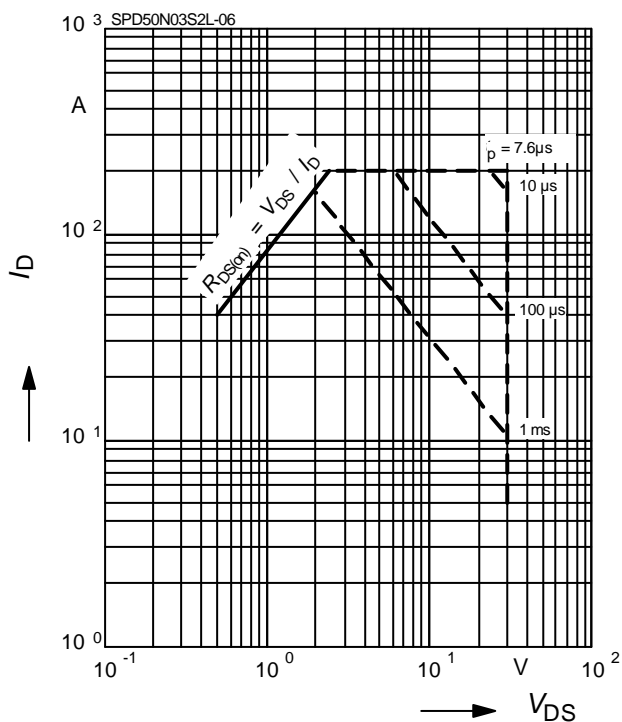
parameter: $V_{GS} \geq 10 \text{ V}$



3 Safe operating area

$$I_D = f(V_{DS})$$

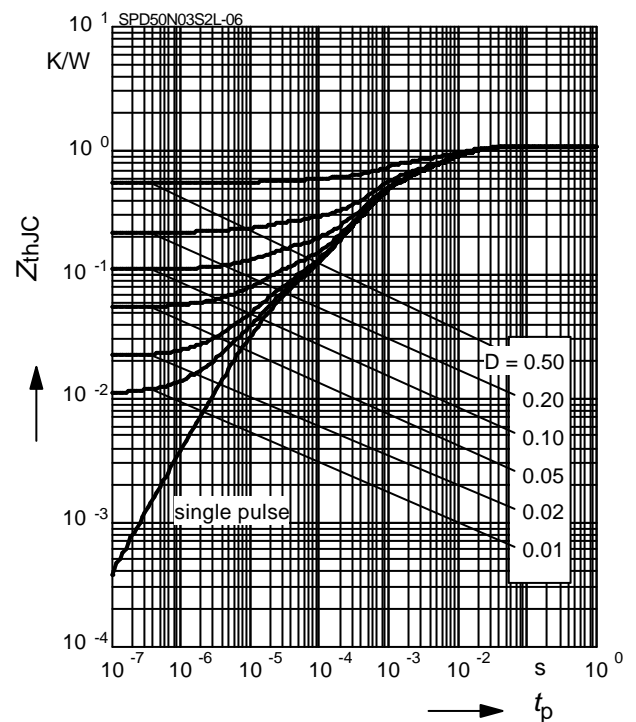
parameter: $D = 0$, $T_C = 25 \text{ °C}$



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

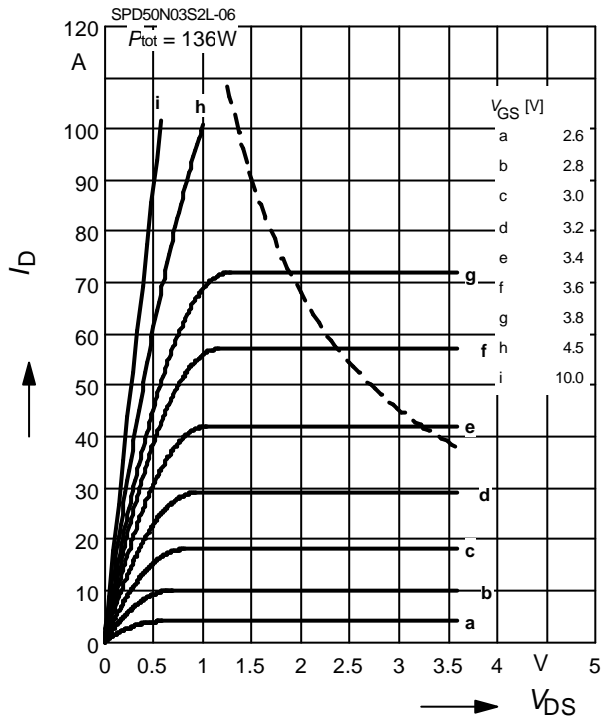
parameter: $D = t_p/T$



5 Typ. output characteristic

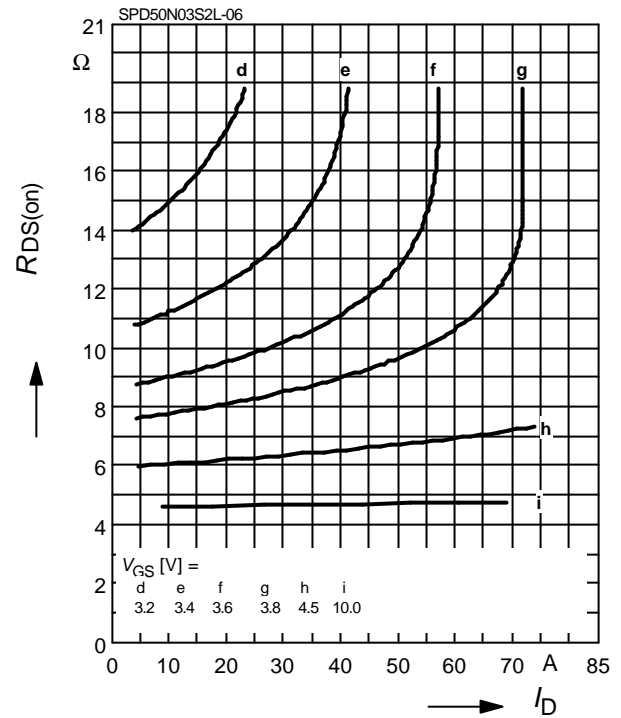
$$I_D = f(V_{DS}); T_J = 25^\circ\text{C}$$

parameter: $t_p = 80 \mu\text{s}$


6 Typ. drain-source on resistance

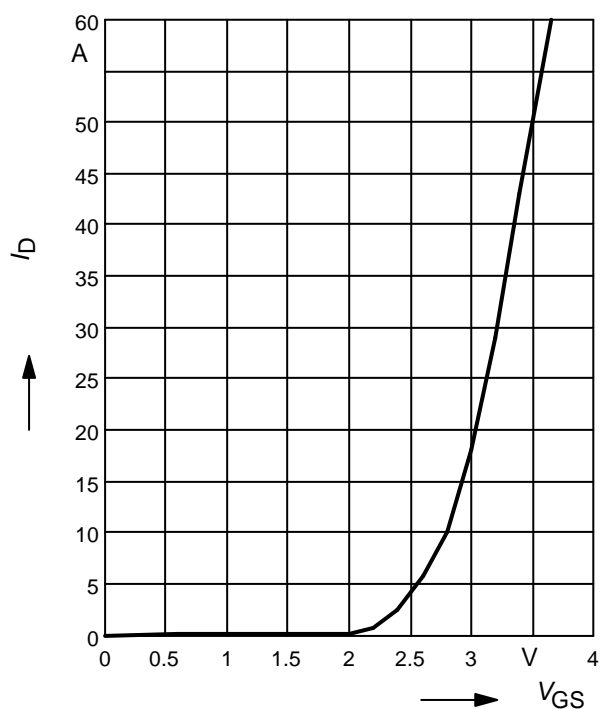
$$R_{DS(on)} = f(I_D)$$

parameter: $V_{GS} = 10\text{V}$


7 Typ. transfer characteristics

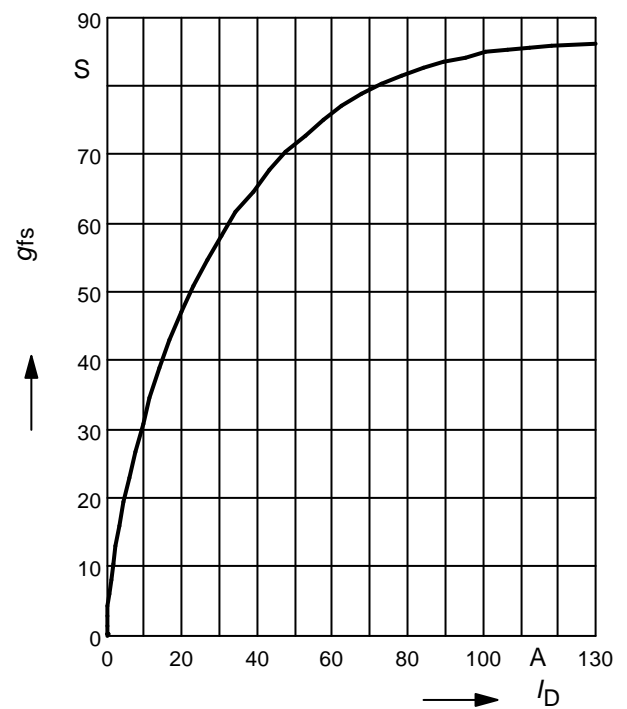
$$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$$

parameter: $t_p = 80 \mu\text{s}$


8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_J = 25^\circ\text{C}$$

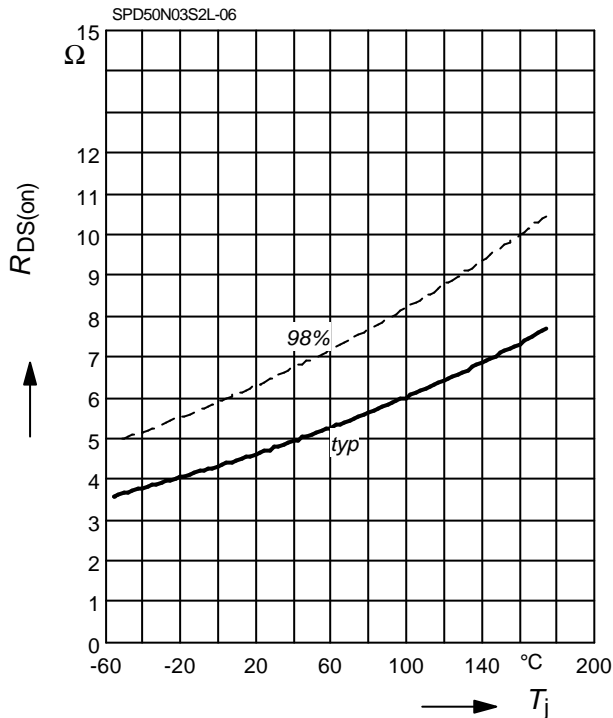
parameter: g_{fs}



9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j)$$

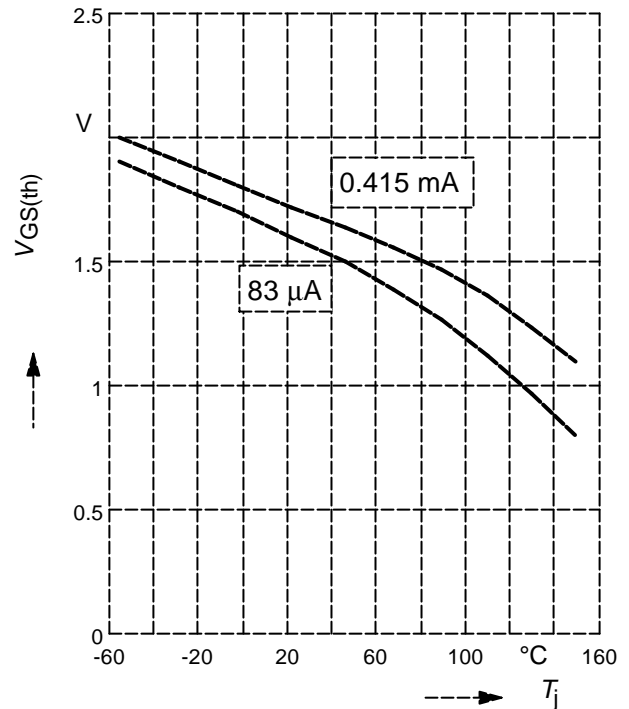
parameter: $I_D = 50\text{ A}$, $V_{GS} = 10\text{ V}$



10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j)$$

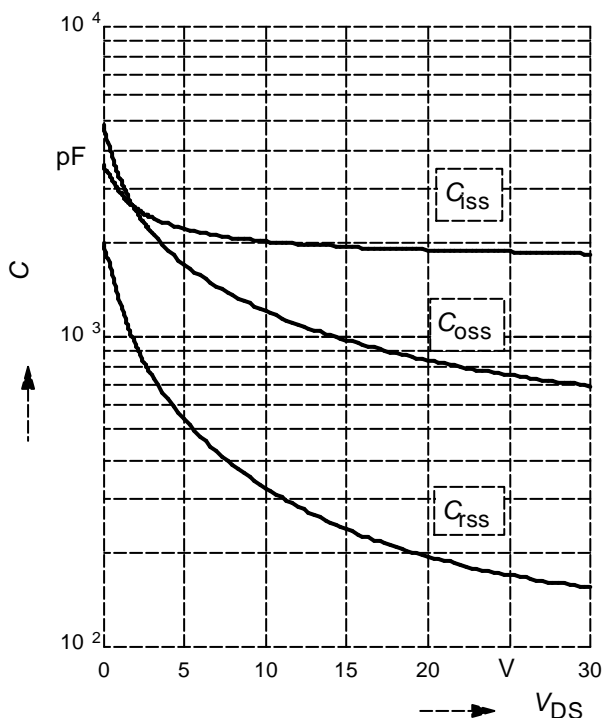
parameter: $V_{GS} = V_{DS}$



11 Typ. capacitances

$$C = f(V_{DS})$$

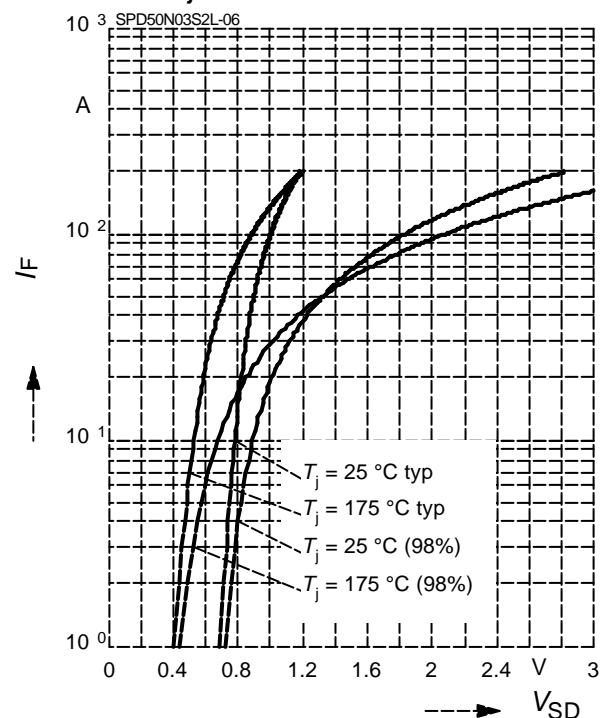
parameter: $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$



12 Forward character. of reverse diode

$$I_F = f(V_{SD})$$

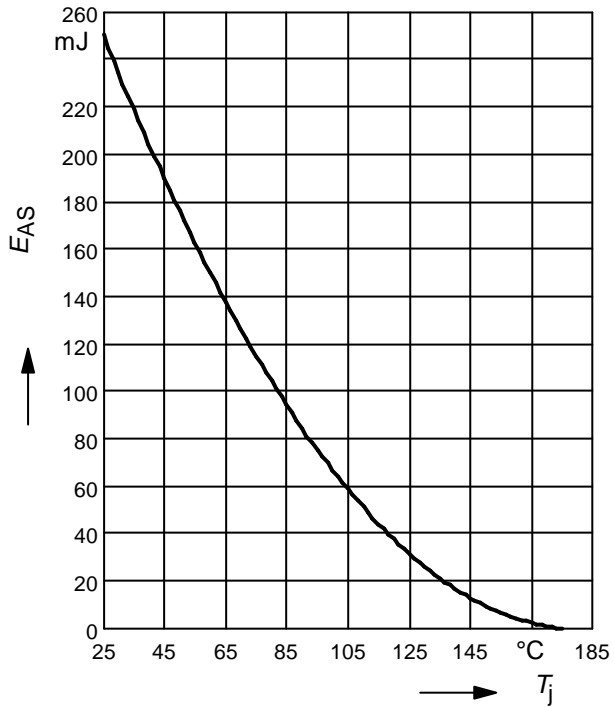
parameter: T_j , $t_p = 80\text{ }\mu\text{s}$



13 Typ. avalanche energy

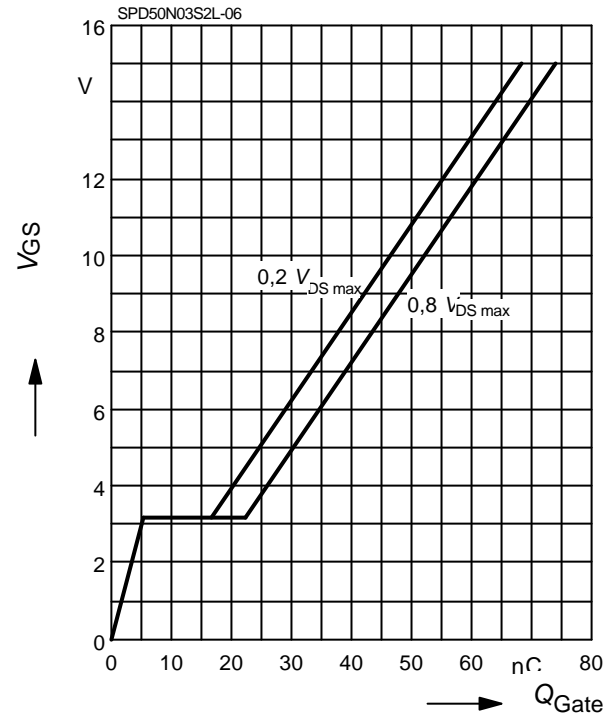
$$E_{AS} = f(T_j)$$

par.: $I_D = 50\text{ A}$, $V_{DD} = 25\text{ V}$, $R_{GS} = 25\ \Omega$


14 Typ. gate charge

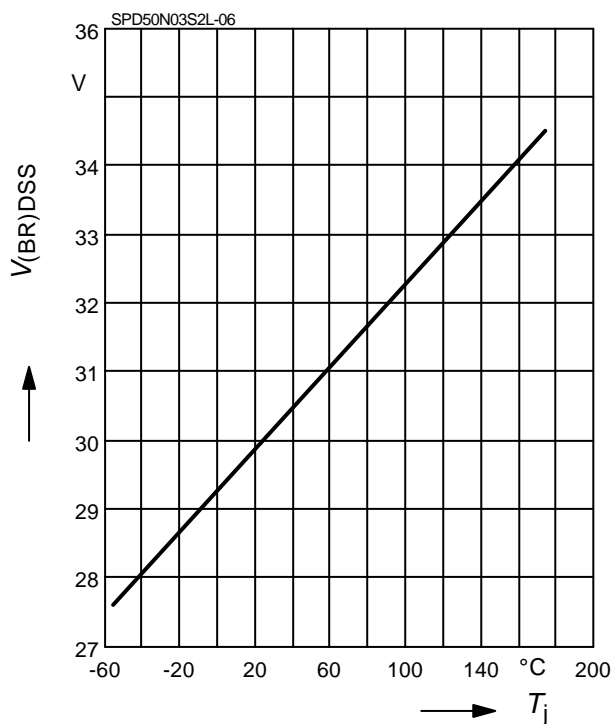
$$V_{GS} = f(Q_{Gate})$$

parameter: $I_D = 50\text{ A}$ pulsed


15 Drain-source breakdown voltage

$$V_{(BR)DSS} = f(T_j)$$

parameter: $I_D = 10\text{ mA}$



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Further information

Please notice that the part number is BSPD50N03S2L-06, for simplicity the device is referred to by the term SPD50N03S2L-06 throughout this documentation.