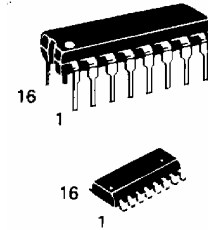


DUAL J-K FLIP-FLOP WITH SET AND RESET High-Performance Silicon-Gate CMOS

The IN74HCT109 is identical in pinout to the LS/ALS109. The IN74HCT109 may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

This device consists of two J- \bar{K} flip-flops with individual set, reset, and clock inputs. Changes at the inputs are reflected at the outputs with the next low-to-high transition of the clock. Both Q to \bar{Q} outputs are available from each flip-flop.

- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A



**N SUFFIX
PLASTIC**

**D SUFFIX
SOIC**

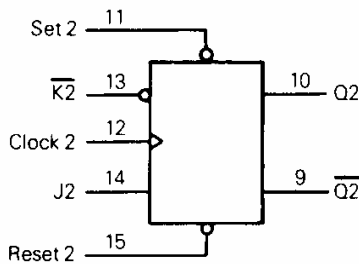
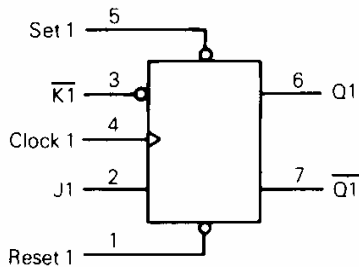
ORDERING INFORMATION

IN74HCT109N Plastic

IN74HCT109D SOIC

$T_A = -55^\circ$ to 125° C for all packages.

LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND

PIN ASSIGNMENT

RESET 1	1	16	V_{CC}
J1	2	15	RESET 2
$\bar{K}1$	3	14	J2
CLOCK 1	4	13	$\bar{K}2$
SET 1	5	12	CLOCK 2
Q1	6	11	SET 2
$\bar{Q}1$	7	10	Q2
GND	8	9	$\bar{Q}2$

FUNCTION TABLE

Inputs					Output	
Set	Reset	Clock	J	\bar{K}	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	X	L	L	L	H
H	H	X	H	L	Toggle	
H	H	X	L	H	No Change	
H	H	X	H	H	H	L
H	H	L	X	X	No Change	

X = Don't care

*Both outputs will remain high as long as Set and Reset are low., but the output states are unpredictable if Set and Reset go high simultaneously.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low -Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IL} or V _{IH} I _{OUT} ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V _{IN} = V _{IL} or V _{IH} I _{OUT} ≤4.0 mA	4.5	0.26	0.33	0.4	
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	5.5	4.0	40	80	μA
ΔI _{CC}	Additional Quiescent	V _{IN} = 2.4 V, Any One Input V _{IN} =V _{CC} or GND, Other Inputs		≥-55°C	25°C to 125°C		μA
	Supply Current	I _{OUT} =0μA	5.5	2.9	2.4		

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.5\text{ V} \pm 10\%$, $C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85 °C	≤125 °C	
f_{\max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	30	24	20	MHz
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Q or \bar{Q} (Figures 1 and 4)	35	44	53	ns
t_{PHL}	Maximum Propagation Delay, Set or Reset to Q or \bar{Q} (Figures 2 and 4)	46	58	69	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	15	19	22	ns
C_{IN}	Maximum Input Capacitance	10	10	10	pF

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop)	Typical @25°C,V _{CC} =5.0 V	pF
	Used to determine the no-load dynamic power consumption: P _D =C _{PD} V _{CC} ² f+I _{CC} V _{CC} +ΔI _{CC} V _{CC}	60	

TIMING REQUIREMENTS ($V_{CC}=5.5\text{ V} \pm 10\%$, $C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125°C	
t_{SU}	Minimum Setup Time, J or K to Clock (Figure 3)	20	25	30	ns
t_h	Minimum Hold Time, Clock to J or K (Figure 3)	5	5	5	ns
t_{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	5	5	5	ns
t_w	Minimum Pulse Width, Set or Reset (Figure 2)	16	20	24	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	16	20	24	ns
t_r , t_f	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

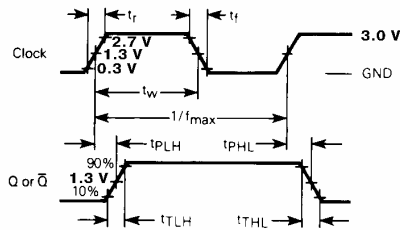


Figure 1. Switching Waveforms

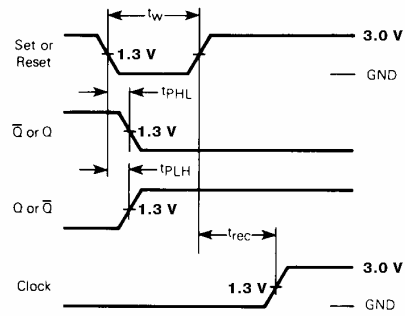


Figure 2. Switching Waveforms

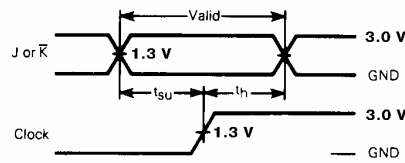
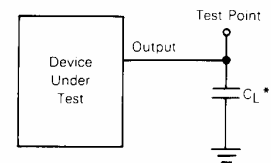


Figure 3. Switching Waveforms



* Includes all probe and jig capacitance.

Figure 4. Switching Waveforms

EXPANDED LOGIC DIAGRAM

