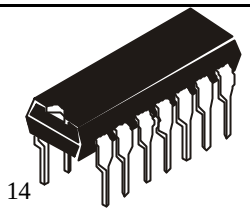
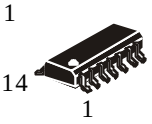
IN74LV164

8-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER



N SUFFIX
PLASTIC DIP



D SUFFIX
SO

ORDERING INFORMATION

IN74LV164N	Plastic DIP
IN74LV164D	SOIC
IZ74LV164	chip

T_A = -40° to 125° C for all packages

The IN74LV164 is a low-voltage Si-gate CMOS device and is pin and function compatible with the IN74HC/HCT164.

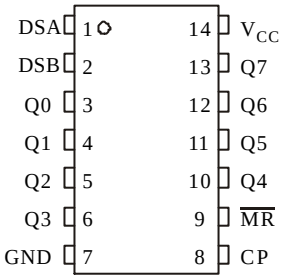
The IN74LV164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (DSA or DSB); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into Q_0, which is the logical AND of the two data inputs (DSA, DSB) that existed one set-up time prior to the rising clock edge.

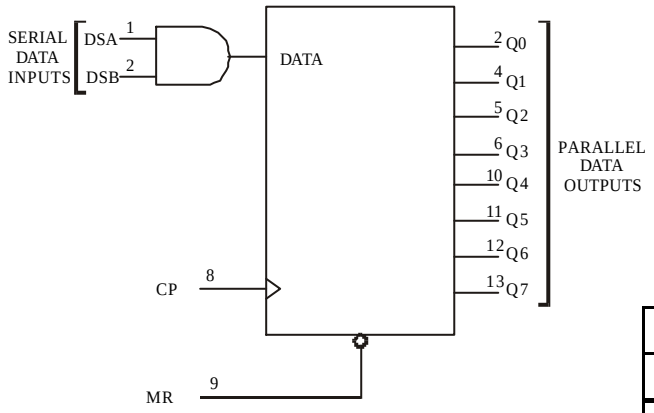
A LOW on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 1.2 to 5.5 V
- Low Input Current: 1.0 µA, 0.1 µÀ at Ò = 25 °Ñ
- Output Current: 6 mA at V_{CC} = 3.0 V; 12 mA at V_{CC} = 4.5 V
- High Noise Immunity Characteristic of CMOS Devices

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 14=V_{CC}
PIN 7 = GND

FUNCTION TABLE

Inputs				Outputs	
$\overline{MR}$	CP	DSA	DSB	Q0	Q1 ... Q7
L	X	X	X	L	L … L
H	⎍	L	L	L	Q0 ... Q6
H	⎍	L	H	L	Q0 ... Q6
H	⎍	H	L	L	Q0 ... Q6
H	⎍	H	H	H	Q0 ... Q6

H = high voltage level
L = low voltage level
X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.5 to + 7.0	V
I_{IK} *1	DC Input diode current	±20	mA
I_{OK} *2	DC Output diode current	±50	mA
I_O *3	DC Output source or sink current	±25	mA
I_{CC}	V_{CC} current	±50	mA
I_{GND}	GND current	±50	mA
P_D	Power dissipation per package: *4 Plastic DIP SO	 750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
*1 $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V.
*2 $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V.
*3 -0.5 V $< V_O < V_{CC} + 0.5$ V.
*4 Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
SO Package: : - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		1.2	5.5	V
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	1.0 V ≤ V_{CC} < 2.0 V	0	500	ns
		2.0 V ≤ V_{CC} < 2.7 V	0	200	
		2.7 V ≤ V_{CC} < 3.6 V	0	100	
		3.6 V ≤ V_{CC} ≤ 5.5 V	0	50	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				25°C to -40°C		85°C		125°C		
				min	max	min	max	min	max	
V_{IH}	HIGH level input voltage		1.2 2.0 2.7 3.0 3.6 4.5 5.5	0.9 1.4 2.0 2.0 2.0 3.15 3.85	- - - - - - -	0.9 1.4 2.0 2.0 2.0 3.15 3.85	- - - - - - -	0.9 1.4 2.0 2.0 2.0 3.15 3.85	- - - - - - -	V
V_{IL}	LOW level input voltage		1.2 2.0 2.7 3.0 3.6 4.5 5.5	- - - - - - -	0.3 0.6 0.8 0.8 0.8 1.35 1.65	- - - - - - -	0.3 0.6 0.8 0.8 0.8 1.35 1.65	- - - - - - -	0.3 0.6 0.8 0.8 0.8 1.35 1.65	V
V_{OH}	HIGH level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = -100 µÀ	1.2 2.0 2.7 3.0 3.6 4.5 5.5	1.05 1.85 2.55 2.85 3.45 4.35 5.35	- - - - - - -	1.0 1.8 2.5 2.8 3.4 4.3 5.3	- - - - - - -	1.0 1.8 2.5 2.8 3.4 4.3 5.3	- - - - - - -	V
		$V_I = V_{IH}$ or V_{IL} I_O = -6.0 mÀ	3.0	2.48	-	2.40	-	2.20	-	V
		$V_I = V_{IH}$ or V_{IL} I_O = -12.0 mÀ	4.5	3.70	-	3.60	-	3.50	-	V
V_{OL}	LOW level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = 100 µÀ	1.2 2.0 2.7 3.0 3.6 4.5 5.5	- - - - - - -	0.15 0.15 0.15 0.15 0.15 0.15 0.15	- - - - - - -	0.2 0.2 0.2 0.2 0.2 0.2 0.2	- - - - - - -	0.2 0.2 0.2 0.2 0.2 0.2 0.2	V
		$V_I = V_{IH}$ or V_{IL} I_O = 6.0 mÀ	3.0	-	0.33	-	0.4	-	0.5	V
		$V_I = V_{IH}$ or V_{IL} I_O = 12.0 mÀ	4.5	-	0.40	-	0.55	-	0.65	V
I_I	Input current	$V_I = V_{CC}$ or 0 V	5.5	-	±0.1	-	±1.0	-	±1.0	µÀ
I_{CC}	Supply current	$V_I = V_{CC}$ or 0 V I_O = 0 µÀ	5.5	-	8.0	-	80	-	160	µÀ
I_{CC1}	Supply current	$V_I = V_{CC} - 0.6$ V	2.7 3.6	-	0.2	-	0.5	-	0.85	mÀ

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, t_r=t_f= 2.5 ns, R_L = 1 kΩ)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				25°C to -40°C		85°C		125°C		
				min	max	min	max	min	max	
t_{PHL}, t_{PLH}	Propagation delay , CP to Qn	V_I = 0 V or V_1 Figure 1 and 4	1.2	-	150	-	180	-	210	ns
			2.0	-	30	-	39	-	49	
			2.7	-	23	-	29	-	36	
			3.0	-	18	-	23	-	29	
			4.5	-	15	-	19	-	24	
t_{PHL}	Propagation delay , $\overline{MR}$ to Qn	V_I = 0 V or V_1 Figure 1 and 4	1.2	-	150	-	180	-	210	ns
			2.0	-	30	-	39	-	49	
			2.7	-	23	-	29	-	36	
			3.0	-	18	-	23	-	29	
			4.5	-	15	-	19	-	24	
t_w	Pulse Width, CP or MR	V_I = 0 V or V_1 Figure 1	1.2	100	-	130	-	160	-	ns
			2.0	28	-	34	-	41	-	
			2.7	21	-	25	-	30	-	
			3.0	17	-	20	-	24	-	
			4.5	14	-	17	-	20	-	
t_{su}	Setup Time, DSA or DSB to CP	V_I = 0 V or V_1 Figure 3	1.2	60	-	80	-	100	-	ns
			2.0	19	-	22	-	26	-	
			2.7	13	-	16	-	19	-	
			3.0	11	-	13	-	15	-	
			4.5	9	-	11	-	13	-	
t_h	Hold Time, DSA or DSB to CP	V_I = 0 V or V_1 Figure 3	1.2	50	-	50	-	50	-	ns
			2.0	5	-	5	-	5	-	
			2.7	5	-	5	-	5	-	
			3.0	5	-	5	-	5	-	
			4.5	5	-	5	-	5	-	
t_{rec}	Recovery Time, $\overline{MR}$ to CP	V_I = 0 V or V_1 Figure 2	1.2	70	-	100	-	130	-	ns
			2.0	15	-	19	-	24	-	
			2.7	11	-	14	-	18	-	
			3.0	9	-	11	-	14	-	
			4.5	8	-	10	-	12	-	
f_{max}	Clock Frequency	V_I = 0 V or V_1 Figure 1 and 4	1.2	-	2	-	1	-	1	MHz
			2.0	-	16	-	14	-	12	
			2.7	-	22	-	19	-	16	
			3.0	-	27	-	24	-	20	
			4.5	-	32	-	27	-	24	
C_I	Input capacitance		5.0	-	7.0	-	-	-	-	pF
C_{PD}	Power dissipation capacitance	V_I = 0 V or V_{CC}	5.5	-	80	-	-	-	-	pF

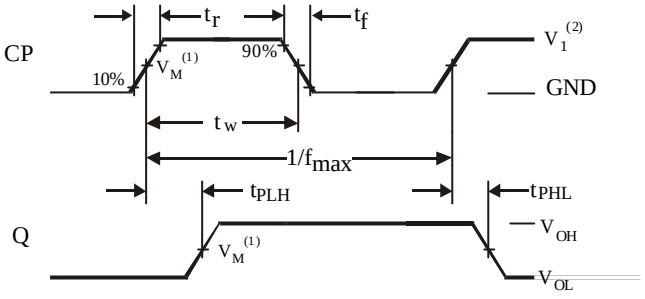


Figure 1. Switching Waveforms

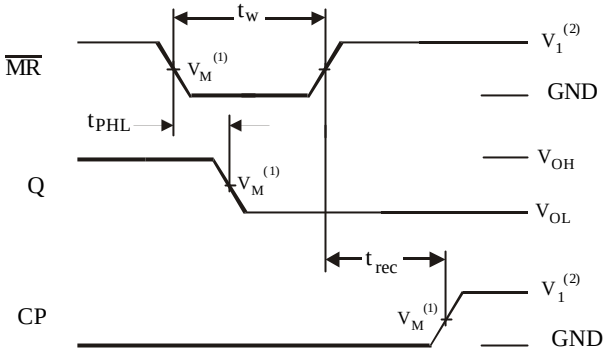


Figure 2. Switching Waveforms

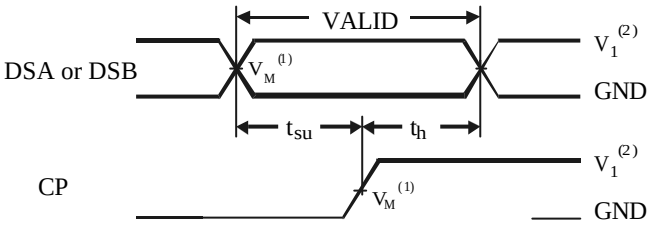
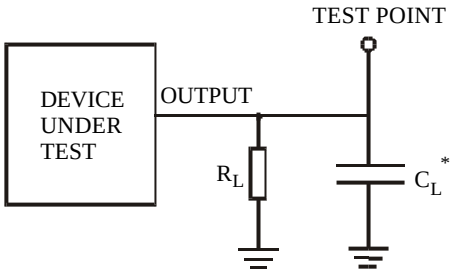


Figure 3. Switching Waveforms



* Includes all probe and jig capacitance

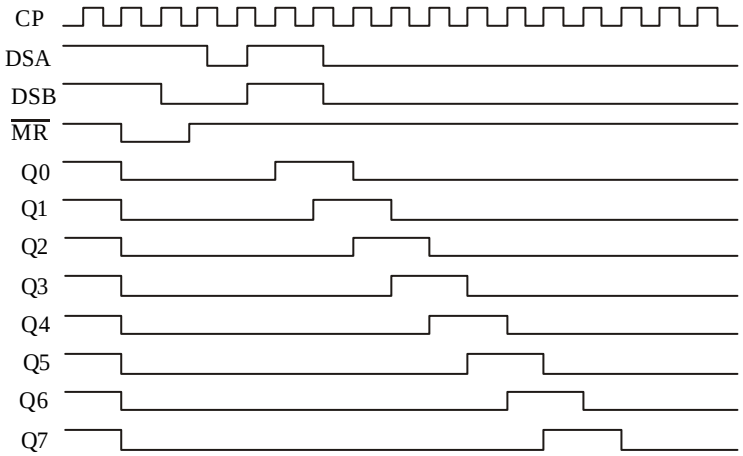
Figure 4. Test Circuit

Note:

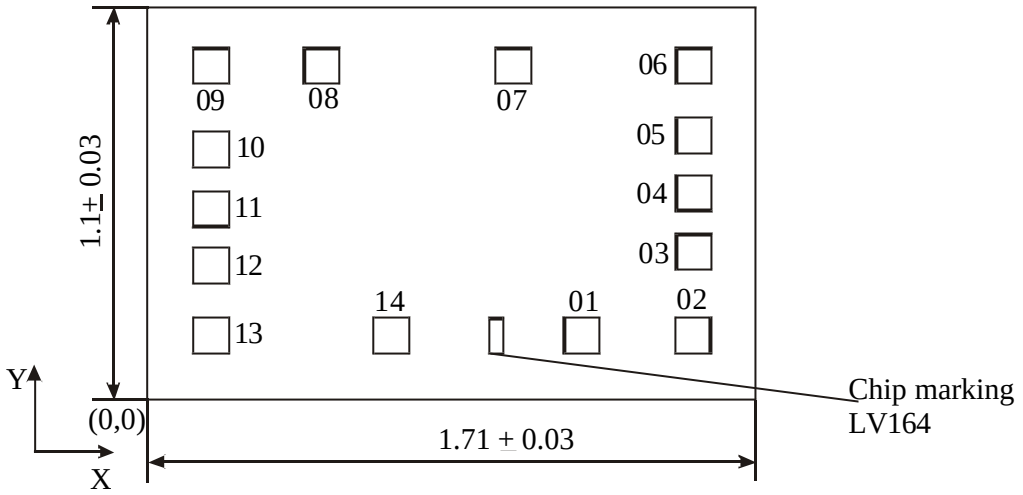
(1) V_M = 1.5 V at V_{CC} = 2.7 V
$V_M = 0.5 \cdot V_{CC}$ at V_{CC} =1.2 V, 2.0 V, 3.0 V, 4.5 V

(2) $V_1 = V_{CC}$ at V_{CC} =1.2 V, 2.0 V, 2.7 V, 4.5 V
V_1 = 2.7 V at V_{CC} = 3.0 V

TIMING DIAGRAM



CHIP PAD DIAGRAM



Location of marking (mm): left lower corner x= 0.960, y= 0.130.

Chip thickness: 0.46 ± 0.02 (0.35 ± 0.02) mm.

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	DSA	1.172	0.131	0.100 õ 0.100
02	DSB	1.486	0.131	0.100 õ 0.100
03	Q0	1.486	0.363	0.100 õ 0.100
04	Q1	1.486	0.531	0.100 õ 0.100
05	Q2	1.486	0.689	0.100 õ 0.100
06	Q3	1.486	0.885	0.100 õ 0.100
07	GND	0.978	0.885	0.100 õ 0.100
08	CP	0.440	0.885	0.100 õ 0.100
09	$\overline{MR}$	0.127	0.885	0.100 õ 0.100
10	Q4	0.127	0.653	0.100 õ 0.100
11	Q5	0.127	0.485	0.100 õ 0.100
12	Q6	0.127	0.326	0.100 õ 0.100
13	Q7	0.127	0.131	0.100 õ 0.100
14	V_{CC}	0.635	0.131	0.100 õ 0.100

Note: Pad location is given as per passivation layer