



P8748H/P8749H 8048AH/8035AHL/8049AH/8039AHL/8050AH/8040AHL HMOS SINGLE-COMPONENT 8-BIT MICROCONTROLLER

- High Performance HMOS II
- Interval Time/Event Counter
- Two Single Level Interrupts
- Single 5-Volt Supply
- Over 96 Instructions; 90% Single Byte
- Programmable ROMs Using 21V
- Easily Expandable Memory and I/O
- Up to 1.36 μ s Instruction Cycle All Instructions 1 or 2 Cycles

The Intel MCS®-48 family are totally self-sufficient, 8-bit parallel computers fabricated on single silicon chips using Intel's advanced N-channel silicon gate HMOS process.

The family contains 27 I/O lines, an 8-bit timer/counter, and on-board oscillator/clock circuits. For systems that require extra capability, the family can be expanded using MCS®-80/MCS®-85 peripherals.

These microcontrollers are available in both masked ROM and ROMless versions as well as a new version, The Programmable ROM. The Programmable ROM provides the user with the capability of a masked ROM while providing the flexibility of a device that can be programmed at the time of requirement and to the desired data. Programmable ROM's allow the user to lower inventory levels while at the same time decreasing delay times and code risks.

These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting of mostly single byte instructions and no instructions over 2 bytes in length.

Device	Internal	Memory	RAM STANDBY
8050AH	4K x 8 ROM	256 x 8 RAM	yes
8049AH	2K x 8 ROM	128 x 8 RAM	yes
8048AH	1K x 8 ROM	64 x 8 RAM	yes
8040AHL	None	256 x 8 RAM	yes
8039AHL	None	128 x 8 RAM	yes
8035AHL	None	64 x 8 RAM	yes
P8749H	2K x 8 Programmable ROM	128 x 8 RAM	no
P8748H	1K x 8 Programmable ROM	64 x 8 RAM	no

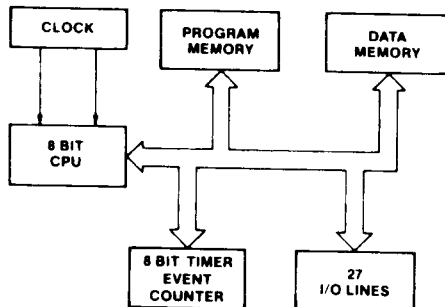


Figure 1. Block Diagram

270053-1

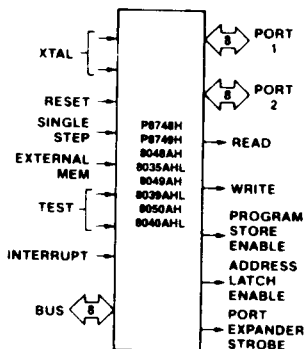


Figure 2. Logic Symbol

270053-2

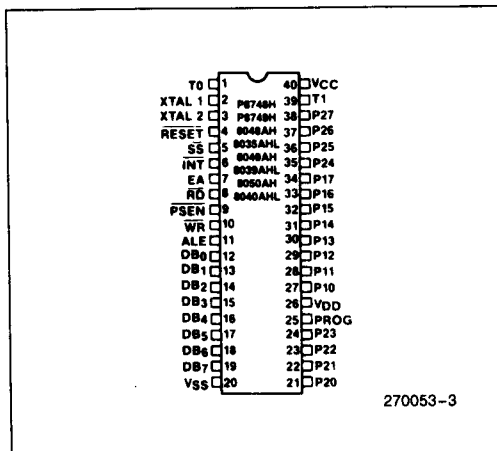


Figure 3. Pin Configuration

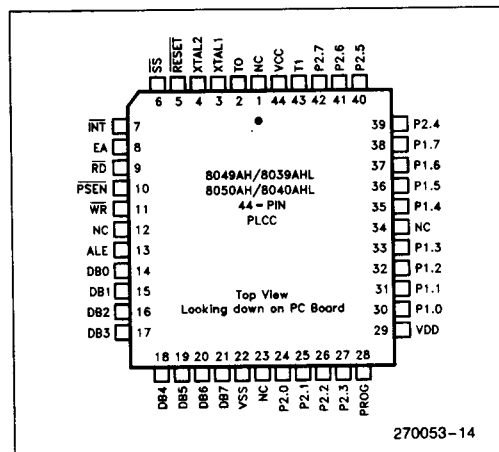


Figure 4. Pad Configuration

Table 1. Pin Description

Symbol	Pin No.	Function	Device
VSS	20	Circuit GND potential.	All
VDD	26	+ 5V during normal operation.	All
		Low power standby pin.	8048AH 8035AHL 8049AH 8039AHL 8050AH 8040AHL
		Programming power supply (+ 21V).	P8748H P8749H
VCC	40	Main power supply; + 5V during operation and programming.	All
PROG	25	Output strobe for 8243 I/O expander.	All
		Program pulse (+ 18V) input pin During Programming.	P8748H P8749H
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.	All
P20-P23 P24-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.	All
DB0-DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the RD, WR strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, RD, and WR.	All
T0	1	Input pin testable using the conditional transfer instruction JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.	All
		Used during programming.	P8748H P8749H

Table 1. Pin Description (Continued)

Symbol	Pin No.	Function	Device
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.	All
INT	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low) interrupt must remain low for at least 3 machine cycles for proper operation.	All
RD	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. (Active low)	All
RESET	4	Input which is used to initialize the processor. (Active low) (Non TTL V_{IH})	All
		Used during power down.	8048AH 8035AHL 8049AH 8039AHL 8050AH 8040AHL
		Used during programming.	P8748H P8749H
		Used during ROM verification.	8048AH P8748H 8049AH P8749H 8050AH
WR	10	Output strobe during a bus write. (Active low) Used as write strobe to external data memory.	All
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.	All
PSEN	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)	All
SS	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction.	All
		(Active low) Used in sync mode.	8048AH 8035AHL 8049AH 8039AHL 8050AH 8040AHL
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug. (Active high)	All
		Used during (18V) programming.	P8748H P8749H
		Used during ROM verification (12V).	8048AH 8049AH 8050AH
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})	All
XTAL2	3	Other side of crystal input.	All

Table 2. Instruction Set

Accumulator				Input/Output			
Mnemonic	Description	Bytes	Cycles	Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1	IN A, P	Input port to A	1	2
ADD A, @R	Add data memory to A	1	1	OUTL P, A	Output A to port	1	2
ADD A, #data	Add immediate to A	2	2	ANL P, #data	And immediate to port	2	2
ADDC A, R	Add register with carry	1	1	ORL P, #data	Or immediate to port	2	2
ADDC A, @R	Add data memory with carry	1	1	INS A, BUS	Input BUS to A	1	2
ADDC A, #data	Add immediate with carry	2	2	OUTL BUS, A	Output A to BUS	1	2
ANL A, R	And register to A	1	1	ANL BUS, #data	And immediate to BUS	2	2
ANL A, @R	And data memory to A	1	1	ORL BUS, #data	Or immediate to BUS	2	2
ANL A, #data	And immediate to A	2	2	MOVD A, P	Input expander port to A	1	2
ORL A, R	Or register to A	1	1	MOVD P, A	Output A to expander port	1	2
ORL A, @R	Or data memory to A	1	1	ANLD P, A	And A to expander port	1	2
ORL A, #data	Or immediate to A	2	2	ORLD P, A	Or A to expander port	1	2
XRL A, R	Exclusive or register to A	1	1				
XRL A, @R	Exclusive or data memory to A	1	1	Registers			
XRL A, #data	Exclusive or immediate to A	2	2	Mnemonic	Description	Bytes	Cycles
INC A	Increment A	1	1	INC R	Increment register	1	1
DEC A	Decrement A	1	1	INC @R	Increment data memory	1	1
CLR A	Clear A	1	1	DEC R	Decrement register	1	1
CPL A	Complement A	1	1				
DA A	Decimal adjust A	1	1	Branch			
SWAP A	Swap nibbles of A	1	1	Mnemonic	Description	Bytes	Cycles
RL A	Rotate A left	1	1	JMP addr	Jump unconditional	2	2
RLC A	Rotate A left through carry	1	1	JMPP @A	Jump indirect	1	2
RR A	Rotate A right	1	1	DJNZ R, addr	Decrement register and skip	2	2
RRC A	Rotate A right through carry	1	1	JC addr	Jump on carry = 1	2	2
				JNC addr	Jump on carry = 0	2	2
				JZ addr	Jump on A zero	2	2
				JNZ addr	Jump on A not zero	2	2
				JT0 addr	Jump on T0 = 1	2	2
				JNT0 addr	Jump on T0 = 0	2	2
				JT1 addr	Jump on T1 = 1	2	2
				JNT1 addr	Jump on T1 = 0	2	2
				JF0 addr	Jump on F0 = 1	2	2
				JF1 addr	Jump on F1 = 1	2	2
				JTF addr	Jump on timer flag	2	2
				JNI addr	Jump on $\overline{INT} = 0$	2	2
				JBb addr	Jump on accumulator bit	2	2

Table 2. Instruction Set (Continued)

Subroutine			
Mnemonic	Description	Bytes	Cycles
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2

Flags			
Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	Clear flag 0	1	1
CPL F0	Complement flag 0	1	1
CLR F1	Clear flag 1	1	1
CPL F1	Complement flag 1	1	1

Data Moves			
Mnemonic	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, #data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, #data	Move immediate to register	2	2
MOV @R, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and data memory	1	1
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @A	Move to A from page 3	1	2

Timer/Counter			
Mnemonic	Description	Bytes	Cycles
MOV A, T	Read timer/counter	1	1
MOV T, A	Load timer/counter	1	1
STRT T	Start timer	1	1
STRT CNT	Start counter	1	1
STOP TCNT	Stop timer/counter	1	1
EN TCNTI	Enable timer/counter interrupt	1	1
DIS TCNTI	Disable timer/counter interrupt	1	1

Control			
Mnemonic	Description	Bytes	Cycles
EN I	Enable external interrupt	1	1
DIS I	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT0 CLK	Enable clock output on T0	1	1

Mnemonic	Description	Bytes	Cycles
NOP	No operation	1	1

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias 0°C to +70°C

Storage Temperature -65°C to +150°C

Voltage on any Pin with Respect

to Ground -0.5V to +7V

Power Dissipation 1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS $T_A = 0^\circ\text{C to } +70^\circ\text{C}; V_{CC} = V_{DD} = 5V \pm 10\%; V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions	Device
		Min	Typ	Max			
V_{IL}	Input Low Voltage (All Except RESET, X1, X2)	-0.5		0.8	V		All
V_{IL1}	Input Low Voltage (RESET, X1, X2)	-0.5		0.6	V		All
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, RESET)	2.0		V_{CC}	V		All
V_{IH1}	Input High Voltage (X1, X2, RESET)	3.8		V_{CC}	V		All
V_{OL}	Output Low Voltage (BUS)			0.45	V	$I_{OL} = 2.0 \text{ mA}$	All
V_{OL1}	Output Low Voltage (RD, WR, PSEN, ALE)			0.45	V	$I_{OL} = 1.8 \text{ mA}$	All
V_{OL2}	Output Low Voltage (PROG)			0.45	V	$I_{OL} = 1.0 \text{ mA}$	All
V_{OL3}	Output Low Voltage (All Other Outputs)			0.45	V	$I_{OL} = 1.6 \text{ mA}$	All
V_{OH}	Output High Voltage (BUS)	2.4			V	$I_{OH} = -400 \mu\text{A}$	All
V_{OH1}	Output High Voltage (RD, WR, PSEN, ALE)	2.4			V	$I_{OH} = -100 \mu\text{A}$	All
V_{OH2}	Output High Voltage (All Other Outputs)	2.4			V	$I_{OH} = -40 \mu\text{A}$	All

D.C. CHARACTERISTICS $T_A = 0^\circ\text{C to } +70^\circ\text{C}$; $V_{CC} = V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$ (Continued)

Symbol	Parameter	Limits			Unit	Test Conditions	Device
		Min	Typ	Max			
I_{L1}	Leakage Current (T1, INT)			± 10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$	All
I_{LI1}	Input Leakage Current (P10–P17, P20–P27, EA, SS)			–500	μA	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$	All
I_{LI2}	Input Leakage Current RESET	–10		–300	μA	$V_{SS} \leq V_{IN} \leq 3.8$	All
I_{LO}	Leakage Current (BUS, T0) (High Impedance State)			± 10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$	All
I_{DD}	V_{DD} Supply Current (RAM Standby)		3	5	mA		8048AH 8035AHL
			4	7	mA		8049AH 8039AHL
			5	10	mA		8050AH 8040AHL
$I_{DD} + I_{CC}$	Total Supply Current*		30	65	mA		8048AH 8035AHL
			35	70	mA		8049AH 8039AHL
			40	80	mA		8050AH 8040AHL
			30	100	mA		P8748H
			50	110	mA		P8749H
V_{DD}	RAM Standby Voltage	2.2		5.5	V	Standby Mode Reset $\leq V_{IL1}$	8048AH 8035AH
		2.2		5.5	V		8049AH 8039AH
		2.2		5.5	V		8050AH 8040AHL

* $I_{CC} + I_{DD}$ are measured with all outputs in their high impedance state; RESET low; 11 MHz crystal applied; INT, SS, and EA floating.

1

A.C. CHARACTERISTICS $T_A = 0^\circ\text{C to } +70^\circ\text{C}; V_{CC} = V_{DD} = 5\text{V} \pm 10\%; V_{SS} = 0\text{V}$

Symbol	Parameter	f (t) (Note 3)	11 MHz		Unit	Conditions (Note 1)
			Min	Max		
t	Clock Period	1/xtal freq	90.9	1000	ns	(Note 3)
t _{LL}	ALE Pulse Width	3.5t–170	150		ns	
t _{AL}	Addr Setup to ALE	2t–110	70		ns	(Note 2)
t _{LA}	Addr Hold from ALE	t–40	50		ns	
t _{CC1}	Control Pulse Width ($\overline{\text{RD}}$, $\overline{\text{WR}}$)	7.5t–200	480		ns	
t _{CC2}	Control Pulse Width ($\overline{\text{PSEN}}$)	6t–200	350		ns	
t _{DW}	Data Setup before $\overline{\text{WR}}$	6.5t–200	390		ns	
t _{WD}	Data Hold after $\overline{\text{WR}}$	t–50	40		ns	
t _{DR}	Data Hold ($\overline{\text{RD}}$, $\overline{\text{PSEN}}$)	1.5t–30	0	110	ns	
t _{RD1}	$\overline{\text{RD}}$ to Data in	6t–170		375	ns	
t _{RD2}	$\overline{\text{PSEN}}$ to Data in	4.5t–170		240	ns	
t _{AW}	Addr Setup to $\overline{\text{WR}}$	5t–150	300		ns	
t _{AD1}	Addr Setup to Data ($\overline{\text{RD}}$)	10.5t–220		730	ns	
t _{AD2}	Addr Setup to Data ($\overline{\text{PSEN}}$)	7.5t–200		460	ns	
t _{AFC1}	Addr Float to $\overline{\text{RD}}$, $\overline{\text{WR}}$	2t–40	140		ns	(Note 2)
t _{AFC2}	Addr Float to $\overline{\text{PSEN}}$	0.5t–40	10		ns	(Note 2)
t _{LAF1}	ALE to Control ($\overline{\text{RD}}$, $\overline{\text{WR}}$)	3t–75	200		ns	
t _{LAF2}	ALE to Control ($\overline{\text{PSEN}}$)	1.5t–75	60		ns	
t _{CA1}	Control to ALE ($\overline{\text{RD}}$, $\overline{\text{WR}}$, PROG)	t–65	25		ns	
t _{CA2}	Control to ALE ($\overline{\text{PSEN}}$)	4t–70	290		ns	
t _{CP}	Port Control Setup to PROG	1.5t–80	50		ns	
t _{PC}	Port Control Hold to PROG	4t–260	100		ns	
t _{PR}	PROG to P2 Input Valid	8.5t–120		650	ns	
t _{PF}	Input Data Hold from PROG	1.5t	0	140	ns	
t _{DP}	Output Data Setup	6t–290	250		ns	
t _{PD}	Output Data Hold	1.5t–90	40		ns	
t _{PP}	PROG Pulse Width	10.5t–250	700		ns	
t _{PL}	Port 2 I/O Setup to ALE	4t–200	160		ns	
t _{LP}	Port 2 I/O Hold to ALE	0.5t–30	15		ns	
t _{PV}	Port Output from ALE	4.5t + 100		5.0	ns	
t _{0PRR}	T0 Rep Rate	3t	270		ns	
t _{CY}	Cycle Time	15t	1.36	15.0	μs	

NOTES:1. Control outputs: $C_L = 80\text{ pF}$. BUS Outputs: $C_L = 150\text{ pF}$.

2. BUS High Impedance Load 20 pF

3. f(t) assumes 50% duty cycle on X1, X2. Max clock period is for a 1 MHz crystal input.

INSTRUCTION FETCH FROM PROGRAM MEMORY



The timing diagram shows the relationship between the ALE, RD, and BUS FLOPING signals. The ALE signal is active high. The RD signal is active low. The BUS FLOPING signal is active high. The diagram illustrates the sequence of events: ALE is active high, followed by RD (active low) which is then active high. The bus is floating, then ADDRESS (IAD1) is valid, followed by DATA (IRD1) which is then floating. The diagram also shows the timing for IAF1, ICC1, ICA1, and IDR.

270053-5

The diagram shows the timing of the 270053-6 device. The signals are ALE, WR, and BUS FLOPING. The timing parameters are:

- t_{LAFCl} : Delay from ALE to WR.
- t_{CC1} : Delay from WR to the start of the first data bus cycle.
- t_{CA1} : Delay from WR to the start of the second data bus cycle.
- t_{Dw} : Delay from the start of the first data bus cycle to the start of the second data bus cycle.
- t_{D} : Delay from the start of the second data bus cycle to the start of the third data bus cycle.
- t_{Aw} : Delay from the start of the first data bus cycle to the start of the second data bus cycle.
- t_{Dw} : Delay from the start of the second data bus cycle to the start of the third data bus cycle.

270053-6

2.4V ———— 2.0V ———— 2.0V ————
0.45V ———— 0.8V ———— TEST POINTS ———— 0.8V ————

270053-7

A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Output timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

270053-7

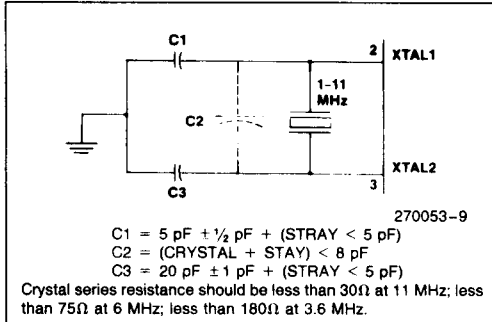
A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Output timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

The diagram illustrates the timing sequence for a memory read cycle. It is divided into a 1st cycle and a 2nd cycle. The signals and their timing parameters are as follows:

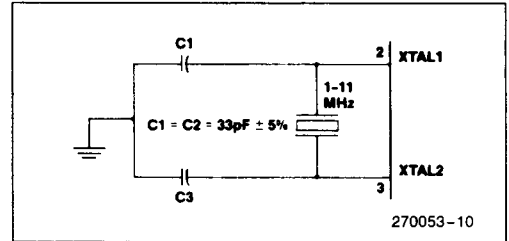
- ALE**: Active Low Enable. Timing: t_{PL} (pulse width), t_{PV} (pulse-to-void time).
- PSEN**: Active Low Strobe. Timing: t_{LP} (pulse width).
- P20-23 OUTPUT**: Data bus output. Timing: t_{LP} (pulse width).
- P24-27 P10-17 OUTPUT**: Data bus output. Timing: t_{LP} (pulse width).
- EXPANDER PORT OUTPUT**: Data bus output. Timing: t_{LP} (pulse width), t_{AL} (address latch enable), t_{LA} (address latch enable), t_{PL} (pulse width), t_{DP} (data pulse width), t_{PD} (data pulse-to-void time).
- EXPANDER PORT INPUT**: Data bus input. Timing: t_{PR} (pulse width), t_{PF} (pulse-to-void time), t_{CP} (clock pulse width), t_{PC} (clock pulse-to-void time).
- PROG**: Active Low Program Strobe. Timing: t_{PP} (pulse width).

270053-8

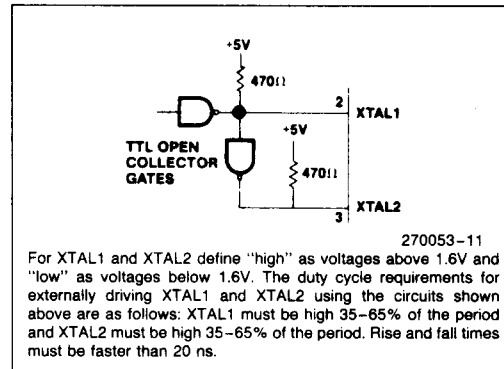
CRYSTAL OSCILLATOR MODE



CERAMIC RESONATOR MODE



DRIVING FROM EXTERNAL SOURCE



PROGRAMMING AND VERIFYING THE P8749H/48H PROGRAMMABLE ROM

Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL1	Clock Input (3 to 4.0 MHz)
XTAL2	
RESET	Initialization and Address Latching
T0	Selection of Program or Verifying Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input
	Data Output During Verify
P20-P22	Address Input
V _{DD}	Programming Power Supply
PROG	Program Pulse Input

WARNING:

An attempt to program a missocketed P8749H/48H will result in severe damage to the part. An indication of a properly socketed part is the appearance of the ALE clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

1. V_{DD} = 5V, Clock applied or internal oscillator operating, RESET = 0V, T0 = 5V, EA = 5V, BUS and PROG floating. P10 and P11 must be tied to ground.
2. Insert P8749H/48H in programming socket
3. T0 = 0V (select program mode)
4. EA = 18V (activate program mode)
5. Address applied to BUS and P20-22
6. RESET = 5V (latch address)
7. Data applied to BUS
8. V_{DD} = 21V (programming power)
9. PROG = V_{CC} or float followed by one 50 ms pulse to 18V
10. V_{DD} = 5V
11. T0 = 5V (verify mode)
12. Read and verify data on BUS
13. T0 = 0V
14. RESET = 0V and repeat from step 5
15. Programmer should be at conditions of step 1 when P8749H/48H is removed from socket.

NOTE:

Once programmed the P8749H/48H cannot be erased.

A.C. TIMING SPECIFICATION FOR PROGRAMMING P8748H/P8749H ONLY

$T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$; $V_{CC} = 5\text{V} \pm 5\%$; $V_{DD} = 21 \pm 0.5\text{V}$

Symbol	Parameter	Min	Max	Unit	Test Conditions
t_{AW}	Address Setup Time to <u>RESET</u>	$4t_{CY}$			
t_{WA}	Address Hold Time After <u>RESET</u>	$4t_{CY}$			
t_{DW}	Data in Setup Time to PROG	$4t_{CY}$			
t_{WD}	Data in Hold Time After PROG	$4t_{CY}$			
t_{PH}	<u>RESET</u> Hold Time to Verify	$4t_{CY}$			
t_{VDDW}	V_{DD} Hold Time Before PROG	0	1.0	ms	
t_{VDDH}	V_{DD} Hold Time After PROG	0	1.0	ms	
t_{PW}	Program Pulse Width	50	60	ms	
t_{TW}	T0 Setup Time for Program Mode	$4t_{CY}$			
t_{WT}	T0 Hold Time After Program Mode	$4t_{CY}$			
t_{DO}	T0 to Data Out Delay		$4t_{CY}$		
t_{WW}	<u>RESET</u> Pulse Width to Latch Address	$4t_{CY}$			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	100	μs	
t_{CY}	CPU Operation Cycle Time	3.75	5	μs	
t_{RE}	<u>RESET</u> Setup Time before EA	$4t_{CY}$			

NOTE:

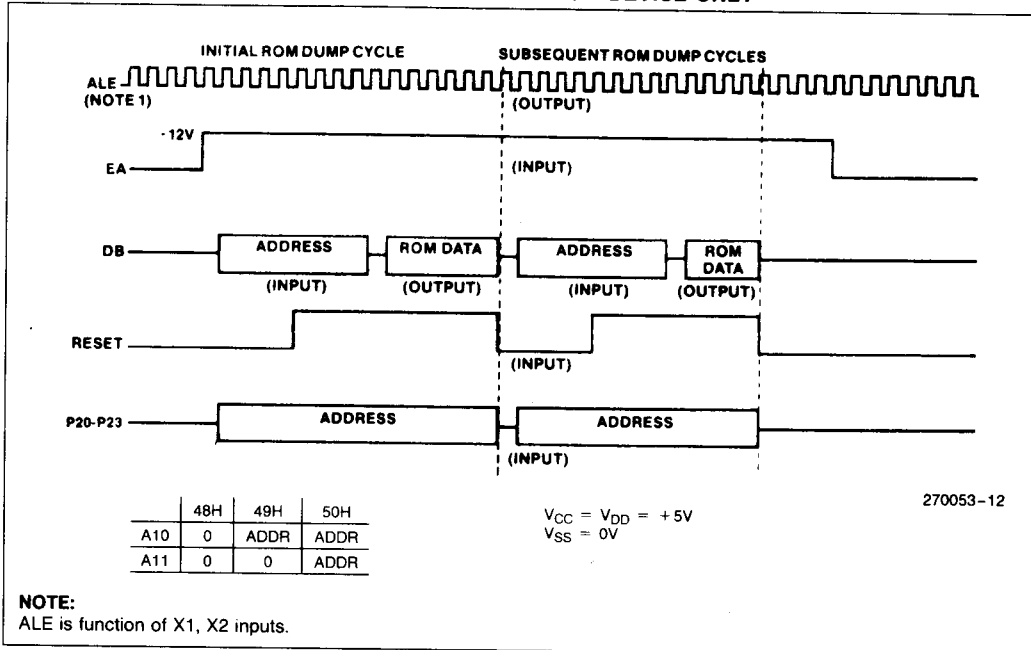
If Test 0 is high, t_{DO} can be triggered by RESET.

D.C. CHARACTERISTICS FOR PROGRAMMING P8748H/P8749H ONLY

$T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$; $V_{CC} = 5\text{V} \pm 5\%$; $V_{DD} = 21 \pm 0.5\text{V}$

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{DDH}	V_{DD} Program Voltage High Level	20.5	21.5	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	17.5	18.5	V	
V_{PL}	PROG Voltage Low Level	4.0	V_{CC}	V	
V_{EAH}	EA Program or Verify Voltage High Level	17.5	18.5	V	
I_{DD}	V_{DD} High Voltage Supply Current		20.0	mA	
I_{PROG}	PROG High Voltage Supply Current		1.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

SUGGESTED ROM VERIFICATION ALGORITHM FOR ROM DEVICE ONLY



NOTE:

ALE is function of X1, X2 inputs.

COMBINATION PROGRAM/VERIFY MODE (PROGRAMMABLE ROMS ONLY)

