

STEL-2105

Data Sheet

STEL-2105

**Digital Downconverter &
Bit Synchronizer/QPSK
Demodulator
For Cable Applications**

TABLE OF CONTENTS

FEATURES AND BENEFITS	3
BLOCK DIAGRAM.....	3
PACKAGE OUTLINE -- PLCC Package	4
PIN CONFIGURATION -- PLCC Package	4
PACKAGE OUTLINE -- TQFP Package	5
PIN CONFIGURATION -- TQFP Package	5
INTRODUCTION	6
FUNCTION BLOCKS – DESCRIPTION.....	7
Control and Microprocessor Interface Block.....	7
Local Oscillator NCO Block.....	7
Downconverter Block.....	7
Integrate and Dump Filter Block.....	7
Symbol Integrator Block.....	7
Symbol Timing Discriminator and Loop Filter Block.....	7
Symbol Timing NCO Block.....	8
Carrier Discriminator and Loop Filter Block.....	8
INPUT SIGNAL DESCRIPTIONS	9
OUTPUT SIGNAL DESCRIPTIONS	11
MODE CONTROL (WRITE) REGISTERS.....	12
STATUS (READ) REGISTERS	18
DECIMAL, HEX AND BINARY ADDRESS EQUIVALENTS	20
REGISTER SUMMARY: MODE CONTROL REGISTERS.....	21
REGISTER SUMMARY: STATUS REGISTERS.....	22
ELECTRICAL CHARACTERISTICS:	
ABSOLUTE MAXIMUM RATINGS.....	23
RECOMMENDED OPERATING CONDITIONS.....	23
D.C. CHARACTERISTICS.....	23
MICROPROCESSOR INTERFACE TIMING.....	24
INPUT/OUTPUT TIMING.....	25

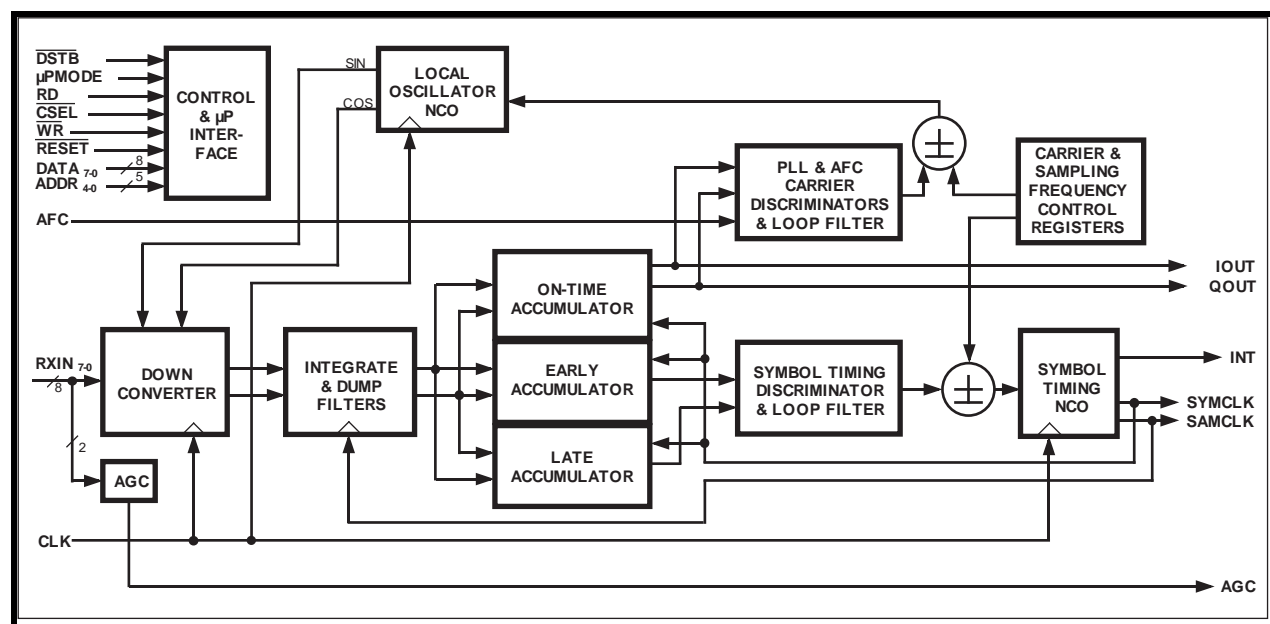
FEATURES

- Complete Digital CMOS QPSK Demodulator in a Single Package
- Fully programmable to operate up to 8 Mbps
- Includes Digital Downconverter
- Carrier Discriminator Operates in both PLL and AFC Modes
- Includes Carrier Tracking Oscillator with Second Order Loop Filter
- Includes Symbol Timing Discriminator and Oscillator
- Fully Programmable via Versatile Microprocessor Interface
- 68-Pin PLCC or 64-Pin TQFP Package Options

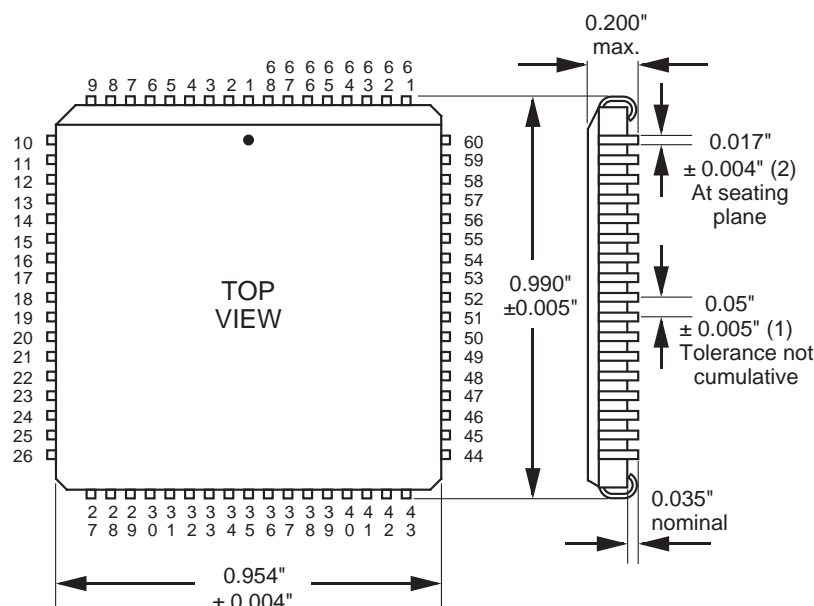
BENEFITS

- Low Power, High Reliability and Performance With Low Manufacturing Costs
- Programmable to Operate over a Wide Range of Data Rates Without Hardware Changes
- Permits Direct Sampling at I.F.
- Combines Fast Acquisition with Coherent Demodulation
- Minimizes Component Count and Adjustments in Production
- Very Accurate Symbol Timing with Minimum Clock Jitter
- No Hardware Changes Required when Changing Parameters
- Small Footprint, Surface Mount

BLOCK DIAGRAM



PACKAGE OUTLINE - 68-pin PLCC



Notes: (1) Tolerances on pin spacing are not cumulative

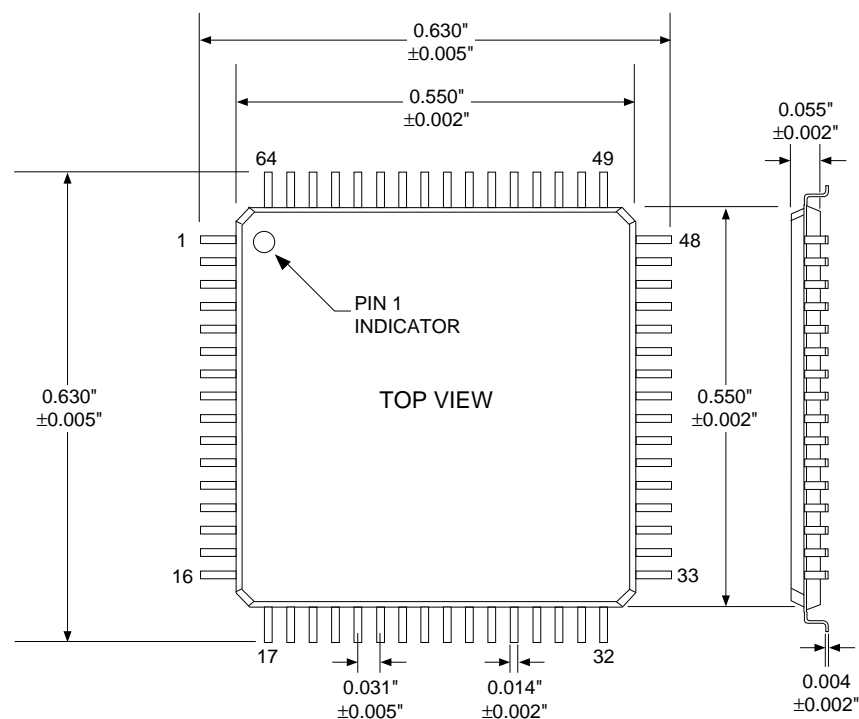
(2) Dimensions shown are at seating plane

(3) I.C. denotes Internal Connection. This pin *must* be left unconnected. **Do not use for vias.**

PIN CONFIGURATION

1	DATA ₇	18	V _{SS}	35	V _{SS}	52	V _{SS}
2	V _{SS}	19	RXIN ₇	36	V _{DD}	53	SYMCLK
3	V _{SS}	20	RXIN ₆	37	I.C.	54	V _{SS}
4	ADDR ₄	21	RXIN ₅	38	N.C.	55	V _{SS}
5	ADDR ₃	22	RXIN ₄	39	SAMCLK	56	I.C.
6	ADDR ₂	23	RXIN ₃	40	V _{SS}	57	V _{SS}
7	ADDR ₁	24	RXIN ₂	41	I.C.	58	AFC
8	ADDR ₀	25	RXIN ₁	42	N.C.	59	$\overline{\text{INT}}$
9	V _{DD}	26	RXIN ₀	43	V _{DD}	60	V _{DD}
10	V _{DD}	27	V _{DD}	44	V _{DD}	61	V _{DD}
11	$\overline{\text{CSEL}}$	28	I.C.	45	I.C.	62	DATA ₀
12	$\overline{\text{DSTB}}$	29	AGC	46	IOUT	63	DATA ₁
13	$\overline{\text{WR}}$	30	V _{SS}	47	I.C.	64	DATA ₂
14	$\overline{\text{RESET}}$	31	I.C.	48	I.C.	65	DATA ₃
15	$\overline{\text{RD}}$	32	V _{SS}	49	QOUT	66	DATA ₄
16	μPMODE	33	N.C.	50	I.C.	67	DATA ₅
17	CLK	34	N.C.	51	I.C.	68	DATA ₆

PACKAGE OUTLINE - 64-pin TQFP



WBP 54598.c-9/10/98

Notes: (1) Tolerances on pin spacing are not cumulative

(2) Dimensions shown are at seating plane

(3) I.C. denotes Internal Connection. This pin **must** be left unconnected. **Do not use for vias.**

(4) To order this package configuration, specify Model Number STEL-2105/CR

PIN CONFIGURATION

1	ADDR ₀	18	RXIN ₁	35	IOUT	52	DATA ₁
2	V _{DD}	19	RXIN ₀	36	I.C.	53	DATA ₂
3	V _{DD}	20	V _{DD}	37	I.C.	54	DATA ₃
4	CSEL	21	I.C.	38	QOUT	55	DATA ₄
5	DSTB	22	AGC	39	I.C.	56	DATA ₅
6	WR	23	V _{SS}	40	I.C.	57	DATA ₆
7	RESET	24	I.C.	41	V _{SS}	58	DATA ₇
8	RD	25	V _{SS}	42	SYMCLK	59	V _{SS}
9	μPMODE	26	V _{SS}	43	V _{SS}	60	V _{SS}
10	CLK	27	V _{DD}	44	V _{SS}	61	ADDR ₄
11	V _{SS}	28	I.C.	45	I.C.	62	ADDR ₃
12	RXIN ₇	29	SAMCLK	46	V _{SS}	63	ADDR ₂
13	RXIN ₆	30	V _{SS}	47	AFC	64	ADDR ₁
14	RXIN ₅	31	I.C.	48	INT		
15	RXIN ₄	32	V _{DD}	49	V _{DD}		
16	RXIN ₃	33	V _{DD}	50	V _{DD}		
17	RXIN ₂	34	I.C.	51	DATA ₀		

INTRODUCTION

The STEL-2105 is a single ASIC which performs all the digital processing required to implement a coherent BPSK or QPSK demodulator. The device implements all of the commonly used functions performed by the STEL-2130A Digital downconverter and the STEL-2110A Bit Synchronizer and PSK Demodulator ASICs. The STEL-2105 is designed specifically for CATV applications and provides an extremely low-cost solution for the demodulation of QPSK signals at the set-top decoder box.

The STEL-2105 operates at up to 4 Mbps in BPSK mode and 8 Mbps in QPSK mode. It includes two Numerically Controlled Oscillators (NCOs), one as the local oscillator for carrier tracking and one as the symbol timing generator. The local oscillator NCO generates a quadrature signal which is mixed with the input signal in a complex multiplier to perform down-conversion directly from I.F. to baseband. A single ADC is used to digitize the input signal, as described in the applications section. The I.F. frequency is not limited by the capabilities of the STEL-2105 but by the track-and-hold capabilities of the ADC selected. Signals at I.F. frequencies up to about 100 MHz can be processed by currently available 8-bit ADCs, but the implementation cost, as well as the performance, can be improved by using I.F. frequencies in the 30 MHz region or lower. The output of the downconverter is then filtered with Integrate and Dump filters. These have a $\sin(x)/x$ characteristic which is a function of the number of samples integrated in each dump cycle. The primary purpose of these filters is to allow the device to operate over a wide range of data rates using a constant sampling rate, thereby eliminating the need to

change the anti-aliasing filter for each sampling rate. The output rate of the Integrate and Dump filters should be set to four samples per symbol to permit correct operation of the symbol timing circuit.

Symbol timing and clock recovery is performed by integrating the four signal samples over a symbol period using early and late integration relative to the on-time signal used for the data. By integrating the samples one quarter of a symbol early and late a discrimination function is obtained which goes to zero when the timing is correct, and this signal is used to drive the symbol timing NCO via a loop filter. The loop filter parameters are completely programmable and can be changed during operation, allowing the parameters to be optimized for fast acquisition and tracking as well as maximum stability.

The carrier discriminator will generate both frequency tracking (AFC) and phase tracking (PLL) functions. The loop filter is programmable to operate with both types of loops. This allows the device to be set up for frequency tracking for fast carrier acquisition and then switched to phase tracking for coherent demodulation. A lock indicator function is provided to allow the switch over to be done at the optimum time. The I and Q channel outputs of the on-time integrator are provided as the I and Q output bits.

The STEL-2105 is completely programmable via the microprocessor interface. This interface has been made very flexible to optimize direct interconnect with a wide range of 8-bit microprocessors and microcomputer devices.

FUNCTION BLOCKS – DESCRIPTION

Control and Microprocessor Interface Block

Most of the functions of the STEL-2105 are programmed via the Control and Microprocessor Interface Block. The setup and parameter information is written into the twenty five 8-bit on-chip registers via the microprocessor interface, and the contents of the twenty one 8-bit status registers are also read out in this way. The microprocessor interface has been designed for optimum interconnection to most of the 8-bit microprocessors and microcontrollers available.

Local Oscillator NCO Block

The STEL-2105 incorporates a Numerically Controlled Oscillator (NCO) to synthesize a local oscillator signal for the downconverter. The NCO is clocked with the master clock signal, **CLK**. The NCO has 32-bit frequency resolution and generates 8-bit quadrature outputs. The frequency is controlled by the data stored in the 32-bit Carrier Frequency Control Register as 4 bytes at addresses 10_H to 13_H. The output of the Carrier Tracking Loop Filter is added to or subtracted from this data to form the actual frequency control information.

The frequencies of the Symbol Timing NCO and the Local Oscillator NCO are both updated once every symbol period during normal operation. However, until the nominal symbol period information has been written into the Symbol Timing NCO after a reset no automatic updates will occur since the symbol frequency will be set to zero. It is therefore necessary to manually load the Symbol Timing NCO frequency after a reset by setting bit 0 high. This will load both NCOs. Bit 0 will automatically reset itself when this is done.

Downconverter Block

The STEL-2105 incorporates a Half Quadrature (Double Sideband) Downconverter which allows the received signal to be sampled and digitized directly at IF and converted to baseband digitally. The downconverter includes two multipliers in which the 8-bit receiver input signal is multiplied by the sine and cosine signals from the NCO. All operations in the downconverter are controlled by the main clock signal, **CLK**. In conjunction with the built-in frequency tracking loop, this permits the received signal to be downconverted accurately to baseband. The input signal can be accepted in either Two's Complement or Offset Binary formats according to the setting of bit 2 in address 14_H.

The outputs of the multipliers are:

$$I_{OUT} = RXIN \cdot \cos(wt)$$

$$Q_{OUT} = RXIN \cdot \sin(wt)$$

$$\text{where } w = 2\pi f_{NCO}$$

These are fed into the I and Q channel Integrate and Dump Filters.

Integrate and Dump Filter Block

These filters integrate the downconverted samples over the number of sample periods determined by the dump rate. The dump rate is controlled by the Symbol Timing NCO such that either four or five samples at the dump rate occur in each symbol period, as determined by the setting of bit 0 in address 16_H. These samples are then fed into the Symbol Integrator Block. Since the accumulation process increases the magnitudes of the signal values a selectable viewport is provided at the outputs of the Integrate and Dump Filters to allow the optimum output bits to be selected for the 8-bit inputs of the Symbol Integrator Block. The viewport is controlled by the data stored in bits 3-0 in address 00_H.

Symbol Integrator Block

The I and Q symbol information is generated in the Symbol Integrator Block by integrating the input samples over one symbol period, which corresponds to four or five sample periods, as determined by the setting of bit 0 in address 16_H. The symbol timing discriminator function is derived by repeating the integration process one sample early and one sample late relative to the nominally on-time integration, and these signals are fed into the Symbol Timing Discriminator and Loop Filter Block. The outputs of the I and Q channel on-time integrators are the output symbols, and two selectable viewports are provided to select the optimum 8-bit values fed into the Carrier Discriminator and Loop Filter Block. The signs of these outputs are the output data bits available at the **IOUT** and **QOUT** pins.

Symbol Timing Discriminator and Loop Filter Block

The symbol timing discriminator function is generated from the difference between the sums of the absolute I and Q values of the early and late integrations from the Symbol Integrator Block.

$$\text{i.e., } \{Abs(I_{late}) + Abs(Q_{late})\} - \{Abs(I_{early}) + Abs(Q_{early})\}$$

This is a linear function of the symbol timing error that

goes to zero when the on-time signal is optimally timed. The computation of the symbol timing discriminator results in a 12-bit signal, and a selectable viewport is provided to allow the appropriate output bits to be selected for the 8-bit input of the Symbol Timing Loop Filter. The viewport is controlled by the data stored in bits 2-0 in address 01_H.

The Loop Filter transfer function can be set up to be either first or second order and the coefficient values can be adjusted in powers of 2 from 2⁰ to 2²¹. The overall transfer function is:

$$\text{Transfer Fn.} = K1 + \frac{1}{4} K2 \cdot \frac{z^{-1}}{1 - z^{-1}}$$

The 1/4 factor is introduced because the signal in the integrator path of the loop is divided by four after the integrator by truncating the 2 LSBs of the signal. This signal is then added to the signal in the direct path such that the LSBs of the signals are aligned. The coefficients K1 and K2 are determined by the data stored in bits 4-0 in addresses 0B_H and 0A_H, respectively. K1 and K2 can also be set to zero individually by setting bits 2 or 3, respectively, high in address 05_H, giving the user full control of the loop filter characteristics. In addition, the value of the accumulator output in the K2 path of the loop filter can be forced to limit at a boundary (which applies to both positive and negative accumulated values) set by the data stored in bits 3-0 in addresses 06_H. The boundary function can be enabled or disabled, according to the setting of bit 0 in address 15_H.

Symbol Timing NCO Block

The STEL-2105 incorporates a Numerically Controlled Oscillator (NCO) to synthesize a sampling clock which is used as the dump function of the Integrate and Dump Filters in the Downconverter block. This clock is further divided by four or five, according to the setting of bit 0 in address 16_H, to provide the symbol clock output, **SYMCLK**, so that the sampling rate of the signal is synchronized to the symbol rate for all further processing. The NCO is clocked with the master clock signal, **CLK**. The NCO has 32-bit frequency resolution and the effective length of the accumulator is extended to 39 bits by means of an additional 7-bit divider. This extends the lower end of the frequency range of the sampling clock by an additional seven octaves, thereby allowing the STEL-2105 to operate at very low data rates while maintaining high resolution in the sampling rate control. The sampling clock is derived from one of the eight most significant phase bits of the NCO, according to the data stored in

bits 3-1 of addresses 16_H. Normally the MSB of the accumulator itself (Bit 31) is used as the clock. Selecting successively higher order bits results in the clock frequency being reduced by a factor of two each time, and the frequency control word should be increased accordingly to compensate for this. The frequency of the NCO is controlled by the data stored in the 32-bit Sampling Frequency Control Register as 4 bytes at addresses 0C_H to 0F_H. The output of the Symbol Timing Loop Filter is added to or subtracted from this data to form the actual sampling rate control information.

The frequencies of the Symbol Timing NCO and the Local Oscillator NCO are both updated once every symbol period during normal operation. However, until the nominal symbol period information has been written into the Symbol Timing NCO after a reset no automatic updates will occur since the symbol frequency will be set to zero. It is therefore necessary to manually load the Symbol Timing NCO frequency after a reset by setting bit 0 high. This will load both NCOs. Bit 0 will automatically reset itself when this is done.

Carrier Discriminator and Loop Filter Block

The carrier frequency discriminator functions are decision directed values derived from the I and Q signals. These are used to generate AFC (frequency tracking) and PLL (phase tracking) signals for the frequency acquisition and tracking loop filter. The algorithm used depends on the signal type, which is controlled by the setting of bit 7 in address 14_H, as well as the state of the **AFC** input, which determines whether the AFC or PLL tracking mode is used.

When the **AFC** input signal is set high the device will operate in the AFC mode. In this mode the dot and cross products of I and Q are generated. These are the real and imaginary results of the complex multiplication of the current and previous symbols

If bit 7 is set low the discriminator circuit is set into the QPSK/AFC mode, using the following algorithm to compute the carrier discriminator function, CD:

$$CD = (\text{Cross} \times \text{Sign}[\text{Dot}]) - (\text{Dot} \times \text{Sign}[\text{Cross}])$$

The computation of the AFC discriminator results in an 18-bit signal which is sign-extended to form a 19-bit

value. A selectable viewport is provided to allow the appropriate output bits to be selected for the 8-bit input of the Loop Filter. This viewport is controlled by the data stored in bits 3-0 in address 04_H.

When the **AFC** input signal is set low the device will operate in the PLL mode

If bit 7 is set low the discriminator circuit is set into the QPSK/PLL mode. In this mode it is necessary to set the carrier phase rotation to -45° by setting bits 3 and 2 in address 15_H to 11. The following algorithm is then used to compute the carrier discriminator function, CD, using rotated versions, I_{rot} and Q_{rot} , of I and Q:

Polarity of		CD
I	Q	
+	+	$-I_{rot}$
-	+	Q_{rot}
-	-	I_{rot}
+	-	$-Q_{rot}$

The PLL discriminator output is an 8-bit value which, therefore, does not require scaling before being fed into the Loop Filter.

The Loop Filter transfer function can be set up to be either first or second order and the coefficient values can be adjusted in powers of 2 from 2^0 to 2^{21} . The overall transfer function is:

$$\text{Transfer Fn.} = K1 + \frac{1}{4} K2 \cdot \frac{z^{-1}}{1 - z^{-1}}$$

The $\frac{1}{4}$ factor is introduced because the signal in the integrator path of the loop is divided by four after the integrator by truncating the 2 LSBs of the signal. This signal is then added to the signal in the direct path such that the LSBs of the signals are aligned. The coefficients K1 and K2 are determined by the data stored in bits 4-0 in addresses 09_H and 08_H, respectively. K1 and K2 can both be set to zero individually by setting bits 0 or 1, respectively, high in address 05_H, giving the user full control of the loop filter characteristics.

INPUT SIGNAL DESCRIPTIONS

$\overline{\text{RESET}}$ (Pin 14)

The **$\overline{\text{RESET}}$** input provides the master reset function for the STEL-2100A. When is set low it will reset the mode control registers, as well as the signals in all the data paths, to zero. Normal operation of the circuit will resume when **$\overline{\text{RESET}}$** returns to the high state.

CLK (Pin 17)

The **CLK** input is the master system clock. With the exception of the generation of the **AGC** output, all internal operations occur, and all output signals change, on the rising edges of **CLK**. This signal should nominally be a square wave with a maximum frequency is 36 MHz.

RXIN₇₋₀ (Pins 19 - 26)

The **RXIN₇₋₀** input is an 8-bit port for signals from an external A/D converter. The data may be in either Two's Complement or Offset Binary format, according to the setting of bit 2 in address 14_H. The data on this input is latched in on the rising edges of **CLK**.

AFC (Pin 58)

In the **STEL-2100A**, carrier discrimination can be achieved either by frequency or phase discrimination. The frequency discriminator uses the dot and cross products of the I and Q signals to generate the AFC

error for the frequency acquisition and tracking loop. The phase discriminator computes the PLL error from either the in-phase or the quadrature-phase data in QPSK mode of operation. The PLL error can be inverted by setting bit 4 of address 20 to a logic low value. The algorithm used in both methods depends on the signal type and is controlled by bit 7 of address 20. When the AFC input is set high the frequency discriminator is selected. When it is set low the phase lock loop is selected.

DATA₇₋₀ (Pins 1, 68 - 62)

The 8-bit bi-directional **DATA₇₋₀** bus is the micro-processor interface bus that provides access to the internal registers. **DATA₇₋₀** is used in conjunction with the **ADDR₄₋₀**, **$\overline{\text{WR}}$** , **$\overline{\text{DSTB}}$** and **$\overline{\text{RD}}$** signals to set the values of the mode control registers and to read internal status information. Please refer to the Mode Configuration map (write mode register) and the Internal Status map (read mode register) for more details.

ADDR₄₋₀ (Pins 4 - 8)

ADDR₄₋₀ is a 5-bit address bus that selects the mode control register location into which the information provided on the **DATA₇₋₀** bus will be written. **ADDR₄₋₀** is used in conjunction with **$\overline{\text{WR}}$** and **DATA₇₋₀** to write the information into the registers.

$\overline{\text{CSEL}}$ (Pin 11)

The chip select function input, $\overline{\text{CSEL}}$, is provided to enable or disable the microprocessor operation of the STEL-2100A. When $\overline{\text{CSEL}}$ is set high the ADDR_{4-0} and $\overline{\text{WR}}$ become disabled and have no effect on the device. When $\overline{\text{CSEL}}$ is set low the device is in its normal mode of operation and ADDR_{4-0} and $\overline{\text{WR}}$ are active.

μPMODE (Pin 16)

When μPMODE is set low, the device is configured to interface with microprocessors that require an interface using a Read/ $\overline{\text{Write}}$ signal and a Data Strobe, e.g., Z80, 68xx. In this mode, $\overline{\text{WR}}$ and $\overline{\text{DSTB}}$ control the read and write functions, with $\overline{\text{WR}}$ performing the Read/ $\overline{\text{Write}}$ function. When μPMODE is set high, the device is configured to interface with microprocessors that require an interface using separate read and write signals, e.g., i 80XX. In this mode the write operation is controlled by the $\overline{\text{WR}}$ signal and the read operation by the $\overline{\text{RD}}$ signal. In this case, $\overline{\text{DSTB}}$ is not used and should be tied low.

$\overline{\text{WR}}$ (Pin 13)

When μPMODE is set low, $\overline{\text{WR}}$ is used to enable write or read functions of the microprocessor. In this mode, $\overline{\text{DSTB}}$ is used to latch information into the mode

control registers when $\overline{\text{WR}}$ is low. The mode control registers are transparent latches while $\overline{\text{DSTB}}$ is low and the information will be latched when $\overline{\text{DSTB}}$ returns high. When $\overline{\text{WR}}$ is high, internal status information is available on the DATA_{7-0} bus when $\overline{\text{DSTB}}$ is low. When μPMODE is set high, $\overline{\text{DSTB}}$ should always be grounded, and $\overline{\text{WR}}$ is used to latch information into the mode control registers. In this mode, the read operation is controlled by the $\overline{\text{RD}}$ pin.

$\overline{\text{RD}}$ (Pin 15)

Read Bar. When μPMODE is set low, $\overline{\text{RD}}$ is not used and should be tied low. When μPMODE is set high, $\overline{\text{RD}}$ is used to read data from the DATA_{7-0} bus.

$\overline{\text{DSTB}}$ (Pin 12)

Data Strobe Bar. When μPMODE is low, $\overline{\text{DSTB}}$ is used to write data into the write registers when $\overline{\text{WR}}$ is low and to read data from the read register when $\overline{\text{WR}}$ is high. When μPMODE is set high, $\overline{\text{DSTB}}$ should be tied low.

OUTPUT SIGNAL DESCRIPTIONS

IOUT, QOUT (Pins 46, 49)

These are the in-phase and quadrature-phase output signals, respectively. They represent the signs of the internal 11-bit outputs of the on-time accumulators..

SAMCLK (Pin 39)

The **SAMCLK** output is the internal sampling clock signal which is used as the dump clock in the Integrate and Dump Filter Block. **SAMCLK** is generated from one of the MSBs of the phase output of the Symbol Timing NCO, according to the data programmed into bits 3-1 in address 16_H. There will be four or five cycles of **SAMCLK** for each cycle of **SYMCLK**, according to the data programmed into bit 0 in address 16_H.

SYMCLK (Pin 53)

The **SYMCLK** output is a clock occurring at the symbol rate. This period is equal to four cycles of

the sample clock, **SAMCLK**, with a 50% duty cycle. The falling edges of this signal can be used to strobe the **IOUT** and **QOUT** data.

AGC (Pin 29)

This is the AGC indicator output. **AGC** serves as a measure of the signal amplitude of the signal input,

RXIN₇₋₀. This is done by comparing the top two MSBs of **RXIN**. Using the internal Two's Complement format, whenever these bits are equal is an indication that the magnitude of the current sample is less than one half the peak value, as determined by the saturation limits of the Analog to Digital Converter. Consequently, when the input signal level is high the two MSBs will be different during some signal sample periods, and by integrating the **AGC** pulses an AGC control signal can be obtained. The polarity of the **AGC** function is programmable via bit 3 of address 14_H. If this bit is set high then **AGC** will normally be set low and will pulse high during sample periods when the sample amplitudes are higher than one half of the peak value. If this bit is set low then the **AGC** output will be logically inverted. This signal is asynchronous with respect to the **CLK**, its timing is directly related to the edges of **RXIN₇** and **RXIN₆**.

$\overline{\text{INT}}$ (Pin 59)

The $\overline{\text{INT}}$ output will pulse low for two **SYMCLK** cycles every 64 cycles of **SYMCLK**, indicating that the value of **SYMLOCK** in the Symbol Lock Indicator Register at address 15_H has been updated. This signal can be used as an interrupt to the microprocessor to read the new value of **SYMLOCK**.

MODE CONTROL (WRITE) REGISTERS

Address 00_H:

Bits 0 through 3 -- Integrate and Dump Filter Viewport Control

The magnitudes of the signals in the Integrate and Dump Filters in the Downconverter section increases as the number of accumulations is increased, so that the word-length of the outputs signals can reach 17 bits. The STEL-2105 incorporates a data selector circuit to select any eight consecutive bits from the 17-bit output of the I & D Filters for processing in the Symbol Integrator Block. The significance of this 8 bit value is determined by the data loaded into bits 3-0 in address 00_H. The resulting 8 bit value provided to the Matched Filter will be equivalent to the 17 bit value divided by 2^n , where n = the unsigned value of bits 3-0.

Bits 3-0 control the viewport of the Integrate and Dump filter outputs as shown in Table 1:

Bits 3-0	I & D bits output to Symbol Int. Block
0 _H	7-0
1 _H	8-1
2 _H	9-2
3 _H	10-3
.....
.....
8 _H	15-8
9 _H	16-9

Table 1. Integrate & Dump Filter Viewport Control

If I and Q are larger than the range specified by the scale factor, I and Q will be saturated to the maximum or minimum values of the 8-bit number, i.e., 7F_H or 80_H.

Address 01_H:

Bits 0 through 2 -- Symbol Timing Discriminator Viewport Control

The Symbol Timing Discriminator produces a 12-bit symbol timing error, E, as follows:

$$E = \{ \text{Abs}(I_{\text{late}}) + \text{Abs}(Q_{\text{late}}) \} - \{ \text{Abs}(I_{\text{early}}) + \text{Abs}(Q_{\text{early}}) \}$$

where I_{late} and Q_{late} are the accumulated late values of I and Q over four or five samples, according to the setting of bit 0 in address 16_H, and I_{early} and Q_{early} are the corresponding early values. This 12-bit value is extended to 13 bits by sign extension. The STEL-2105

incorporates a data selector circuit to select any eight consecutive bits from the 13-bit output of the Symbol Timing Discriminator for processing in the Symbol Integrator Loop Filter. The significance of this 8 bit value is determined by the data loaded into bits 2-0 in address 01_H. The resulting 8 bit value provided to the Matched Filter will be equivalent to the 13 bit value divided by 2^n , where n = the unsigned value of bits 2-0.

Bits 2-0 control the viewport of the Symbol Timing Discriminator output as shown in Table 2:

Bits 3-0	Discriminator bits output to Loop Filter
0 _H	7-0
1 _H	8-1
2 _H	9-2
3 _H	10-3
4 _H	11-4
5 _H	12-5

Table 2. Symbol Timing Discriminator Viewport Control

If the output is larger than the range specified by the scale factor, it will be saturated to the maximum or minimum values of the 8-bit number, i.e., 7F_H or 80_H.

Address 02_H:

Bits 0 through 3 -- Symbol Lock Accumulator Viewport Control

The symbol lock function, is computed by accumulating the following function over a period of 64 symbols:

$$\text{SYMLOCK} = \sum_{0}^{63} \{ I + Q_{\text{on-time}} - 9/16 \{ I + Q_{\text{late}} + I + Q_{\text{early}} \} \}$$

where $I + Q_{\text{(time)}} = I_{\text{(time)}} + Q_{\text{(time)}}$

and (time) = on-time, late or early, as appropriate

SYMLOCK is calculated to an accuracy of 19 bits. The STEL-2105 incorporates a data selector circuit to select any eight consecutive bits from the 19-bit SYMLOCK output and makes it available in the Symbol Lock Indicator Register at address 15_H. The significance of this 8 bit value is determined by the data

loaded into bits 3-0 in address 02_H. The resulting 8 bit value written into the Symbol Lock Indicator Register will be equivalent to the 19 bit value divided by 2^n , where n = the unsigned value of bits 3-0.

Bits 3-0 control the viewport of the Symbol Lock Accumulator output as shown in Table 3:

Bits 3-0	SYMLOCK bits output to Register
0 _H	7-0
1 _H	8-1
2 _H	9-2
3 _H	10-3
.....
.....
8 _H	15-8
9 _H	16-9
A _H	17-10
B _H	18-11

Table 3. Symbol Lock Accumulator Viewport Control

If the output is larger than the range specified by the scale factor, it will be saturated to the maximum or minimum values of the 8-bit number, i.e., 7F_H or 80_H

Address 03_H:

Bits 0 and 1 -- On-Time Symbol Integrator Viewport Control

The 11-bit outputs of the On-time I and Q Channel Accumulators in the Symbol Integrator Block are used as the inputs for the Carrier Discriminator function. The STEL-2105 incorporates data selector circuits to select any eight consecutive bits from the 11-bit outputs of the On-time Accumulators for processing in the Carrier Discriminator. The significance of this 8 bit value is determined by the data loaded into bits 1-0 in address 03_H. The resulting 8 bit value provided to the Carrier Discriminator will be equivalent to the 11-bit value divided by 2^n , where n = the unsigned value of bits 1-0.

Bits 1-0 control the viewport of the On-time Symbol Integrator Block output as shown in Table 4:

Bits 1-0	On-Time Acc. bits output to Carr. Disc.
0 _H	7-0
1 _H	8-1
2 _H	9-2
3 _H	10-3

Table 4. On-Time Symbol Integrator Viewport Control

If the output is larger than the range specified by the scale factor, it will be saturated to the maximum or minimum values of the 8-bit number, i.e., 7F_H or 80_H.

Address 04_H:

Bits 0 through 3 -- AFC Discriminator Viewport Control

When the AFC input signal is set high the Carrier Discriminator will operate in the AFC mode. In this mode the dot and cross products of I and Q are generated. These are the real and imaginary results of the complex multiplication of the current and previous symbols.

If bit 7 is set low the discriminator circuit is set into the QPSK/AFC mode, using the following algorithm to compute the carrier discriminator function, CD:

$$CD = (Cross \times Sign[Dot]) - (Dot \times Sign[Cross])$$

The computation of the AFC discriminator results in an 18-bit signal which is sign-extended to form a 19-bit value. The STEL-2105 incorporates a data selector circuit to select any eight consecutive bits from the 19-bit CD output for processing in the Carrier Tracking Loop Filter. The significance of this 8 bit value is determined by the data loaded into bits 3-0 in address 04_H. The resulting 8 bit value provided to the Loop Filter will be equivalent to the 19 bit value divided by 2^n , where n = the unsigned value of bits 3-0.

Bits 3-0 control the viewport of the AFC Discriminator output as shown in Table 5:

Bits 3-0	AFC bits output to Loop Filter
0 _H	7-0
1 _H	8-1
2 _H	9-2
3 _H	10-3
.....
.....
8 _H	15-8
9 _H	16-9
A _H	17-10
B _H	18-11

Table 5. AFC Discriminator Viewport Control

If the output is larger than the range specified by the scale factor, it will be saturated to the maximum or minimum values of the 8-bit number, i.e., 7F_H or 80_H

Address 05_H:

Bit 0 -- K1 Off in Carrier Tracking Loop Filter

Setting this bit high will set the value of K1 in the Carrier Tracking Loop Filter to zero, thereby disabling the first order path in this loop filter.

Bit 1 -- K2 Off in Carrier Tracking Loop Filter

Setting this bit high will set the value of K2 in the Carrier Tracking Loop Filter to zero, thereby disabling the second order path in this loop filter.

Bit 2 -- K1 Off in Symbol Timing Tracking Loop Filter

Setting this bit high will set the value of K1 in the Symbol Timing Tracking Loop Filter to zero, thereby disabling the first order path in this loop filter (AFC Mode).

Bit 3 -- K2 Off in Symbol Timing Tracking Loop Filter

Setting this bit high will set the value of K2 in the Symbol Timing Tracking Loop Filter to zero, thereby disabling the second order path in this loop filter.

Address 06_H:

Bits 0 through 3 -- Symbol Timing Tracking Loop Filter Accumulator Boundary

The output of the accumulator in the K2 path of the

Symbol Timing Tracking Loop Filter is provided with a programmable boundary circuit which prevents the magnitude of the output value from exceeding the set boundary. This function is normally disabled and can be enabled by setting bit 0 in address 15_H high. Bits 0 to 4 in address 06_H set the boundary value according to the following equations:

Positive boundary value = 2^{n+15}

Negative boundary value = $2^{31} + 2^{n+15}$

where n is the 5 bit Boundary Value

The magnitude values may range from 00 00 80 00_H to 40 00 00 00_H, as shown in Table 6:

Bits 3-0	Accumulator Output Value Range (- to +)
0 _H	80 00 80 00 _H to 00 00 80 00 _H
1 _H	80 01 00 00 _H to 00 01 00 00 _H
2 _H	80 02 00 00 _H to 00 02 00 00 _H
3 _H	80 04 00 00 _H to 00 04 00 00 _H
.....
.....
C _H	88 00 00 00 _H to 08 00 00 00 _H
D _H	90 00 00 00 _H to 10 00 00 00 _H
E _H	A0 00 00 00 _H to 20 00 00 00 _H
F _H	C0 00 00 00 _H to 40 00 00 00 _H

Table 6. Symbol Timing Tracking Loop Filter Accumulator Bounded Values

Address 07_H:

Bits 0 through 3 -- Carrier Tracking Loop Filter Accumulator Boundary

The output of the accumulator in the K2 path of the Carrier Tracking Loop Filter is provided with a programmable boundary circuit which prevents the magnitude of the output value from exceeding the set boundary. This function is normally disabled and can be enabled by setting bit 1 in address 15_H high. Bits 0 to 4 in address 07_H set the boundary value according to the following equations:

Positive boundary value = 2^{n+15}

Negative boundary value = $2^{31} + 2^{n+15}$

where n is the 5 bit Boundary Value

The magnitude values may range from 00 00 80 00_H to 40 00 00 00_H, as shown in Table 7:

Bits 3-0	Accumulator Output Value Range (– to +)
0 _H	80 00 80 00 _H to 00 00 80 00 _H
1 _H	80 01 00 00 _H to 00 01 00 00 _H
2 _H	80 02 00 00 _H to 00 02 00 00 _H
3 _H	80 04 00 00 _H to 00 04 00 00 _H
.....
.....
C _H	88 00 00 00 _H to 08 00 00 00 _H
D _H	90 00 00 00 _H to 10 00 00 00 _H
E _H	A0 00 00 00 _H to 20 00 00 00 _H
F _H	C0 00 00 00 _H to 40 00 00 00 _H

Table 7. Carrier Tracking Loop Filter Accumulator Bounded Values

Address 08_H:

Bits 0 through 4 -- K2 Gain Value in Carrier Tracking Loop Filter

Bits 0 to 4 control the gain factor K2 of the second order Carrier Tracking Loop Filter path. The gain factor multiplies the signal before the accumulator by the value of 2^n , where n is the 5 bit K2 Gain Value.

The value of n may range from 0 to 21 (15_H), as shown in Table 8:

Bits 4-0	Gain in K2 Path
00 _H	2^0
01 _H	2^1
.....
.....
14 _H	2^{20}
15 _H	2^{21}

Table 8. K2 Gain Values

Address 09_H:

Bits 0 through 4 -- K1 Gain Value in Carrier Tracking Loop Filter

Bits 0 to 4 control the gain factor K1 of the first order Carrier Tracking Loop Filter path. The gain factor multiplies the signal before the accumulator by the value of 2^n , where n is the 5 bit K1 Gain Value.

The value of n may range from 0 to 21 (15_H), as shown in Table 9:

Bits 4-0	Gain in K1 Path
00 _H	2^0
01 _H	2^1
.....
.....
14 _H	2^{20}
15 _H	2^{21}

Table 9. K1 Gain Values

Address 0A_H:

Bits 0 through 4 -- K2 Gain Value in Symbol Timing Tracking Loop Filter

Bits 4 to 0 control the gain factor K2 of the second order Symbol Timing Tracking Loop Filter path. The gain factor multiplies the signal before the accumulator by the value of 2^n , where n is the 5 bit K2 Gain Value.

The value of n may range from 0 to 21 (15_H), as shown in Table 10:

Bits 4-0	Gain in K2 Path
00 _H	2^0
01 _H	2^1
.....
.....
14 _H	2^{20}
15 _H	2^{21}

Table 10. K2 Gain Values

Address 0B_H:

Bits 0 through 4 -- K1 Gain Value in Symbol Timing Tracking Loop Filter

Bits 4 to 0 control the gain factor K1 of the first order Symbol Timing Tracking Loop Filter path. The gain factor multiplies the signal before the accumulator by the value of 2^n , where n is the 5 bit K1 Gain Value.

The value of n may range from 0 to 21 (15_H), as shown in Table 11:

Bits 4-0	Gain in K1 Path
00 _H	2 ⁰
01 _H	2 ¹
....
....
14 _H	2 ²⁰
15 _H	2 ²¹

Table 11. K1 Gain Values

Addresses 0C_H through 0F_H: Symbol Timing NCO Frequency Control Word

The internal Symbol Timing NCO is driven by a frequency control word that is the sum of the timing discriminator error value (generated in the demodulator) and the 32-bit frequency control word stored in this location (FCW). The four 8-bit registers at addresses 0C_H through 0F_H are used to store the 32-bit frequency control word as shown in Table 12. The LSB of each byte is stored in bit 0 of each register.

ADDR _{0F_H}	ADDR _{0E_H}	ADDR _{0D_H}	ADDR _{0C_H}
Bits 31-24	Bits 23-16	Bits 15-8	Bits 7-0

Table 12. Symbol Timing NCO FCW Storage

Addresses 10_H through 13_H: Local Oscillator NCO Frequency Control Word

The internal Local Oscillator NCO is driven by a frequency control word that is the sum of the frequency discriminator error value (generated in the demodulator) and the 32-bit frequency control word stored in this location (FCW). The four 8-bit registers at addresses 10_H through 13_H are used to store the 32-bit frequency control word as shown in Table 13. The LSB of each byte is stored in bit 0 of each register.

ADDR _{13_H}	ADDR _{12_H}	ADDR _{11_H}	ADDR _{10_H}
Bits 31-24	Bits 23-16	Bits 15-8	Bits 7-0

Table 13. Local Oscillator NCO FCW Storage

Address 14_H:

Bit 0 -- Unused

This bit should be set to 1 for normal operation.

Bit 1 -- Unused

This bit should be set to 0 for normal operation.

Bit 2 -- Two's Complement Input Select

The **RXIN**₇₋₀ input signal can be in either Two's Complement or Offset Binary formats. Since all internal processing in the device operates on Two's Complement format signals it is necessary to convert the **RXIN**₇₋₀ inputs when they are in the Offset Binary format by inverting the MSBs.

When bit 2 in address 14_H is set high the device expects Two's Complement format inputs on **RXIN**₇₋₀. When it is set low the device expects Offset Binary format on **RXIN**₇₋₀. In Two's Complement the 8 bit input values range from -128 to +127 (80_H to 7F_H). In Offset Binary, the values range from 0 to +255 (00_H to FF_H).

Bit 3 -- Set-AGC-True

This the AGC function is computed by comparing the top two MSBs of **RXIN**₇₋₀. The polarity of the **AGC** function is programmable via bit 3. If bit 3 in address 14_H is set low then **AGC** will normally be set low and will pulse high during sample periods when the sample amplitudes are higher than one half of the peak value. If this bit is set high then the **AGC** output will be logically inverted.

Bit 4 -- Unused

This bit should be set to 0 for normal operation.

Bit 5 -- Unused

This bit should be set to 1 for normal operation.

Bit 6 -- Subtract Carrier Error

The carrier frequency error signal from the Carrier Tracking Loop Filter can be added to or subtracted from the data stored in the Carrier Frequency Control Register to form the actual frequency control information for the Local Oscillator NCO. Setting bit 6 in address 14_H high causes the frequency error signal to be subtracted, and setting it low causes it to be added.

Bit 7 -- Unused

This bit should be set to 0 for normal operation.

Address 15_H:

Bits 0 -- Symbol Timing Tracking Loop Filter Accumulator Boundary Enable

The output of the accumulator in the K2 path of the Symbol Timing Tracking Loop Filter is provided with a programmable boundary circuit which prevents the magnitude of the output value from exceeding the set boundary. This function is normally disabled and can

be enabled by setting bit 0 in address 15_H high.

Bits 1 -- Carrier Tracking Loop Filter Accumulator Boundary Enable

The output of the accumulator in the K2 path of the Carrier Tracking Loop Filter is provided with a programmable boundary circuit which prevents the magnitude of the output value from exceeding the set boundary. This function is normally disabled and can be enabled by setting bit 1 in address 15_H high.

Bits 2 to 7 -- Unused

These bits should all be set to 1 for normal operation.

Address 16_H:

Bit 0 -- Unused

This bit should be set to 1 for normal operation.

Bits 1 through 3 -- Sampling Clock Scaling Control

The Symbol Timing NCO has 32-bit frequency resolution and the effective length of the accumulator is extended to 39 bits by means of an additional 7-bit divider. This extends the lower end of the frequency range of the sampling clock by an additional seven octaves, thereby allowing the STEL-2105 to operate at very low data rates while maintaining high resolution in the sampling rate control. The sampling clock is derived from one of the eight most significant phase bits of the NCO, according to the data stored in bits 1-3 in address 16_H. The MSB of the accumulator itself (Bit 31) is normally used as the clock. Selecting successively higher order bits results in the clock frequency being reduced by a factor of two each time, and the frequency control word should be increased accordingly to compensate for this, as shown in Table 14.

Bits 3-1	Acc. Bit Used for Clock	FCW Compensation Factor
0 _H	31	2 ⁰
1 _H	32	2 ¹
2 _H	33	2 ²
3 _H	34	2 ³
4 _H	35	2 ⁴
5 _H	36	2 ⁵
6 _H	37	2 ⁶
7 _H	38	2 ⁷

Table 14. Sampling Clock Scaling Factors

Address 17_H:

Bit 0 -- Load NCOs

The frequencies of the Symbol Timing NCO and the Local Oscillator NCO are both updated once every symbol period during normal operation. However, until some non-zero information has been loaded into the Symbol Timing NCO after a reset the symbol frequency will be set to zero, and no automatic updates will occur. It is therefore necessary to manually load the Symbol Timing NCO frequency after a reset by setting bit 0 in address 17_H high. This will load both NCOs. Bit 0 will automatically reset itself when this is done.

Address 18_H:

Bit 0 -- Freeze Status Registers

With the exception of the Symbol Lock Indicator Register (address 15_H), the information stored in the Status Registers changes at least once every symbol period. In order to make it possible to read out the contents of these registers more slowly the STEL-2105 is provided with the Freeze Status Registers function. This is implemented by setting bit 0 in address 18_H high, after which the register contents can be read any time during (or after) the next symbol period. When this bit is set high the current contents of the registers will be held until it is set low again.

STATUS (READ) REGISTERS

Address 00_H:

Local Oscillator Phase, Bits 2 through 9
The Local Oscillator NCO generates ten phase bits which are used to address the sine and cosine look-up table (LUT). The top eight bits (bits 9-2) are available in address 00_H. This information changes every cycle of CLK.

Addresses 01_H through 04_H:

Carrier Tracking Loop Filter Output,
Bits 0 through 31

The output of the Carrier Tracking Loop Filter is available in addresses 01_H through 04_H as shown in Table 18:

ADDR _{04_H}	ADDR _{03_H}	ADDR _{02_H}	ADDR _{01_H}
Bits 31-24	Bits 23-16	Bits 15-8	Bits 7-0

Table 18. Carrier Tracking Loop Filter Output Registers

Address 05_H:

Scaled Carrier Tracking AFC
Discriminator Output, Bits 0 through 7

The 8-bit output of the Carrier Tracking AFC Discriminator, after being scaled by the viewport, is available in address 05_H. This information changes every symbol period.

Address 06_H:

Carrier Tracking PLL Discriminator
Output, Bits 0 through 7

The 8-bit output of the Carrier Tracking PLL Discriminator is available in address 06_H. This information changes every symbol period.

Address 07_H:

Rotated Q-Channel Signal,
Bits 0 through 7

The 8-bit rotated Q channel signal is available in address 07_H. This information changes every symbol period. The rotation is controlled by bits 2-3 in address 15_H.

Address 08_H:

Rotated I-Channel Signal,
Bits 0 through 7

The 8-bit rotated I channel signal is available in address 08_H. This information changes every symbol period. The rotation is controlled by bits 2-3 in address 15_H.

Addresses 09_H and 0A_H:

Cross Product Generator Output, Bits 0 through 15

The output of the Cross Product circuit is available in addresses 09_H and 0A_H as shown in Table 19. This information changes every symbol period:

ADDR _{0A_H}	ADDR _{09_H}
Cross Prod. Bits 15-8	Cross Prod. Bits 7-0

Table 19. Cross Product Output Registers

Addresses 0B_H and 0C_H:

Dot Product Generator Output, Bits 0 through 15

The output of the Dot Product circuit is available in addresses 0B_H and 0C_H as shown in Table 20. This information changes every symbol period:

ADDR _{0C_H}	ADDR _{0B_H}
Dot Prod. Bits 15-8	Dot Prod. Bits 7-0

Table 20. Cross Product Output Registers

Addresses 0D_H through 10_H:

Symbol Timing Tracking Loop Filter
Output, Bits 0 through 31

The output of the Symbol Timing Tracking Loop Filter is available in addresses 0D_H through 10_H as shown in Table 21. This information changes every symbol period:

ADDR _{10_H}	ADDR _{0F_H}	ADDR _{0E_H}	ADDR _{0D_H}
Bits 31-24	Bits 23-16	Bits 15-8	Bits 7-0

Table 21. Carrier Tracking Loop Filter Output Registers

Address 11_H:

Symbol Timing Tracking Loop Filter
Input, Bits 0 through 7

The 8-bit input of the Symbol Timing Tracking Loop Filter is available in address 11_H. This information changes every symbol period.

Address 12_H:

Carrier Discriminator I-Channel Input,
Bits 0 through 7

The 8-bit I channel input of the Carrier Discriminator

is available in address 12_H. This information changes every symbol period.

Address 13_H:

Carrier Discriminator Q-Channel Input,
Bits 0 through 7

The 8-bit Q channel input of the Carrier Discriminator is available in address 13_H. This information changes every symbol period.

Address 14_H:

Overflow Flag Register

Address 14 contains eight overflow flags, as described below. They are all normally high, and active low.

Bit 0 -- Symbol Timing Discriminator
Viewport Overflow

The Viewport at the output of the Symbol Timing Discriminator circuit is controlled by bits 0-2 in address 01_H. If the viewport setting is too low the output may be saturated and bit 0 will be set low to indicate this condition.

Bits 1 and 2 -- Not used

Bit 3 -- On-Time Symbol Integrator
Viewport Overflow in I Channel

The Viewport at the output of the On-Time Symbol Integrator which scales signals for the Carrier Discriminators is controlled by bits 0-1 in address 03_H. If the viewport setting is too low the outputs may be saturated and bit 3 will be set low to indicate that this condition exists in the I Channel signal.

Bit 4 -- On-Time Symbol Integrator
Viewport Overflow in Q Channel

The Viewport at the output of the On-Time Symbol Integrator which scales signals for the Carrier Discriminators is controlled by bits 0-1 in address 03_H. If the viewport setting is too low the outputs may be saturated and bit 4 will be set low to indicate that this condition exists in the Q Channel signal.

Bit 5 -- Symbol Timing Loop Filter
Accumulator Overflow

The output of the accumulator in the K2 path of the Symbol Timing Tracking Loop Filter is provided with a programmable boundary circuit which prevents the magnitude of the output value from exceeding the set boundary. This function is normally disabled and can be enabled by setting bit 0 in address 15_H high. The boundary value is set according to the data stored in bits 0 to 4 in address 06_H. If the boundary function is

enabled and the value of the accumulator exceeds the boundary then bit 5 will be set low to indicate this condition. If the boundary function is disabled then bit 5 will be set low if the accumulator itself overflows.

Bit 6 -- Carrier Loop Filter Accumulator
Overflow

The output of the accumulator in the K2 path of the Carrier Tracking Loop Filter is provided with a programmable boundary circuit which prevents the magnitude of the output value from exceeding the set boundary. This function is normally disabled and can be enabled by setting bit 0 in address 15_H high. The boundary value is set according to the data stored in bits 0 to 4 in address 06_H. If the boundary function is enabled and the value of the accumulator exceeds the boundary then bit 6 will be set low to indicate this condition. If the boundary function is disabled then bit 6 will be set low if the accumulator itself overflows.

Bit 7 -- AFC Viewport Overflow

The Viewport at the output of the AFC Discriminator circuit is controlled by bits 0-3 in address 04_H. If the viewport setting is too low the output may be saturated and bit 7 will be set low to indicate this condition.

Address 15_H:

Symbol Lock Indicator, Bits 0 through 7

The symbol lock function, is computed by accumulating the following function over a period of 64 symbols:

$$\text{SYMLOCK} = \sum_{0}^{63} \{I + Q_{\text{on-time}} - 9/16 \{I + Q_{\text{late}} + I + Q_{\text{early}}\}\}$$

where $I + Q_{(\text{time})} = I_{(\text{time})} + Q_{(\text{time})}$

and (time) = on-time, late or early, as appropriate

SYMLOCK is calculated to an accuracy of 19 bits. The STEL-2105 incorporates a data selector circuit to select any eight consecutive bits from the 19-bit SYMLOCK output and makes it available in the Symbol Lock Indicator Register at address 15_H. The significance of this 8 bit value is determined by the data loaded into bits 3-0 in address 02_H. If the output is larger than the range specified by the scale factor, it will be saturated to the maximum or minimum values of the 8-bit number, i.e., 7F_H or 80_H.

DECIMAL, HEX AND BINARY ADDRESS EQUIVALENTS

Dec.	Hex.	Binary	Dec.	Hex.	Binary	Dec.	Hex.	Binary
0	00 _H	00000	9	09 _H	01001	18	12 _H	10010
1	01 _H	00001	10	0A _H	01010	19	13 _H	10011
2	02 _H	00010	11	0B _H	01011	20	14 _H	10100
3	03 _H	00011	12	0C _H	01100	21	15 _H	10101
4	04 _H	00100	13	0D _H	01101	22	16 _H	10110
5	05 _H	00101	14	0E _H	01110	23	17 _H	10111
6	06 _H	00110	15	0F _H	01111	24	18 _H	11000
7	07 _H	00111	16	10 _H	10000			
8	08 _H	01000	17	11 _H	10001			

REGISTER SUMMARY - WRITE REGISTERS

Address	Contents							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00 _H					Integrate & Dump Filter Viewport Control			
01 _H						Symbol Error Scale Factor		
02 _H					Symbol Lock Scale Factor			
03 _H							Carr. Error Scale Factor	
04 _H					AFC Scale Factor			
05 _H					Sym. K2 off	Sym. K1 off	Car. K2 off	Car. K1 off
06 _H					Symbol K2 Boundary			
07 _H					Carrier K2 Boundary			
08 _H				Carrier Tracking Loop K2 Gain Value				
09 _H				Carrier Tracking Loop K1 Gain Value				
0A _H				Symbol Timing K2 Gain Value				
0B _H				Symbol Timing K1 Gain Value				
0C-0F _H	Symbol Timing NCO Frequency Control Word (32 bits)							
10-13 _H	Local Oscillator NCO Frequency Control Word (32 bits)							
14 _H	Unused (set to 0)	Inv. Carrier Loop Filter	Unused (set to 1)	Unused (set to 0)	AGC Polarity	2's Comp. Input	Unused (set to 0)	Unused (set to 1)
15 _H	Unused (set all to 1)						En. Carrier Boundary	En. Symbol Boundary
16 _H					SAMCLK Select			Unused (set to 1)
17 _H								Load NCO
18 _H								Freeze Regs

REGISTER SUMMARY - READ REGISTERS

Address s	Contents							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00 _H	Local Oscillator NCO Phase, Bits 9-2							
01 _H	Carrier Tracking Loop Filter Output, Bits 7-0							
02 _H	Carrier Tracking Loop Filter Output, Bits 15-8							
03 _H	Carrier Tracking Loop Filter Output, Bits 23-16							
04 _H	Carrier Tracking Loop Filter Output, Bits 31-24							
05 _H	Carrier AFC Discriminator Output, Bits 7-0							
06 _H	Carrier PLL Discriminator Output, Bits 7-0							
07 _H	Rotated Q Channel Signal							
08 _H	Rotated I Channel Signal							
09 _H	Cross Product Output, Bits 7-0							
0A _H	Cross Product Output, Bits 15-8							
0B _H	Dot Product Output, Bits 7-0							
0C _H	Dot Product Output, Bits 15-8							
0D _H	Symbol Tracking Loop Filter Output, Bits 7-0							
0E _H	Symbol Tracking Loop Filter Output, Bits 15-8							
0F _H	Symbol Tracking Loop Filter Output, Bits 23-16							
10 _H	Symbol Tracking Loop Filter Output, Bits 31-24							
11 _H	Symbol Tracking Loop Filter Input, Bits 7-0							
12 _H	Carrier Discriminator I Channel Input							
13 _H	Carrier Discriminator Q Channel Input							
14 _H	AFC Viewport Overflow	Carr. Trck. Loop Filter Acc. Ovfl.	Symb.Timing Loop Filter Acc. Ovfl.	Carr. Disc. Q input Overflow	Carr. Disc. I input Overflow	Not used		Symb. Disc. Viewport Overflow
15 _H	Symbol Lock Indicator							

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Warning: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{SS} .

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	-40 to +125	°C
V_{DDmax}	Supply voltage on V_{DD}	-0.3 to +7	volts
$V_{I(max)}$	Input voltage	-0.3 to $V_{DD}+0.3$	volts
I_i	DC input current	± 10	mA

RECOMMENDED OPERATING CONDITIONS

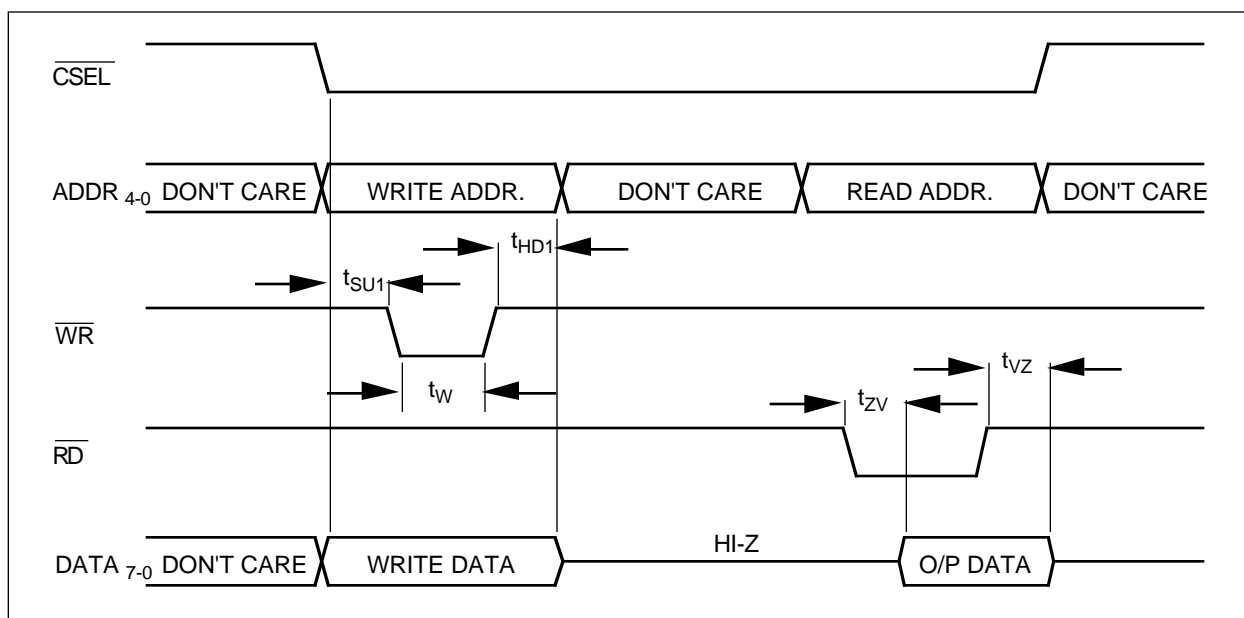
Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage	$+5 \pm 5\%$	volts
T_a	Operating Temperature (Ambient)	-40 to +85	°C

D.C. CHARACTERISTICS

Operating Conditions: $V_{DD} = 5.0\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$, $T_a = -40^\circ\text{ to }85^\circ\text{ C}$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{DDQ}	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational		5		mA/MHz	$f_{CLK} = 36\text{ MHz}$
$V_{IH(min)}$	High Level Input Voltage	2.0			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current			10	μA	CLK only, $V_{IN} = V_{DD}$
$I_{IH(max)}$	High Level Input Current	10	35	110	μA	All other inputs, $V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current			-10	μA	All inputs, $V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5	V_{DD}	volts	$I_O = -2.0\text{ mA}$, All outputs
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	$I_O = +2.0\text{ mA}$, All outputs
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, $V_{DD} = \text{max}$
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

MICROPROCESSOR INTERFACE TIMING

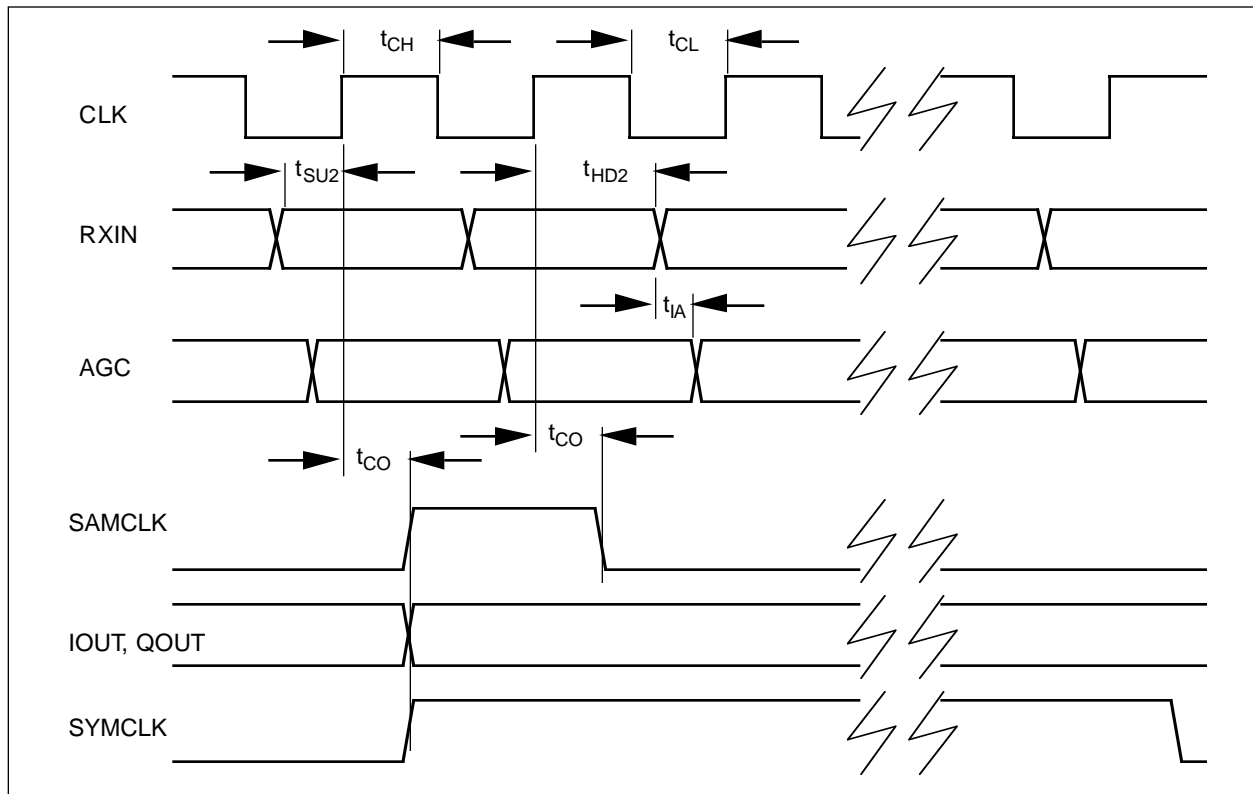


A.C. CHARACTERISTICS

Operating Conditions: $V_{\text{DD}} = 5.0 \text{ V} \pm 5\%$, $V_{\text{SS}} = 0 \text{ V}$, $T_a = -40^\circ \text{ to } 85^\circ \text{ C}$,

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{SU1}	$\overline{\text{CSEL}}$, ADDR, DATA to $\overline{\text{WR}}$ setup	5		nsec.	Load = 10 pF
t_{DH1}	$\overline{\text{WR}}$ to $\overline{\text{CSEL}}$, ADDR, DATA hold	5		nsec.	
t_{W}	$\overline{\text{WR}}$ pulse width	5		nsec.	
t_{ZV}	DATA Hi-Z to DATA valid		40		
t_{VZ}	DATA valid to DATA Hi-Z		40		
t_{SU2}	RXIN to CLK setup	3		nsec.	
t_{DH2}	CLK to RXIN hold	5		nsec.	
t_{IA}	RXIN stable to AGC valid		10	nsec.	
t_{CO}	CLK to output delays:				
	CLK to SAMCLK delay		28	nsec.	
	CLK to SYMCLK delay		13	nsec.	
	CLK to IOUT/QOUT delay		28	nsec.	

INPUT AND OUTPUT TIMING



Information in this document is provided in connection with Intel® products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied

warranty, relating to sale and/or use of Intel® products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

For Further Information Call or Write



INTEL CORPORATION

Cable Network Operation

350 E. Plumeria Drive, San Jose, CA 95134

Customer Service Telephone: (408) 545-9700

Technical Support Telephone: (408) 545-9799

FAX: (408) 545-9888