

## CMOS Counter/Dividers

CD4017BMS - Decade Counter with 10 Decoded Outputs

CD4022BMS - Octal Counter with 8 Decoded Outputs

CD4017BMS and CD4022BMS are 5-stage and 4-stage Johnson counters having 10 and 8 decoded outputs, respectively. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times.

These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson counter configuration permits high speed operation, 2-input decode gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counter sequence. The decoded output are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the CD4017BMS or every 8 clock input cycles in the CD4022BMS and is used to ripple-clock the succeeding device in a multi-device counting chain.

The CD4017BMS and CD4022BMS series types are supplied in these 16 lead outline packages

Braze Seal DIP \*H4W †H4X

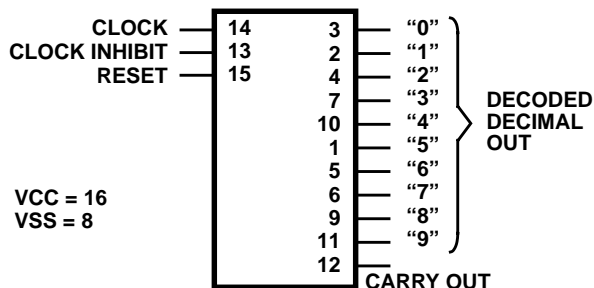
Frit Seal DIP \*H1F †H1E

Ceramic Flatpack H6W

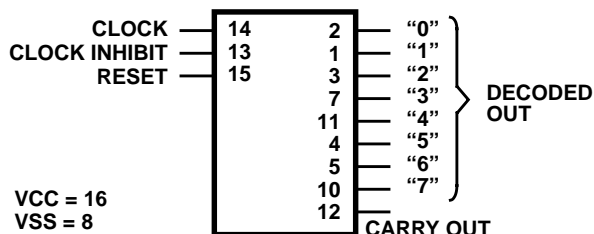
\*CD4017B Only † CD4022B Only

## Functional Diagrams

**CD4017BMS**



**CD4022BMS**



## Features

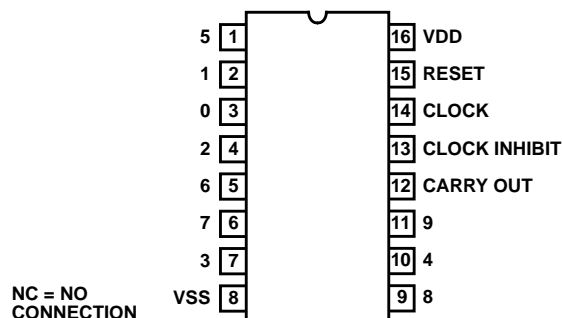
- High Voltage Types (20V Rating)
- Fully Static Operation
- Medium-Speed Operation 10MHz (Typ) at VDD = 10V
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard Number 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

## Applications

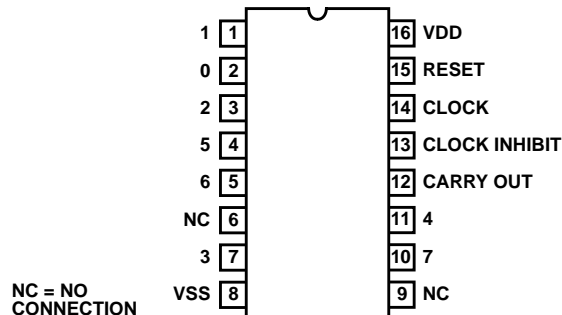
- Decade Counter/Decimal Decode Display (CD4017BMS)
- Binary Counter/Decoder
- Frequency Division
- Counter Control/Timers
- Divide-by-N Counting
- For Further Application Information, See ICAN-6166 "COS/MOS MSI Counter and Register Design and Applications"

## Pinouts

**CD4017BMS  
TOP VIEW**



**CD4022BMS  
TOP VIEW**



### Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V  
 (Voltage Referenced to VSS Terminals)  
 Input Voltage Range, All Inputs ..... -0.5V to VDD +0.5V  
 DC Input Current, Any One Input ..... ±10mA  
 Operating Temperature Range ..... -55°C to +125°C  
 Package Types D, F, K, H  
 Storage Temperature Range (TSTG) ..... -65°C to +150°C  
 Lead Temperature (During Soldering) ..... +265°C  
 At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for  
 10s Maximum

### Reliability Information

Thermal Resistance .....  $\theta_{ja}$   $\theta_{jc}$   
 Ceramic DIP and FRIT Package .... 80°C/W 20°C/W  
 Flatpack Package ..... 70°C/W 20°C/W  
 Maximum Package Power Dissipation (PD) at +125°C  
 For TA = -55°C to +100°C (Package Type D, F, K) ..... 500mW  
 For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate  
 Linearity at 12mW/°C to 200mW  
 Device Dissipation per Output Transistor ..... 100mW  
 For TA = Full Package Temperature Range (All Package Types)  
 Junction Temperature ..... +175°C

**TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	μA
				2	+125°C	-	1000	μA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	μA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10μA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.  
 2. Go/No Go test with limits applied to inputs  
 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

# CD4017BMS, CD4022BMS

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (Note 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Clock to Decode Out	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	650	ns
			10, 11	+125°C, -55°C	-	878	ns
Propagation Delay Clock to Carry Out	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay Reset to Out	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	530	ns
			10, 11	+125°C, -55°C	-	716	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Fre- quency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2.5	-	MHz
			10, 11	+125°C, -55°C	1.85	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	μA
				+125°C	-	150	μA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	300	μA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	600	μA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V

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**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Clock to Decode Out	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	270	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Propagation Delay Clock to Carry Out	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Propagation Delay Reset to out	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	230	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	5.0	-	MHz
		VDD = 15V	1, 2, 3	+25°C	5.5	-	MHz
Minimum Setup Time Clock Inhibit to Clock Setup	TS	VDD = 5V	1, 2, 3	+25°C	-	230	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Minimum Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	260	ns
		VDD = 10V	1, 2, 3	+25°C	-	110	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

**TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	μA
N Threshold Voltage	VTN	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.7	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

- NOTES: 1. All voltages referenced to device GND. 2. CL = 50pF, RL = 200K, Input TR, TF < 20ns. 3. See Table 2 for +25°C limit. 4. Read and Record

**TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C**

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

## CD4017BMS, CD4022BMS

**TABLE 6. APPLICABLE SUBGROUPS**

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

**TABLE 7. TOTAL DOSE IRRADIATION**

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

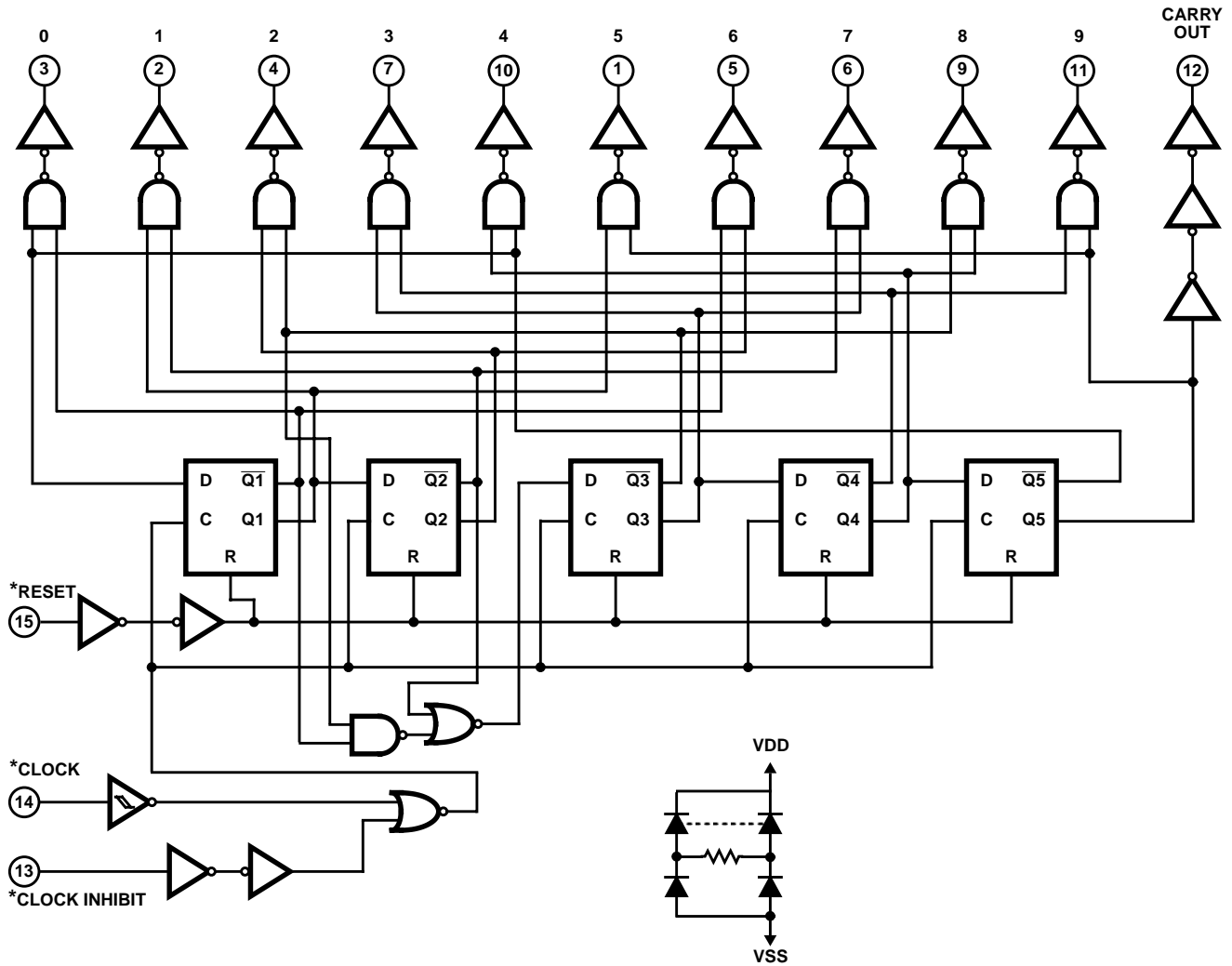
**TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS**

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD4017BMS AND CD4002B						
Static Burn-In 1 Note 1	1 - 7, 9 - 12	8, 13, 15	14, 16	-	-	-
Static Burn-In 2 Note 1	1 - 7, 9 - 12	8, 14	13, 15, 16	-	-	-
Dynamic Burn-In Note 1	-	8, 13, 15	16	1 - 7, 9 - 12	14	-
Irradiation Note 2	1 - 7, 9 - 12	8	13 - 16	-	-	-

NOTE:

- Each pin except VDD and GND will have a series resistor of  $10K \pm 5\%$ ,  $VDD = 18V \pm 0.5V$
- Each pin except VDD and GND will have a series resistor of  $47K \pm 5\%$ ; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures,  $VDD = 10V \pm 0.5V$

## Logic Diagram



\* All Inputs Protected by CMOS Protection Network

FIGURE 1. CD4017BMS

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Logic Diagram (Continued)

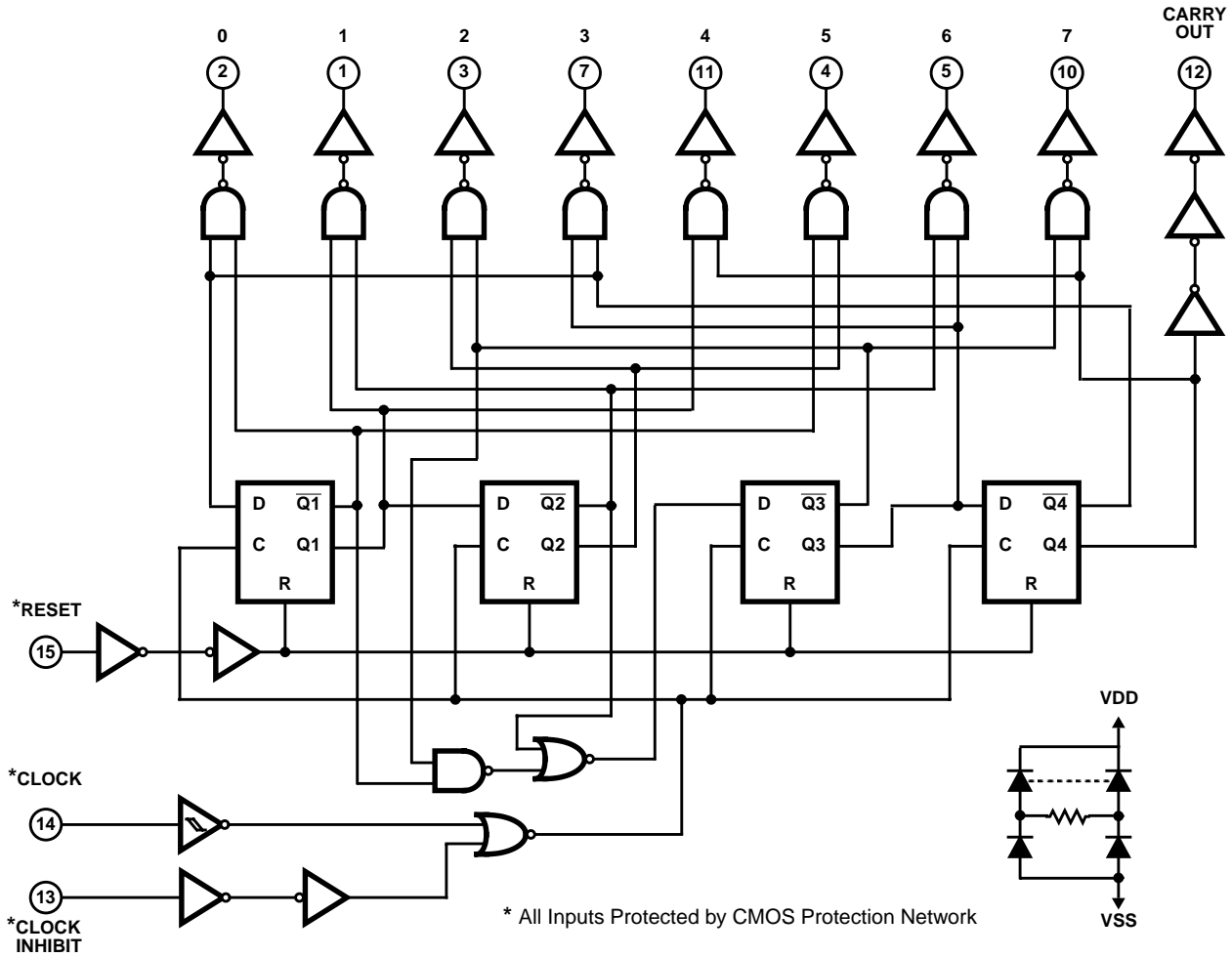


FIGURE 2. CD4022BMS

Timing Diagram

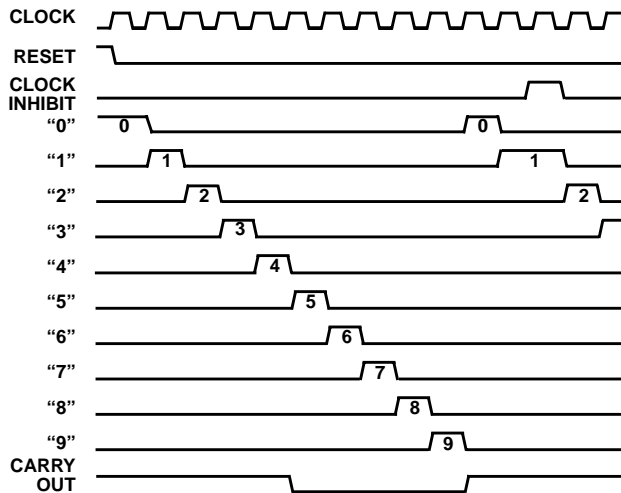


FIGURE 3. CD4017BMS

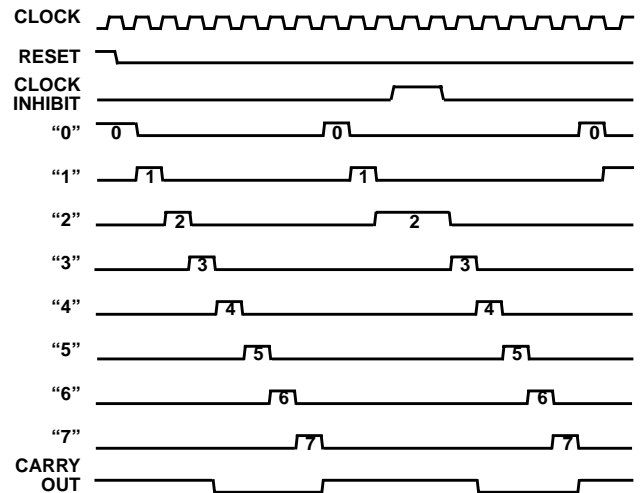


FIGURE 4. CD4022BMS

## Typical Performance Characteristics

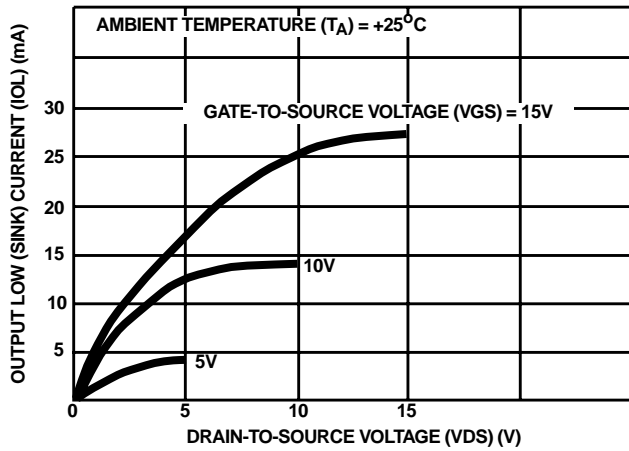


FIGURE 5. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

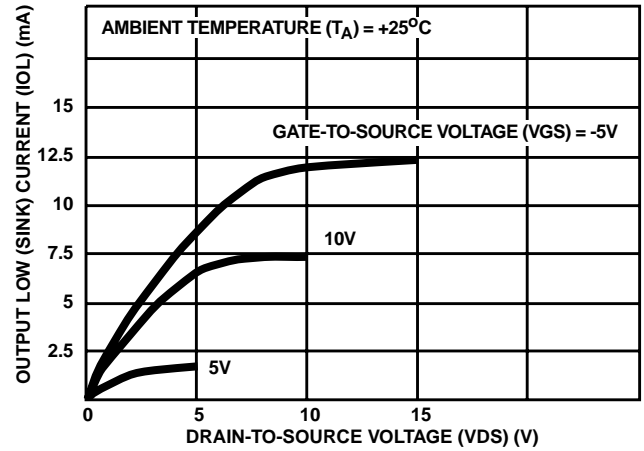


FIGURE 6. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

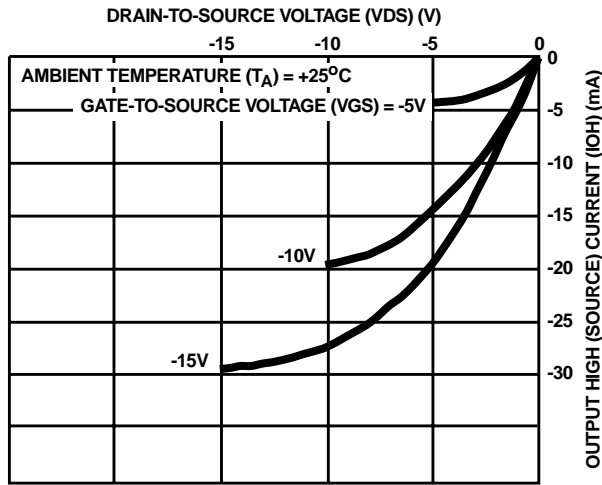


FIGURE 7. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

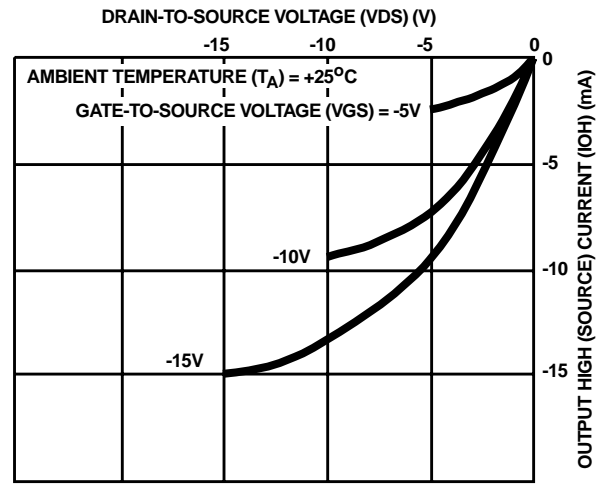


FIGURE 8. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

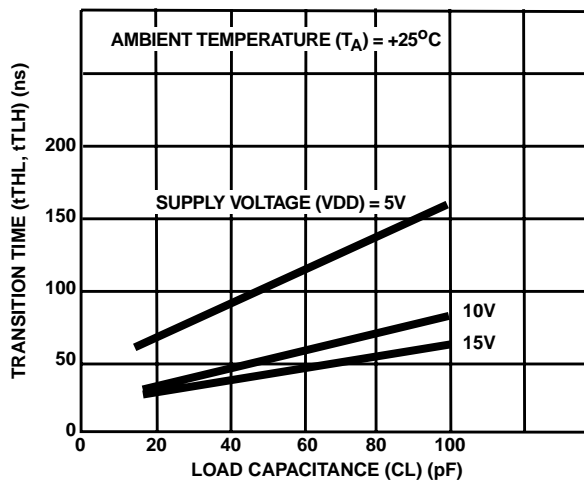


FIGURE 9. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

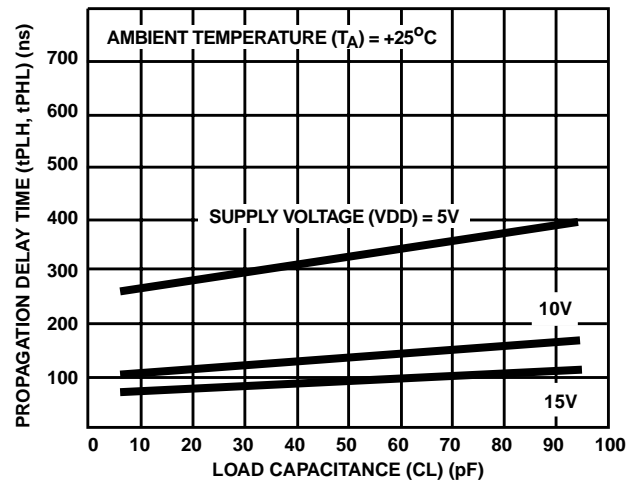


FIGURE 10. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO DECODE OUTPUT)



Typical Performance Characteristics (Continued)

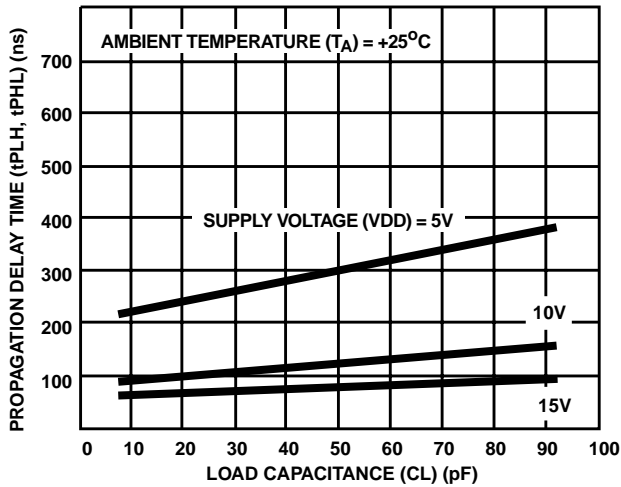


FIGURE 11. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO CARRY OUT)

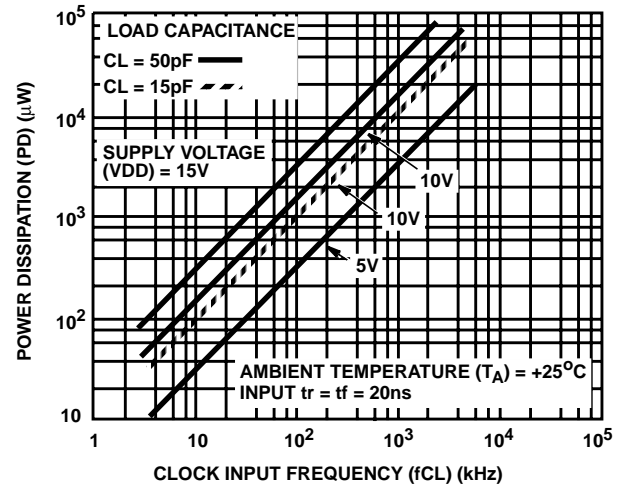
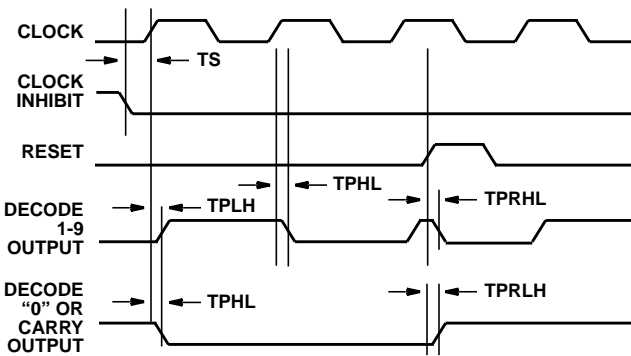


FIGURE 12. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK INPUT FREQUENCY



Delays Measured Between 50% levels on All Waveforms

FIGURE 13. PROPAGATION DELAY, SETUP, AND RESET REMOVAL TIME WAVEFORMS

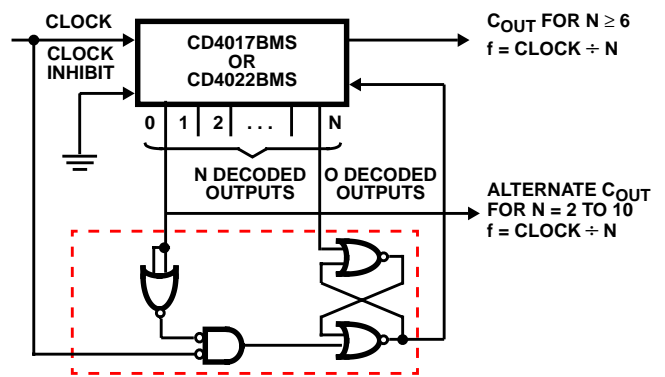


FIGURE 14. DIVIDE BY N COUNTER ( $N \leq 10$ ) WITH N DECODED OUTPUTS

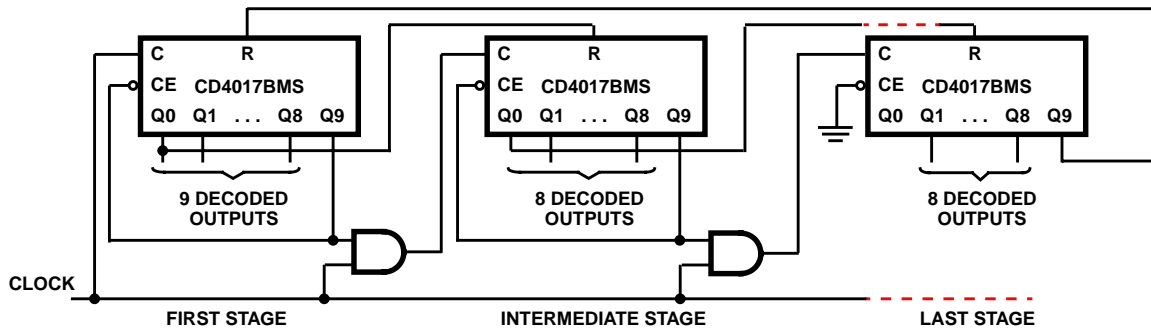
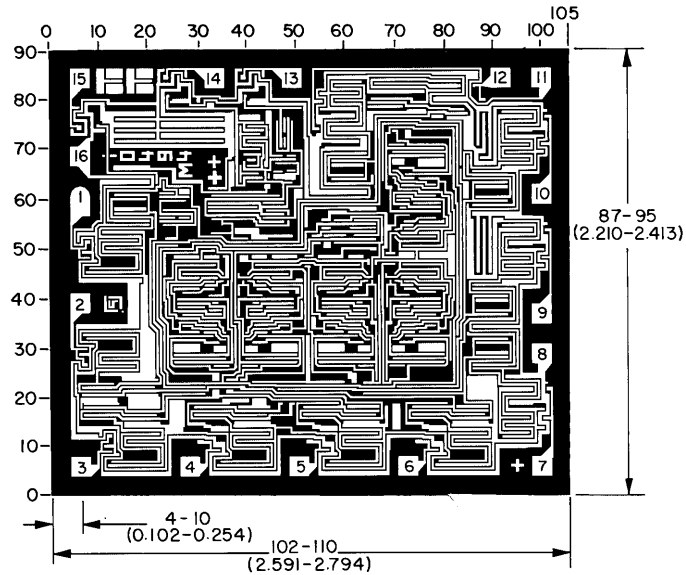


FIGURE 15. CASCADING THE CD4017BMS

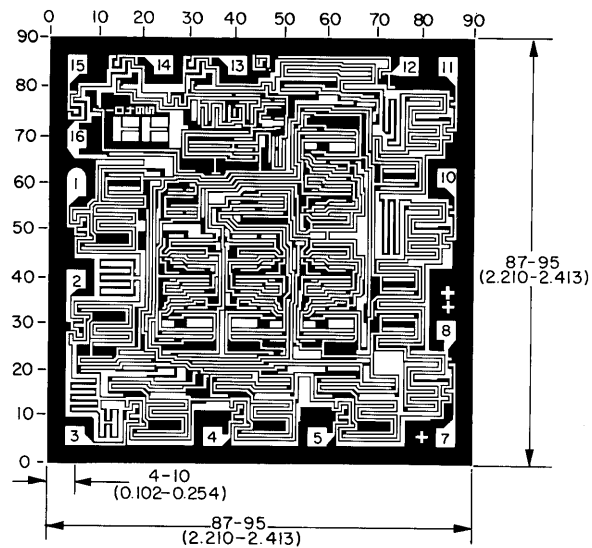
When the  $N^{\text{th}}$  decoded output is reached ( $N^{\text{th}}$  clock pulse) the S-R flip-flop (constructed from two NOR gates of the CD4001B) generates a reset pulse which clears the CD4017BMS or CD4022BMS to its zero count. At this time, if the  $N^{\text{th}}$  decoded output is greater than or equal to 6 in the CD4017BMS or 5 in the CD4022BMS, the  $C_{OUT}$  line goes high to clock the next CD4017BMS or CD4022BMS counter section. The "0"

decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output low resets the S-R flip-flop to enable the CD4017BMS or CD4022BMS. If the  $N^{\text{th}}$  decoded output is less than 6 (CD4017BMS) or 5 (CD4022BMS), the  $C_{OUT}$  line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.

## Chip Dimensions and Pad Layouts



CD4017BMSH



Dimensions in parentheses are in millimeters  
and are derived from the basic inch dimensions  
as indicated. Grid graduations are in mils ( $10^{-3}$  inch)

CD4022BMSH

**METALLIZATION:** Thickness:  $11\text{k}\text{\AA} - 14\text{k}\text{\AA}$ , AL.

**PASSIVATION:**  $10.4\text{k}\text{\AA} - 15.6\text{k}\text{\AA}$ , Silane

**BOND PADS:** 0.004 inches X 0.004 inches MIN

**DIE THICKNESS:** 0.0198 inches - 0.0218