

December 1992

CMOS 4-Bit Magnitude Comparator

Features

- High Voltage Type (20V Rating)
- Expansion to 8, 12, 16 . . . 4N Bits by Cascading Units
- Medium Speed Operation
 - Compares Two 4-Bit Words in 180ns (Typ.) at 10V
- 100% Tested for Quiescent Current at 20V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1 μ A at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
 - 1V at VDD = 5V
 - 2V at VDD = 10V
 - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Servo Motor Controls
- Process Controllers

Description

CD4585BMS is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to" or "greater than" a second 4-bit word.

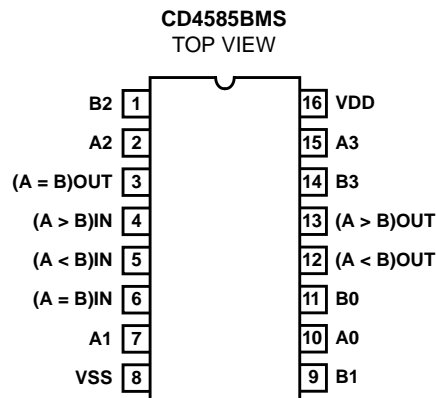
The CD4585BMS has eight comparing inputs (A3, B3, through A0, B0), three outputs (A < B, = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit system designers to expand the comparator function to 8, 12, 16 . . . 4N bits. When a single CD4585BMS is used, the cascading inputs are connected as follows: (A < B) = low, (A = B) = high, (A > B) = high.

Cascading these units for comparison of more than 4 bits is accomplished as shown in Figure 9.

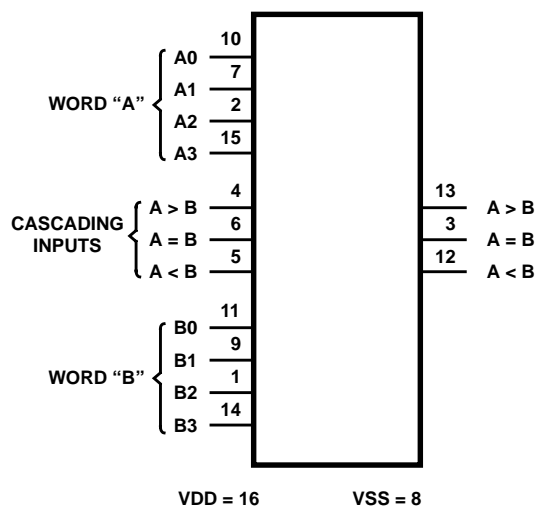
The CD4585BMS is supplied in these 16-lead outline packages:

Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

Pinout



Functional Diagram



Specifications CD4585BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) -0.5V to +20V
 (Voltage Referenced to VSS Terminals)
 Input Voltage Range, All Inputs -0.5V to VDD +0.5V
 DC Input Current, Any One Input $\pm 10\text{mA}$
 Operating Temperature Range -55°C to $+125^{\circ}\text{C}$
 Package Types D, F, K, H
 Storage Temperature Range (TSTG) -65°C to $+150^{\circ}\text{C}$
 Lead Temperature (During Soldering) $+265^{\circ}\text{C}$
 At Distance $1/16 \pm 1/32$ Inch ($1.59\text{mm} \pm 0.79\text{mm}$) from case for
 10s Maximum

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
 Ceramic DIP and FRIT Package 80°C/W 20°C/W
 Flatpack Package 70°C/W 20°C/W
 Maximum Package Power Dissipation (PD) at $+125^{\circ}\text{C}$
 For $T_A = -55^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ (Package Type D, F, K) 500mW
 For $T_A = +100^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (Package Type D, F, K) Derate
 Linearity at $12\text{mW}/^{\circ}\text{C}$ to 200mW
 Device Dissipation per Output Transistor 100mW
 For $T_A = \text{Full Package Temperature Range (All Package Types)}$
 Junction Temperature $+175^{\circ}\text{C}$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	$+25^{\circ}\text{C}$	-	10	μA
				2	$+125^{\circ}\text{C}$	-	1000	μA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	μA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	$+25^{\circ}\text{C}$	-100	-	nA
				2	$+125^{\circ}\text{C}$	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	$+25^{\circ}\text{C}$	-	100	nA
				2	$+125^{\circ}\text{C}$	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	$+25^{\circ}\text{C}$, $+125^{\circ}\text{C}$, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	$+25^{\circ}\text{C}$, $+125^{\circ}\text{C}$, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	$+25^{\circ}\text{C}$	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	$+25^{\circ}\text{C}$	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	$+25^{\circ}\text{C}$	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	$+25^{\circ}\text{C}$	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	$+25^{\circ}\text{C}$	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	$+25^{\circ}\text{C}$	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	$+25^{\circ}\text{C}$	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = $-10\mu\text{A}$		1	$+25^{\circ}\text{C}$	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = $10\mu\text{A}$		1	$+25^{\circ}\text{C}$	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	$+25^{\circ}\text{C}$	$\text{VOH} > \text{VDD}/2$	$\text{VOL} < \text{VDD}/2$	V
		VDD = 20V, VIN = VDD or GND		7	$+25^{\circ}\text{C}$			
		VDD = 18V, VIN = VDD or GND		8A	$+125^{\circ}\text{C}$			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^{\circ}\text{C}$, $+125^{\circ}\text{C}$, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^{\circ}\text{C}$, $+125^{\circ}\text{C}$, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^{\circ}\text{C}$, $+125^{\circ}\text{C}$, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^{\circ}\text{C}$, $+125^{\circ}\text{C}$, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
 2. Go/No Go test with limits applied to inputs.
 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

Specifications CD4585BMS

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Comparing Inputs to Outputs	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay Cascading Inputs to Out- puts	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	μA
				+125°C	-	150	μA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	300	μA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	600	μA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V

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TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Comparing Inputs to Outputs	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Propagation Delay Cascading Inputs to Out- puts	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Inputs	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

- NOTES: 1. All voltages referenced to device GND. 2. CL = 50pF, RL = 200K, Input TR, TF < 20ns. 3. See Table 2 for +25°C limit. 4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

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TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V \pm -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	3, 12, 13	1, 2, 4 - 11, 14, 15	16			
Static Burn-In 2 Note 1	3, 12, 13	8	1, 2, 4 - 7, 9 - 11, 14 - 16			
Dynamic Burn-In Note 1	-	5 - 9, 11, 14, 15	1, 4, 16	3, 12, 13	2	10
Irradiation Note 2	3, 12, 13	8	1, 2, 4 - 7, 9 - 11, 14 - 16			

NOTE:

- Each pin except VDD and GND will have a series resistor of $10K \pm 5\%$, $VDD = 18V \pm 0.5V$
- Each pin except VDD and GND will have a series resistor of $47K \pm 5\%$; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, $VDD = 10V \pm 0.5V$

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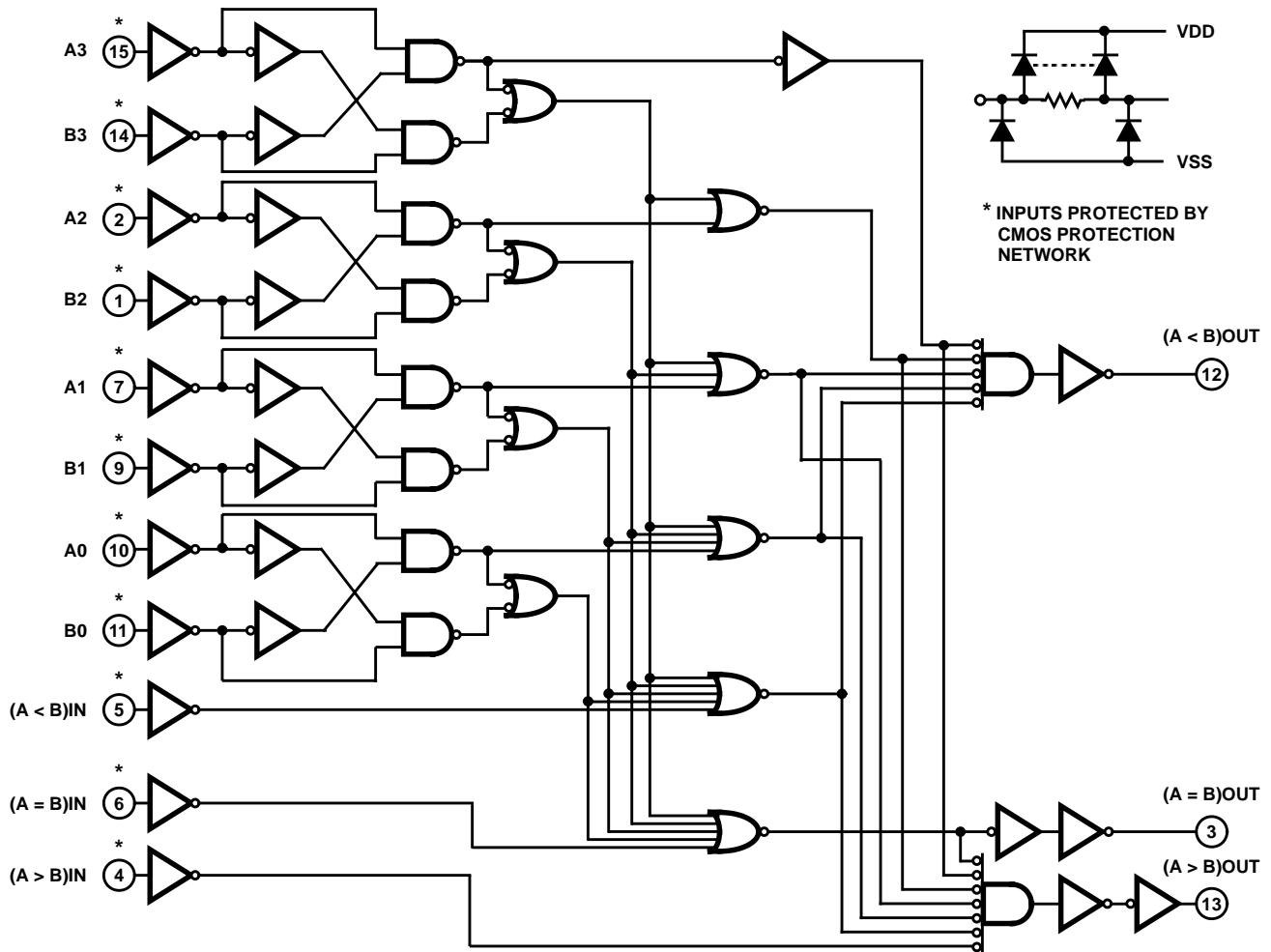
Logic Diagram

FIGURE 1. LOGIC DIAGRAM

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A < B	A = B	A > B	A < B	A = B	A > B
A3 > B3	X	X	X	X	X	1	0	0	1
A3 = B3	A2 > B2	X	X	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 > B1	X	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	X	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	X	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	1	0	0
A3 < B3	X	X	X	X	X	X	1	0	0

X = Don't Care

Logic 1 = High Level

Logic 0 = Low Level

Typical Performance Characteristics

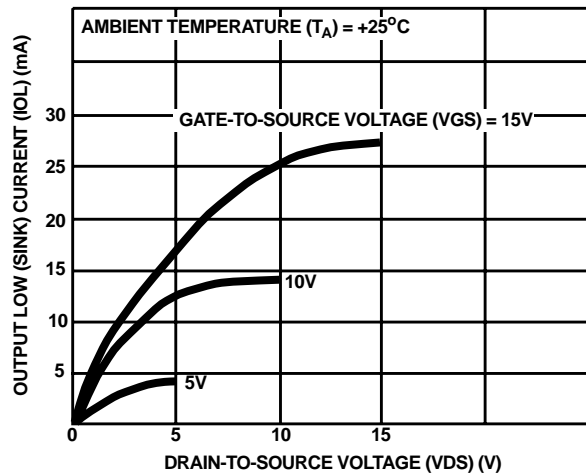


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

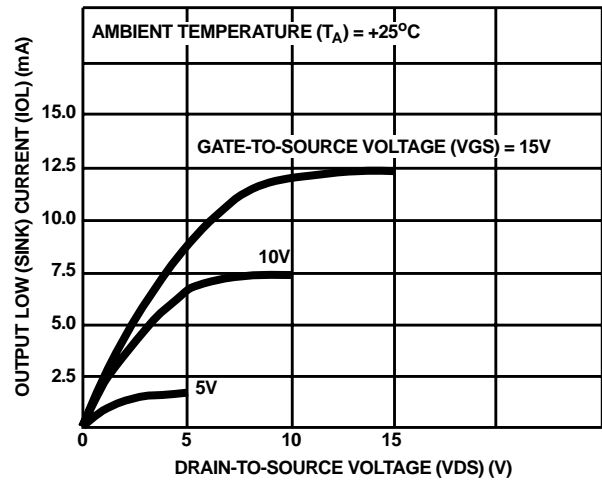


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

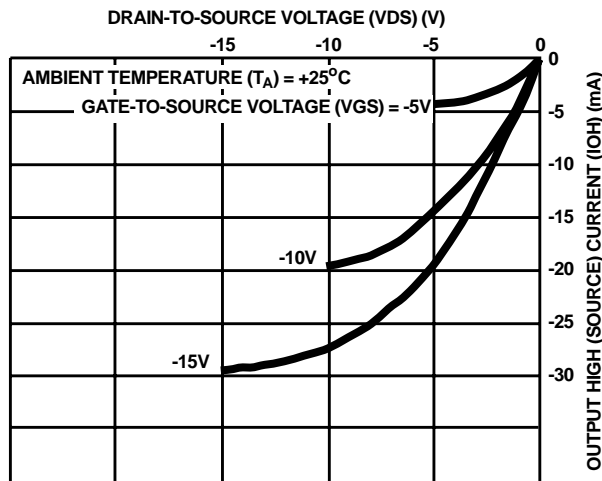


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

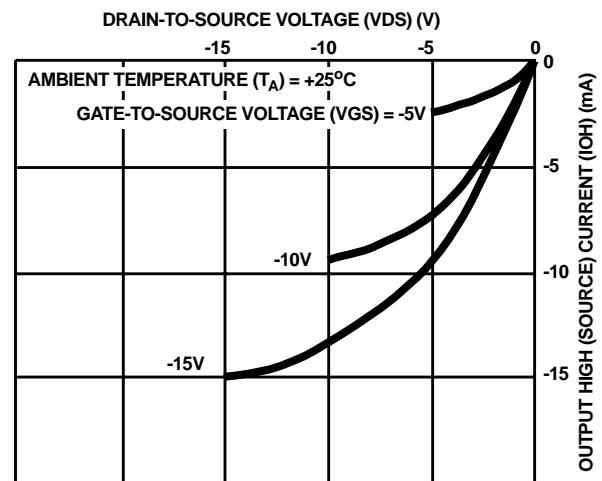


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

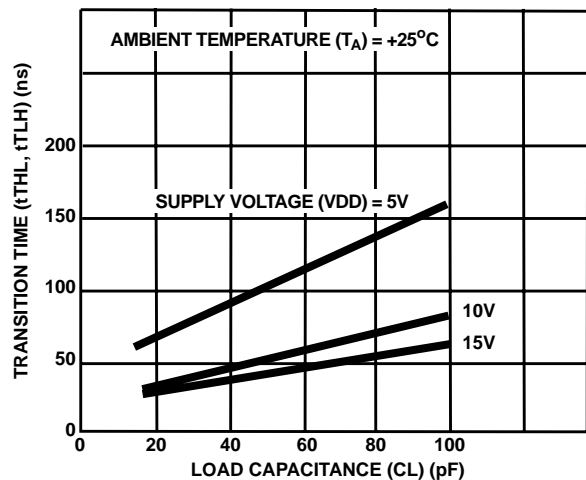


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

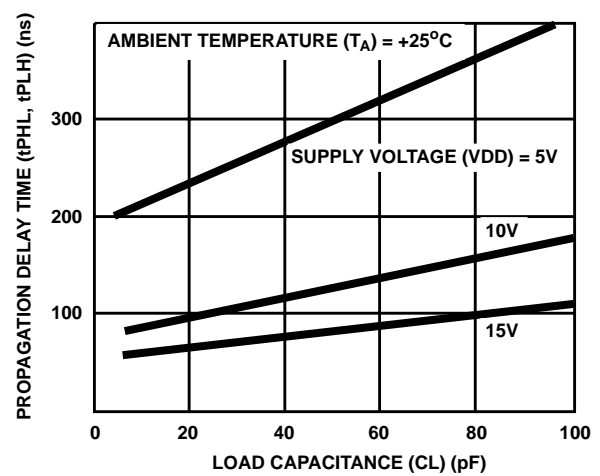


FIGURE 7. TYPICAL PROPAGATION DELAY TIME ("COMPARING INPUTS" TO OUTPUTS) AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

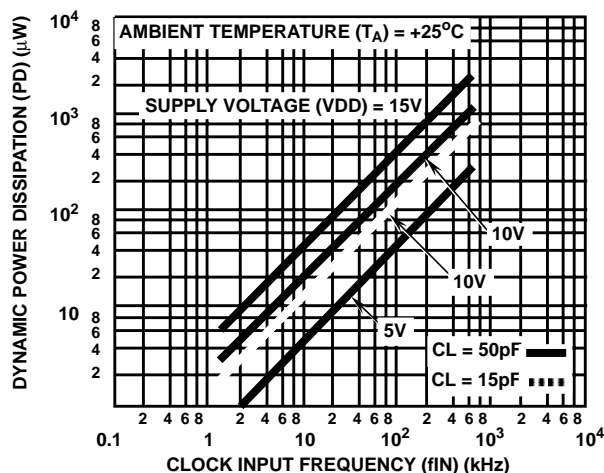


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK INPUT FREQUENCY

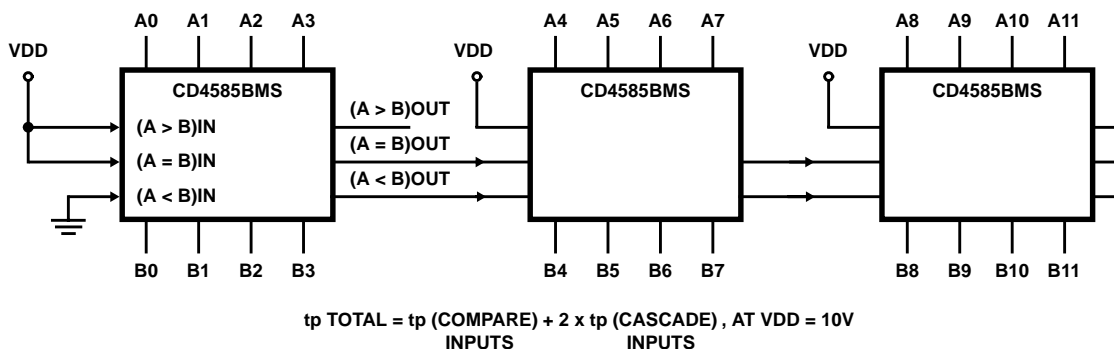
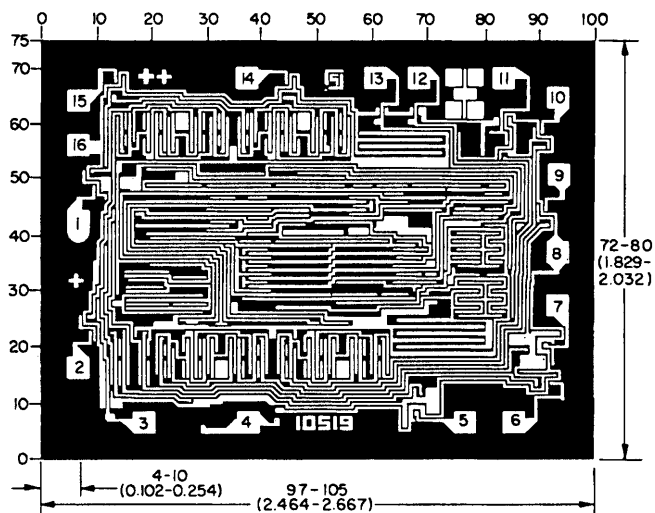


FIGURE 9. TYPICAL SPEED CHARACTERISTICS OF A 12-BIT COMPARATOR

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: $11\text{k}\text{\AA} - 14\text{k}\text{\AA}$, AL.
PASSIVATION: $10.4\text{k}\text{\AA} - 15.6\text{k}\text{\AA}$, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches