

Low Power, 180MHz Buffer Amplifier

élan**tec**

The EL2002 is a low cost monolithic, high slew rate, buffer amplifier. Built using the Elantec monolithic

Complementary Bipolar process, this patented buffer has a -3dB bandwidth of 180MHz, and delivers 100mA, yet draws only 5mA of supply current. It typically operates from $\pm 15V$ power supplies but will work with as little as $\pm 5V$.

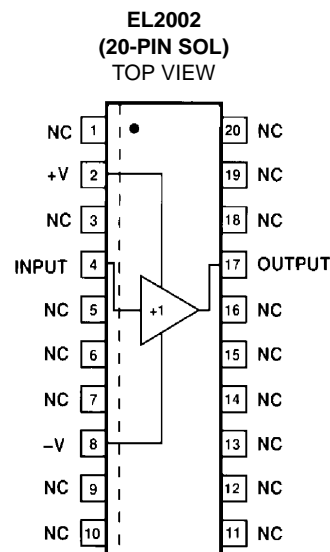
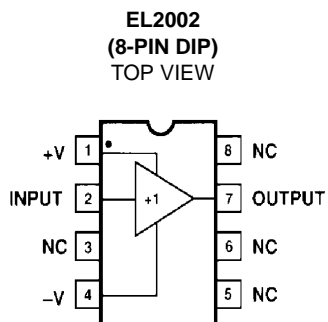
This high speed buffer may be used in a wide variety of applications in military, video and medical systems. Typical examples include fast op-amp output current boosters, coaxial cable drivers and A/D converter input buffers.

Elantec's products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: Elantec's Processing, Monolithic Integrated Circuits.

Ordering Information

| PART NUMBER | TEMP. RANGE | PACKAGE | PKG. NO. |
|-------------|--------------|------------|----------|
| EL2002ACN | 0°C to +75°C | P-DIP | MDP0031 |
| EL2002CM | 0°C to +75°C | 20-Pin SOL | MDP0027 |
| EL2002CN | 0°C to +75°C | P-DIP | MDP0031 |

Pinouts



Features

- 180MHz bandwidth
- 2000V/ μs slew rate
- Low bias current, 3 μA typical
- 100mA output current
- 5mA supply current
- Short circuit protected
- Low cost
- Stable with capacitive loads
- Wide supply range $\pm 5V$ to $\pm 15V$
- No thermal runaway

Applications

- Op amp output current booster
- Cable/line driver
- A/D input buffer
- Isolation buffer

Manufactured under U.S. Patent No. 4,833,424, 4,827,223 U.K. Patent No. 2217134

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$)

V_S Supply Voltage ($V+ - V-$) $\pm 18\text{V}$ or 36V
 V_{IN} Input Voltage $\pm 15\text{V}$ or V_S
 If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds $\pm 7.5\text{V}$ then the input current must be limited to $\pm 50\text{mA}$. See the applications section for more information.

I_{IN} Input Current (See above note) $\pm 50\text{mA}$
 P_D Power Dissipation See Curves
 The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Output Short Circuit Duration Continuous
 A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.
 T_A Operating Temperature Range 0°C to $+75^\circ\text{C}$
 T_J Operating Junction Temperature 150°C
 T_{ST} Storage Temperature -65°C to $+150^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications $V_S = \pm 15\text{V}$, $R_S = 50\Omega$, unless otherwise specified.

| PARAMETER | DESCRIPTION | TEST CONDITIONS | | | LIMITS | | | UNITS |
|-----------|---|------------------|-------------|--------------------|-----------|----------|-----|------------------|
| | | V_{IN} | LOAD | TEMP | MIN | TYP | MAX | |
| V_{OS} | Offset Voltage | 0 | ∞ | 25°C | -15 | 5 | +15 | mV |
| | | | | T_{MIN}, T_{MAX} | -20 | | +20 | mV |
| | | 0 | ∞ | 25°C | -40 | 10 | +40 | mV |
| | | | | T_{MIN}, T_{MAX} | -50 | | +50 | mV |
| I_{IN} | Input Current | 0 | ∞ | 25°C | -10 | 3 | +10 | μA |
| | | | | T_{MIN}, T_{MAX} | -15 | | +15 | μA |
| | | 0 | ∞ | 25°C | -15 | 5 | +15 | μA |
| | | | | T_{MIN}, T_{MAX} | -20 | | +20 | μA |
| R_{IN} | Input Resistance | $\pm 12\text{V}$ | 100Ω | 25°C | 1 | 3 | | $\text{M}\Omega$ |
| | | | | T_{MIN}, T_{MAX} | 0.1 | | | $\text{M}\Omega$ |
| A_{V1} | Voltage Gain | $\pm 12\text{V}$ | ∞ | 25°C | 0.990 | 0.998 | | V/V |
| | | | | T_{MIN}, T_{MAX} | 0.985 | | | V/V |
| A_{V2} | Voltage Gain | $\pm 10\text{V}$ | 100Ω | 25°C | 0.85 | 0.93 | | V/V |
| | | | | T_{MIN}, T_{MAX} | 0.83 | | | V/V |
| A_{V3} | Voltage Gain with $V_S = \pm 5\text{V}$ | $\pm 3\text{V}$ | 100Ω | 25°C | 0.83 | 0.91 | | V/V |
| | | | | T_{MIN}, T_{MAX} | 0.80 | | | V/V |
| V_O | Output Voltage Swing | $\pm 12\text{V}$ | 100Ω | 25°C | ± 10 | ± 11 | | V |
| | | | | T_{MIN}, T_{MAX} | ± 9.5 | | | V |
| R_{OUT} | Output Resistance | $\pm 2\text{V}$ | 100Ω | 25°C | | 8 | 13 | Ω |
| | | | | T_{MIN}, T_{MAX} | | | 15 | Ω |
| I_{OUT} | Output Current | $\pm 12\text{V}$ | (Note 1) | 25°C | +100 | +160 | | mA |
| | | | | T_{MIN}, T_{MAX} | ± 95 | | | mA |
| I_S | Supply Current | 0 | ∞ | 25°C | | 5 | 7.5 | mA |
| | | | | T_{MIN}, T_{MAX} | | | 10 | mA |
| PSRR | Supply Rejection (Note 2) | 0 | ∞ | 25°C | 60 | 75 | | dB |
| | | | | T_{MIN}, T_{MAX} | 50 | | | dB |
| t_R | Rise Time | 0.5V | 100Ω | 25°C | | 2.8 | | ns |
| t_D | Propagation Delay | 0.5V | 100Ω | 25°C | | 1.5 | | ns |

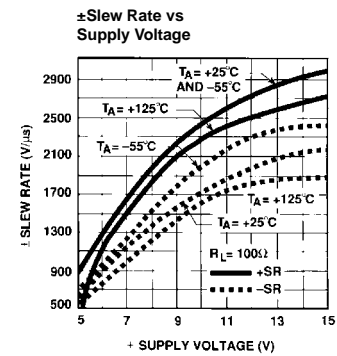
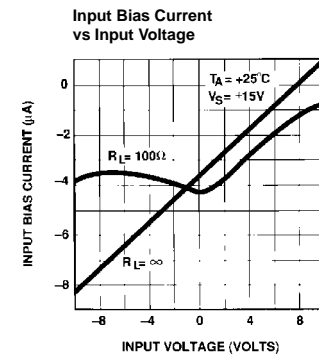
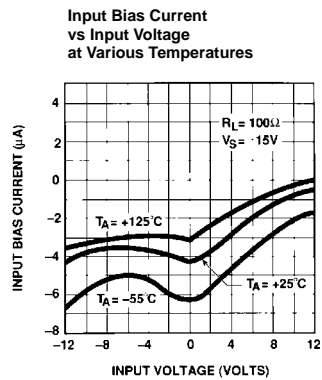
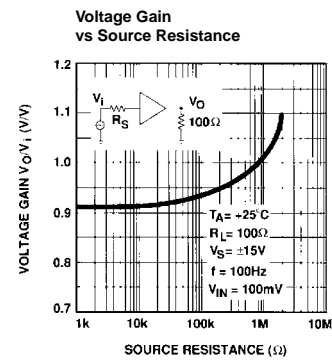
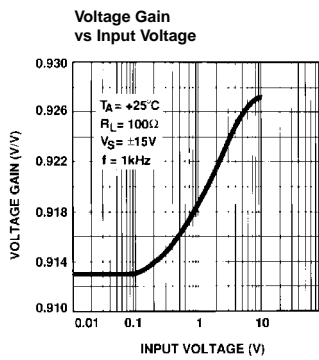
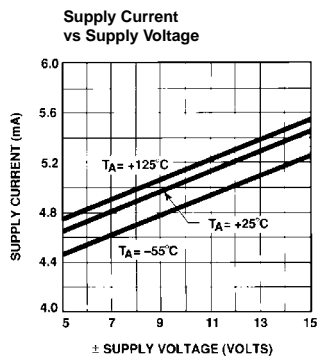
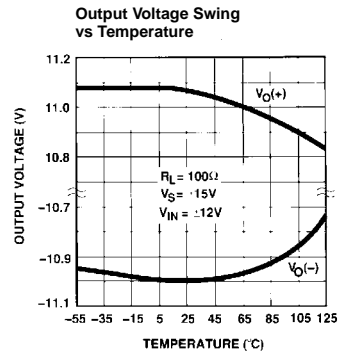
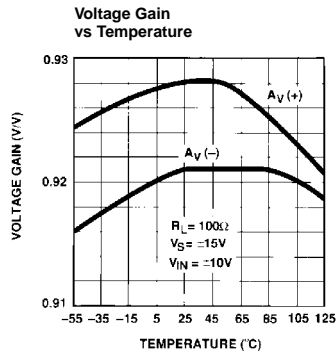
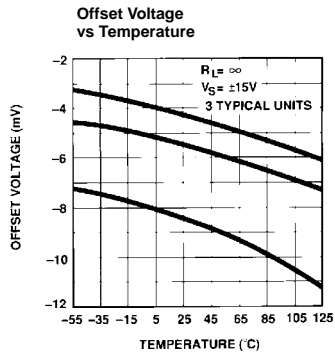
Electrical Specifications $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified. (Continued)

| PARAMETER | DESCRIPTION | TEST CONDITIONS | | | LIMITS | | | UNITS |
|-----------|--------------------|-----------------|-------------|--------------|--------|------|-----|------------|
| | | V_{IN} | LOAD | TEMP | MIN | TYP | MAX | |
| SR | Slew Rate (Note 3) | $\pm 10V$ | 100Ω | $25^\circ C$ | 1200 | 2000 | | V/ μs |

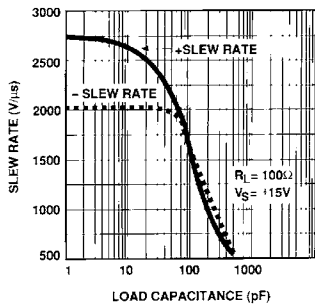
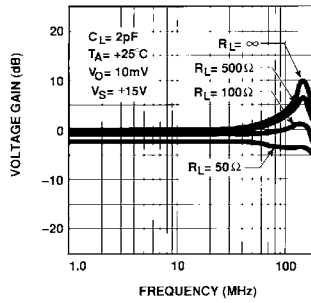
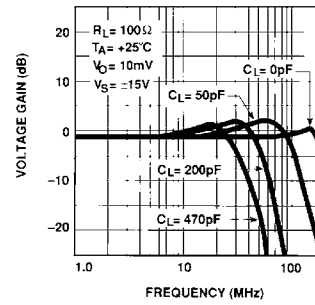
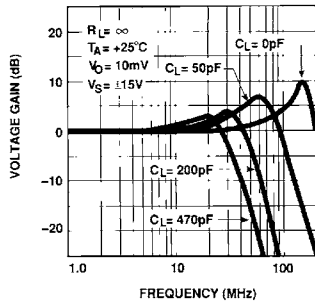
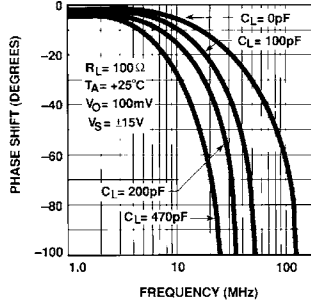
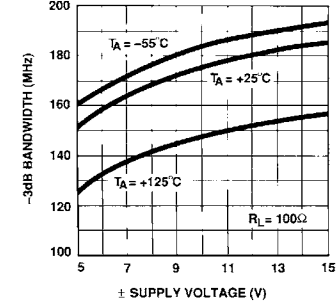
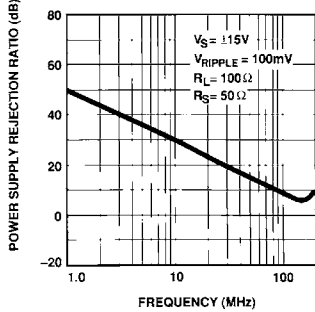
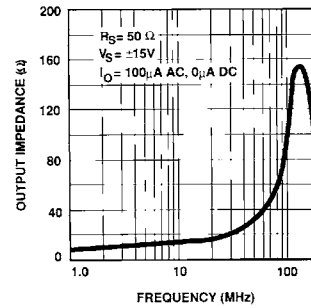
NOTES:

1. Force the input to +12V and the output to +10V and measure the output current. Repeat with -12V_{IN} and -10V on the output.
2. V_{OS} is measured at $V_{S+} = +4.5V$, $V_{S-} = -4.5V$ and $V_{S+} = +18V$, $V_{S-} = 18V$. Both supplies are changed simultaneously.
3. Slew rate is measured between $V_{OUT} = +5V$ and -5V.

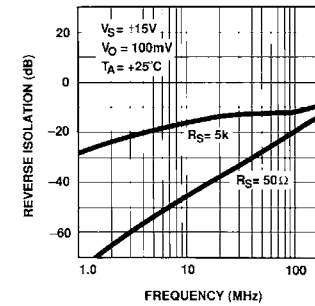
Typical Performance Curves



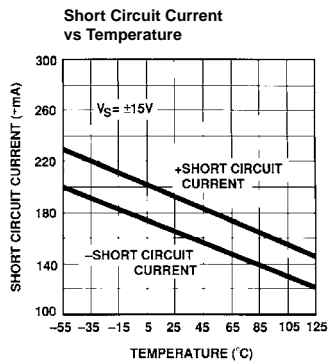
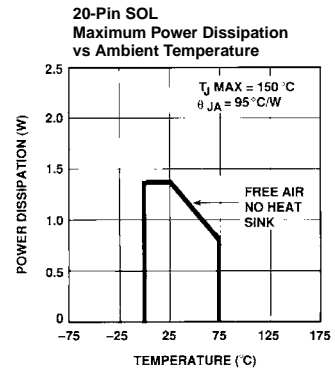
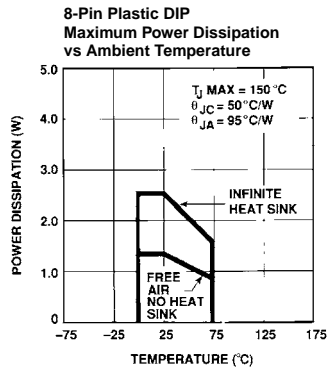
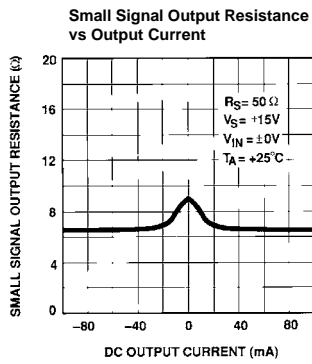
Typical Performance Curves (Continued)

Slew Rate
vs Load CapacitanceVoltage Gain vs Frequency
for Various Resistive LoadsVoltage Gain
vs Frequency for Various
Capacitive Loads; $R_L = 100\Omega$ Voltage Gain
vs Frequency for Various
Capacitive Loads; $R_L = \infty$ Phase Shift vs Frequency
for Various Capacitive Loads-3dB Bandwidth
vs Supply VoltagePower Supply Rejection Ratio
vs FrequencyOutput Impedance vs
Frequency

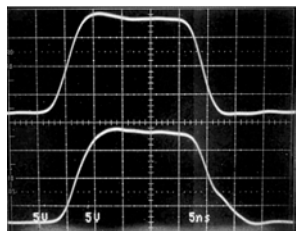
Reverse Isolation vs Frequency



Typical Performance Curves (Continued)



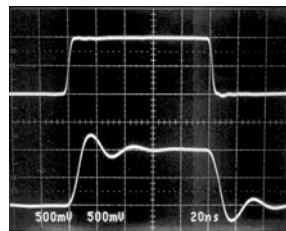
Large Signal Response



← 0V INPUT

← 0V OUTPUT
 $R_L = 100\Omega$
 $C_L = 10pF$
 $f = 20MHz$

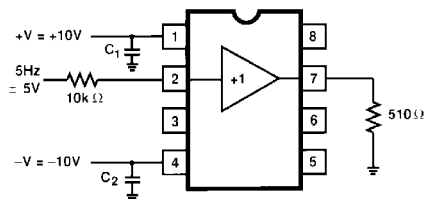
Small Signal Response



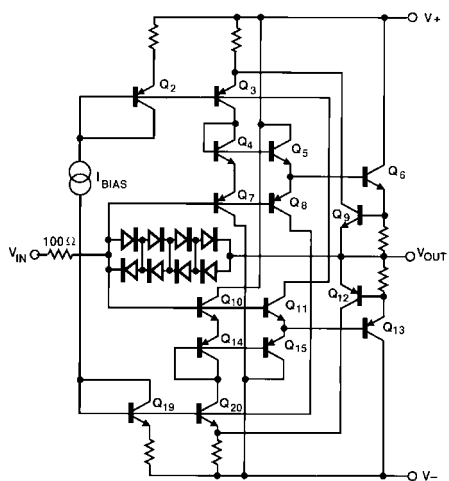
← 0V INPUT

← 0V OUTPUT
 $R_L = \infty$
 $C_L = 220pF$
 $f = 5MHz$

Burn-In Circuit



Simplified Schematic



Application Information

The EL2002 is a monolithic buffer amplifier built on Elantec's proprietary dielectric isolation process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2002 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2001's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 2000V/μs slew rates with 100Ω loads possible with very low supply current.

Power Supplies

The EL2002 may be operated with single or split supplies with total voltage difference between 10V (±5V) and 36V (±18V). It is not necessary to use equal split value supplies. For example -5V and +12V would be excellent for signals from -2V to +9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum, 1μF tantalum capacitor with short leads should be used for both supplies.

Input Characteristics

The input to the EL2002 looks like a resistance in parallel with about 3.5pF in addition to a DC bias current. The DC bias current is due to the mismatch in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (R_{IN}) is affected by the output load, beta and the internal boost. R_{IN} can actually appear negative over portions of the input range; typical input current curves are shown in the characteristic curves. Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about ±2.5V input to output differential. When that happens, the input resistance drops dramatically. The diodes are rated at 50mA. When conducting they have a series resistance of about 20Ω. There is also 100Ω in series with the input that limits input current. Above ±7.5V differential input to output, additional series resistance should be added.

Source Impedance

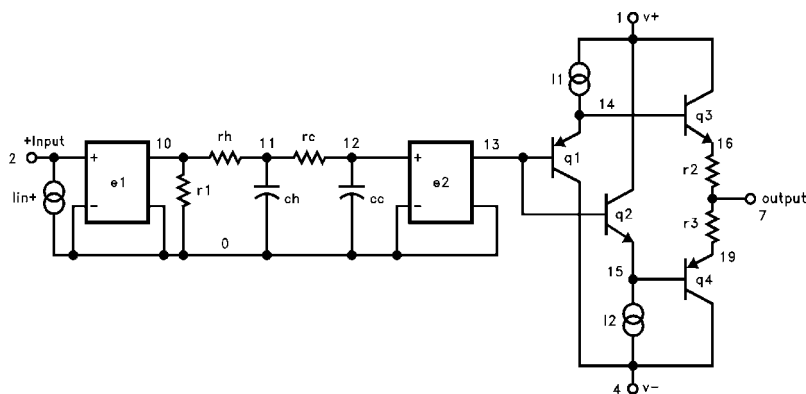
The EL2002 has good input to output isolation. When the buffer is not used in a feedback loop, capacitive and resistive sources up to 1MHz present no oscillation problems. Care must be used in board layout to minimize output to input coupling. CAUTION: When using high source impedances ($R_S > 100kΩ$), significant gain errors can be observed due to output offset, load resistor, and the action of the boost circuit. See typical performance curves.

EL2002 Macromodel

```
* Connections:
```

| | | | | |
|---|--|--|----------|--------|
| * | | | +Vsupply | |
| * | | | -Vsupply | |
| * | | | | output |
| * | | | | |

```
.subckt M2002      2      1      4      7  
* Input Stage  
e1 10 0 2 0 1.0  
r1 10 0 1K  
rh 10 11 150  
ch 11 0 2pF  
rc 11 12 100  
cc 12 0 3pF  
e2 13 0 12 0 1.0  
* Output Stage  
q1 4 13 14 qp  
q2 1 13 15 qn  
q3 1 14 16 qn  
q4 4 15 19 qp  
r2 16 7 1  
r3 19 7 1  
i1 1 14 2mA  
i2 15 4 2mA  
* Bias Current  
iin+ 2 0 3uA  
* Models  
.model qn npn(is=5e-15 bf=150 rb=200 ptf=45 tf=0.1nS)  
.model qp pnp(is=5e-15 bf=150 rb=200 ptf=45 tf=0.1nS)  
.ends
```



All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com