

## Low Cost, Gain of 1, Video Op Amp



The EL2110 operational amplifier, built using Elantec's complementary bipolar process, offers unprecedented high

frequency performance at a very low cost. It is suitable for any application, such as consumer video, where traditional DC performance specifications are of secondary importance to the high frequency specifications. On a 5V supply at a gain of +1 the EL2110 will drive a 150Ω load to +2V, with a bandwidth of 50MHz. This device achieves 0.1dB bandwidth at 5MHz.

The recommended power supply voltage is 5V. At zero and 5V supplies, the inputs will operate to ground. When the outputs are at 0V the amplifier draws only 2.4mA of supply current.

## Features

- Optimized for 5V operation
- Stable at gain of 1
- 50MHz gain bandwidth product
- 130V/μs slew rate
- Drives 150Ω load to video levels
- Input and outputs operate at negative supply rail

## Applications

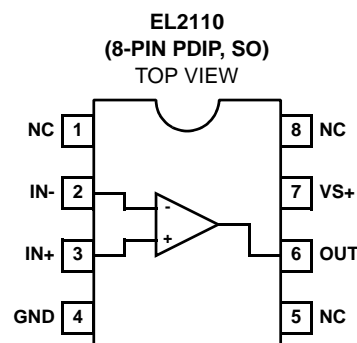
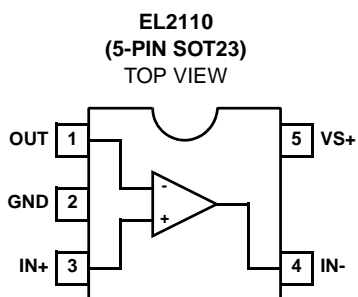
- Consumer video amplifier
- Active filters/integrators
- Cost sensitive applications
- Single supply amplifiers

## Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. NO.
EL2110CN	8-Pin PDIP	-	MDP0031
EL2110CS	8-Pin SO	-	MDP0027
EL2110CW	5-Pin SOT-23*	-	MDP0038

\*EL2110CW symbol is .Dxxx where xxx represents date code

## Pinouts



**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$ )

Total Supply Voltage .....18V  
 Input Voltage .....-6V<sub>S</sub>  
 Differential Input Voltage .....6V  
 Peak Output Current .....75mA per amplifier

Power Dissipation ..... See Curves  
 Storage Temperature Range .....-65°C to +150°C  
 Operating Temperature Range ..... -40°C to +85°C

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**IMPORTANT NOTE:** All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

**DC Electrical Specifications**  $V_S = +5\text{V}$ ,  $R_L = 1\text{k}\Omega$ ,  $V_{IN} = 1\text{V}$ ,  $T_A = 25^\circ\text{C}$  unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OS}$	Input Offset Voltage		-20	10	20	mV
$TCV_{OS}$	Average Offset Voltage Drift	(Note 1)		-50		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current		-15	-7	-3	$\mu\text{A}$
$I_{OS}$	Input Offset Current		-1	0.3	1.0	$\mu\text{A}$
$TCI_{OS}$	Average Offset Current Drift	(Note 1)		-3		$\text{nA}/^\circ\text{C}$
$A_{VOL}$	Open Loop Gain	$V_{OUT} = 0.5, 2.5, R_L = 1\text{k}\Omega$	160	250		V/V
		$V_{OUT} = 0.5, 2.5, R_L = 150\text{k}\Omega$	160	250		V/V
PSRR	Power Supply Rejection Ratio	$V_S = 4.5\text{V}$ to $5.5\text{V}$	43	50		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = 0\text{V}$ to $3.8\text{V}$	55	65		dB
CMIR	Common Mode Input Range		0.0		3.0	V
$V_{OUT}$	Output Voltage Swing	$R_{FB} = R_G = 1\text{k}\Omega$ , $R_L = 150\Omega$	2.8	3.2		V
$I_{SC}$	Output Short Circuit Current	Output to Ground (Note 2)	75	125		mA
$I_S$	Supply Current	No load (per channel) $V_{IN} = 0\text{V}$	2.0	2.4	3.0	mA
$R_{IN}$	Input Resistance	Differential		150		$\text{k}\Omega$
		Common mode		1.5		$\text{M}\Omega$
$C_{IN}$	Input Capacitance	$A_V = 1$ @ 10MHz		1		pF
$R_{OUT}$	Output Resistance			0.150		W
PSOR	Power Supply Operating Range	Single supply	4		6	V

## NOTES:

1. Measured from  $T_{MIN}$  to  $T_{MAX}$ .
2. A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.

**Closed-Loop AC Electrical Specifications**  $V_S = 5\text{V}$ , AC Test Figure,  $T_A = 25^\circ\text{C}$  unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
BW	-3dB Bandwidth ( $V_{OUT} = 0.4\text{mV}_{P-P}$ )	$A_V = 1$		100		MHz
	$\pm 0.1\text{dB}$ Bandwidth ( $V_{OUT} = 0.4\text{mV}_{P-P}$ )	$A_V = 1$		10		MHz
GBWP	Gain Bandwidth Product			50		MHz
PM	Phase Margin			55		°
SR	Slew Rate		85	130		$\text{V}/\mu\text{s}$
FBWP	Full Power Bandwidth	(Note 1)	8	11		MHz
$t_R, t_F$	Rise Time, Fall Time	0.1V step		2		ns
OS	Overshoot	0.1V step		15		%

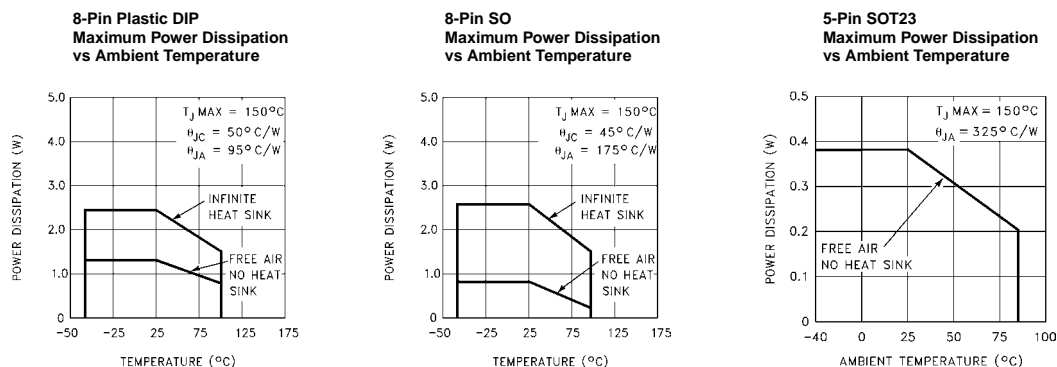
**Closed-Loop AC Electrical Specifications** $V_S = 5V$ , AC Test Figure,  $T_A = 25^\circ C$  unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD}$	Propagation Delay			3.5		ns
$t_S$	Settling to 0.1% ( $A_V = 1$ )	$V_S = 5V$ , 2V step		80		ns
dG	Differential Gain (Note 2)	NTSC/PAL		0.1		%
dP	Differential Phase (Note 2)	NTSC/PAL		0.2		°
$e_N$	Input Noise Voltage	10kHz		15		nV/ $\sqrt{Hz}$
$i_N$	Input Noise Current	10kHz		1.5		nV/ $\sqrt{Hz}$
CS	Channel Separation	P = 5MHz		55		dB

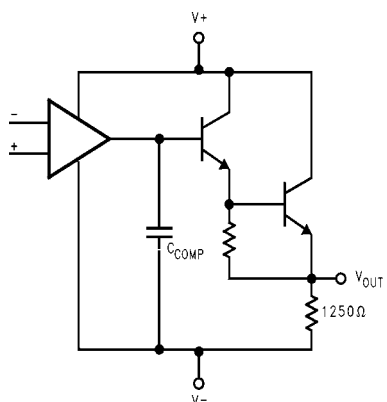
## NOTES:

1. For  $V_S = 5V$ ,  $V_{OUT} = 4V_{P-P}$  Full power bandwidth is based on slew rate measurement using:  $FPBW = SR/(2\pi \cdot V_{PEAK})$
2. Video performance measured at  $V_S = 5V$ ,  $A_V = 2$  with 2 times normal video level across  $R_L = 150\Omega$

## Typical Performance Curves



## Simplified Block Diagram



## Applications Information

### Product Description

The EL2110 operational amplifier is stable at a gain of 1. It is built on Elantec's proprietary complimentary bipolar process. This topology allows it to be used in a variety of applications where current mode amplifiers are not appropriate because of restrictions placed on the feedback elements. This product is especially designed for applications where high bandwidth and good video performance characteristics are desired but the higher cost of more flexible and sophisticated products are prohibitive.

### Power Supplies

The EL2110 is designed to work at a supply voltage difference of 4.5V to 5.5V. It will work on any combination of

$\pm$  supplies. All electrical characteristics are measured with a 5V supply.

### Output Swing vs Load

Please refer to the simplified block diagram. This amplifier provides an NPN pull-up transistor output and a passive 1250Ω pull-down resistor to the most negative supply. In an application where the load is connected to  $V_{S-}$  the output voltage can swing to within 200mV of  $V_{S-}$ .

### Output Drive Capability

This device does not have short circuit protection. Each output is capable of than 100mA into a shorted output. Care must be used in the design to limit the output current with a series resistor.

### Single 5V Supply Video Cable Driver

These amplifiers may be used as a direct coupled video cable driver with a gain of 2. With a 75Ω back matching resistor driving a terminated 75Ω cable the output at the cable load will be original video level (1V NTSC). The best operating mode is with direct coupling. The input signal must be offset to keep the entire signal within the range of the amplifier. The required offset voltage can be set with a resistor divider and a bypass capacitor in the video path (Figure 1). The input DC offset should be between 0.3V and 0.5V. With  $R_A = 68\text{k}$  and  $R_B = 4.7\text{k}$  the input offset will be 0.32V. Since these amplifiers require a DC load at their outputs it is good design practice to add a 250Ω resistor to ground directly at the amplifier output. Then if the 75Ω cable termination resistor were inadvertently removed there would still be an output signal. The values in Figure 1 give an output range of 0V to 2.6V.

Output capacitive coupling also has some restrictions. These amplifiers require a DC load at their outputs. A 75Ω back

matching resistor to a cable and a  $75\Omega$  load to ground at the end of the cable provide a  $150\Omega$  DC load. But output capacitive coupling opens this DC path so an extra pulldown resistor on the amplifier output to ground is required. Figure 4 shows a  $250\Omega$  resistor. Capacitively coupling the output will require that we shift the output offset voltage higher than in the direct coupled case. Using  $R_A = 43k$  and  $R_B = 4.7k$  will make the quiescent output offset voltage about 1V. The output dynamic range will be 0.6V to 3V.

Input capacitive coupling will increase the needed dynamic range of the amplifier. The standard NTSC video signal is 1V peak to peak plus 143mV for the color AC peak. The video signal is made up of the -286mV sync pulse plus the 714mV picture signal which may vary from 0V to 714mV. The video signal average value for a black picture is about 28mV

(Figure 2) and with a white picture level is about 583mV (Figure 3). This gives a maximum change in average value of about 555mV. A direct coupled amplifier with a standard NTSC video signal needs a dynamic range of 1.143V. But with input capacitance coupling the dynamic range requirements are the sum of the 1.143V video plus the average picture value change of 0.555V or 1.698V<sub>P-P</sub>. At a gain of two this doubles to 3.394V. These amplifiers do not have this much dynamic range so a gain of less than 2 must be used to avoid waveform compression under all conditions.

Capacitively coupling the input and output is worse than a capacitor only on the input. Without any special compromises you can only take a gain of one. But if the backmatch resistor is reduced to  $36\Omega$ , reducing the output

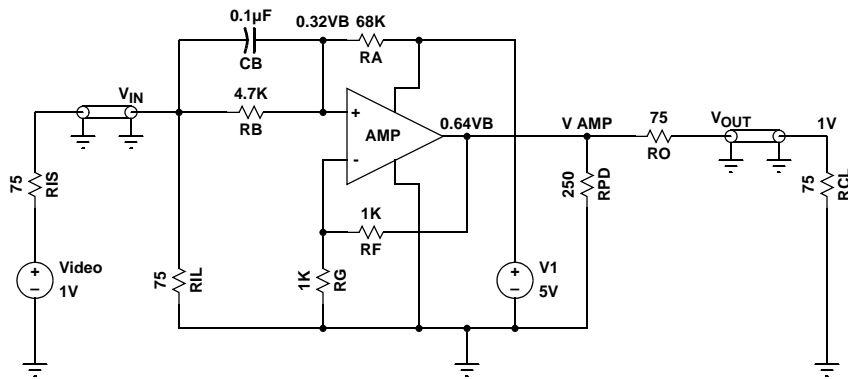


FIGURE 1. VIDEO PATH

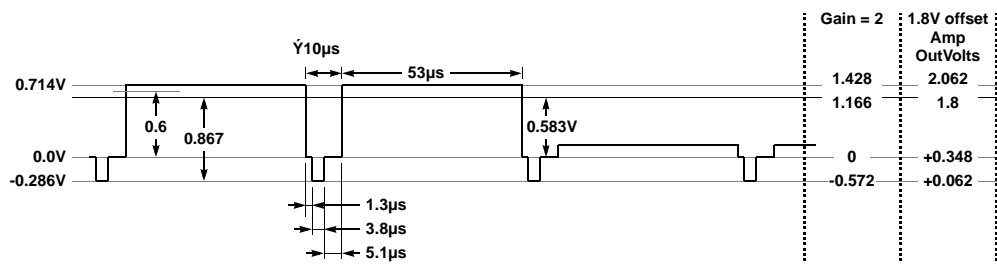


FIGURE 2. WHITE LEVEL VIDEO

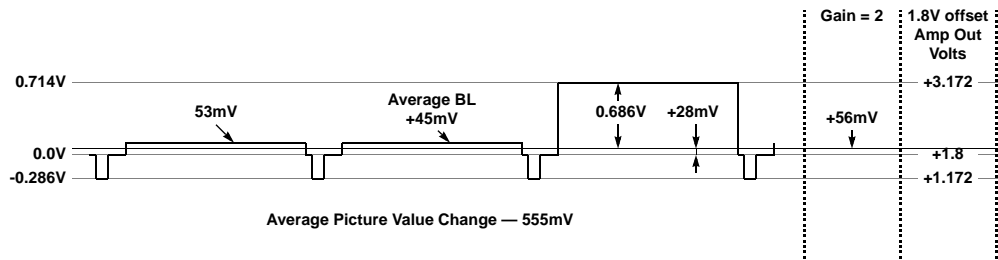


FIGURE 3. BLACK LEVEL VIDEO

range requirement 25% and the output offset is shifted to 2.1V you can take a gain of 1.5 and have a standard NTSC 1V at the 75 $\Omega$  load.

A simple transistor, capacitor and resistor sync tip clamp may be used when the input is already AC coupled to set the sync tip to ground. This gives the input a fixed DC level and can be used like a direct coupled input. The clamp uses a PNP transistor with the collector at ground and the base has a 200k $\Omega$  resistor to 5V. The emitter connects to the amplifier input and a capacitor from the video input. The clamp functions as an inverted Beta current source for input bias current with plus inputs and a clamp to ground for minus inputs. The  $R_A$  and  $R_B$  resistors are removed for the clamp option (Figure 4).

### Printed Circuit Layout

The EL2110 is well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 $\mu$ F ceramic capacitor is recommended for bypassing both supplies. Pin lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5k $\Omega$  because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

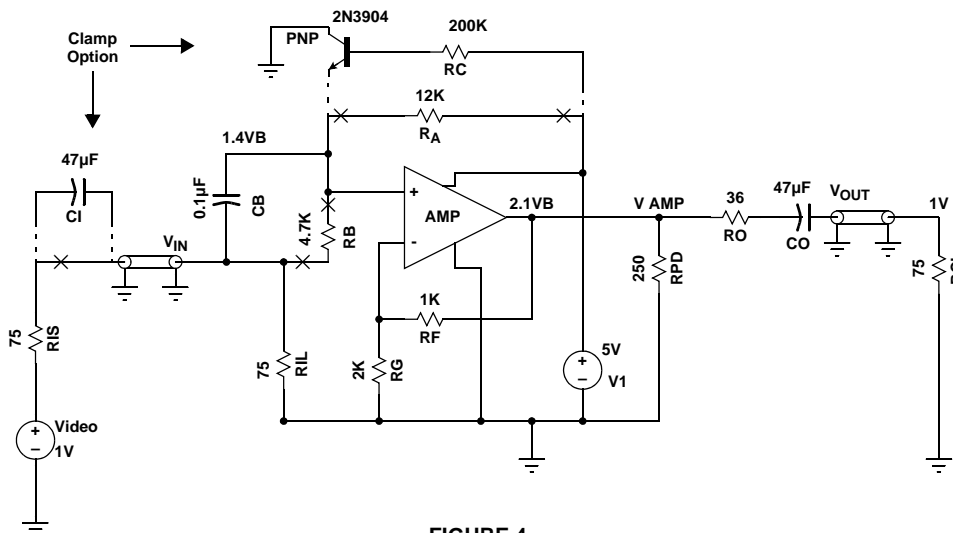


FIGURE 4.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.  
Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)