

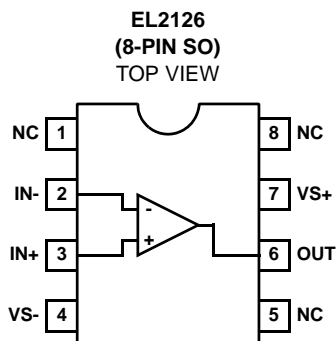
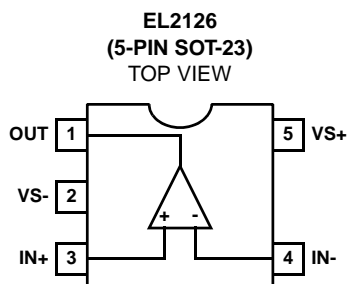
Ultra-Low Noise, Low Power, Wideband Amplifier

The EL2126 is an ultra-low noise, wideband amplifier that runs on half the supply current of competitive parts. It is intended for use in systems such as ultrasound imaging where a very small signal needs to be amplified by a large amount without adding significant noise. Its low power dissipation enables it to be packaged in the tiny SOT-23 package, which further helps systems where many input channels create both space and power dissipation problems.

The EL2126 is stable for gains of 10 and greater and uses traditional voltage feedback. This allows the use of reactive elements in the feedback loop, a common requirement for many filter topologies. It operates from $\pm 2.5V$ to $\pm 15V$ supplies and is available in the 5-pin SOT-23 and 8-pin SO packages.

The EL2126 is fabricated in Elantec's proprietary complementary bipolar process, and is specified for operation over the full $-40^{\circ}C$ to $+85^{\circ}C$ temperature range.

Pinouts



Features

- Voltage noise of only $1.3nV/\sqrt{Hz}$
- Current noise of only $1.2pA/\sqrt{Hz}$
- $200\mu V$ offset voltage
- 100MHz -3dB BW for $A_V = 10$
- Very low supply current - 4.7mA
- SOT-23 package
- $\pm 2.5V$ to $\pm 15V$ operation
- Pb-Free available (RoHS compliant)

Applications

- Ultrasound input amplifiers
- Wideband instrumentation
- Communication equipment
- AGC & PLL active filters
- Wideband sensors

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL2126CW-T7	5-Pin SOT-23	7" (3K pcs)	MDP0038
EL2126CW-T7A	5-Pin SOT-23	7" (250 pcs)	MDP0038
EL2126CS	8-Pin SO	-	MDP0027
EL2126CS-T7	8-Pin SO	7"	MDP0027
EL2126CS-T13	8-Pin SO	13"	MDP0027
EL2126CSZ (See Note)	8-Pin SO (Pb-free)	-	MDP0027
EL2126CSZ-T7 (See Note)	8-Pin SO (Pb-free)	7"	MDP0027
EL2126CSZ-T13 (See Note)	8-Pin SO (Pb-free)	13"	MDP0027

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

V_{S+} to V_{S-} 33V
 Continuous Output Current 40mA
 Any Input $V_{S+} - 0.3\text{V}$ to $V_{S-} + 0.3\text{V}$
 Power Dissipation See Curves

Operating Temperature -40°C to $+85^\circ\text{C}$
 Storage Temperature -60°C to $+150^\circ\text{C}$
 Maximum Die Junction Temperature $+150^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications $V_{S+} = +5\text{V}$, $V_{S-} = -5\text{V}$, $T_A = 25^\circ\text{C}$, $R_F = 180\Omega$, $R_G = 20\Omega$, $R_L = 500\Omega$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
V_{OS}	Input Offset Voltage (SO8)			0.2	2	mV
	Input Offset Voltage (SOT23-5)				3	mV
T_{CVOS}	Offset Voltage Temperature Coefficient			17		$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current		-10	-7		μA
I_{OS}	Input Bias Current Offset			0.06	0.6	μA
T_{CIB}	Input Bias Current Temperature Coefficient			0.013		$\mu\text{A}/^\circ\text{C}$
C_{IN}	Input Capacitance			2.2		pF
A_{VOL}	Open Loop Gain	$V_O = -2.5\text{V}$ to $+2.5\text{V}$	80	87		dB
PSRR	Power Supply Rejection Ratio (Note 1)		80	100		dB
CMRR	Common Mode Rejection Ratio	at CMIR	75	106		dB
CMIR	Common Mode Input Range		-4.6		3.8	V
V_{OUTH}	Positive Output Voltage Swing	No load, $R_F = 1\text{k}\Omega$	3.8	3.8		V
V_{OUTL}	Negative Output Voltage Swing	No load, $R_F = 1\text{k}\Omega$		-4	-3.9	V
V_{OUTH2}	Positive Output Voltage Swing	$R_L = 100\Omega$	3.2	3.45		V
V_{OUTL2}	Negative Output Voltage Swing	$R_L = 100\Omega$		-3.5	-3.2	V
I_{OUT}	Output Short Circuit Current (Note 2)		80	100		mA
I_{SY}	Supply Current			4.7	5.5	mA
AC PERFORMANCE - $R_G = 20\Omega$, $C_L = 3\text{pF}$						
BW	-3dB Bandwidth, $R_L = 500\Omega$			100		MHz
BW $\pm 0.1\text{dB}$	$\pm 0.1\text{dB}$ Bandwidth, $R_L = 500\Omega$			17		MHz
BW $\pm 1\text{dB}$	$\pm 1\text{dB}$ Bandwidth, $R_L = 500\Omega$			80		MHz
Peaking	Peaking, $R_L = 500\Omega$			0.6		dB
SR	Slew Rate	$V_{OUT} = 2V_{PP}$, measured at 20% to 80%	80	110		$\text{V}/\mu\text{s}$
OS	Overshoot, 4Vpk-pk Output Square Wave	Positive		2.8		%
		Negative		-7		%
t_S	Settling Time to 0.1% of $\pm 1\text{V}$ Pulse			51		ns
V_N	Voltage Noise Spectral Density			1.3		$\text{nV}/\sqrt{\text{Hz}}$
I_N	Current Noise Spectral Density			1.2		$\text{pA}/\sqrt{\text{Hz}}$

Electrical Specifications $V_{S+} = +5V$, $V_{S-} = -5V$, $T_A = 25^{\circ}C$, $R_F = 180\Omega$, $R_G = 20\Omega$, $R_L = 500\Omega$ unless otherwise specified. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion (Note 3)			-70		dBc
HD3	3rd Harmonic Distortion (Note 3)			-70		dBc

NOTES:

1. Measured by moving the supplies from $\pm 4V$ to $\pm 6V$
2. Pulse test only and using a 10Ω load
3. Frequency = 1MHz, $V_{OUT} = 2V_{pk-pk}$, into 500Ω and 5pF load

Electrical Specifications $V_{S+} = +15V$, $V_{S-} = -15V$, $T_A = 25^{\circ}C$, $R_F = 180\Omega$, $R_G = 20\Omega$, $R_L = 500\Omega$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
V_{OS}	Input Offset Voltage (SO8)			0.5	3	mV
	Input Offset Voltage (SOT23-5)				3	mV
T_{CVOS}	Offset Voltage Temperature Coefficient			4.5		$\mu V/^{\circ}C$
I_B	Input Bias Current		-10	-7		μA
I_{OS}	Input Bias Current Offset			0.12	0.7	μA
T_{CIB}	Input Bias Current Temperature Coefficient			0.016		$\mu A/^{\circ}C$
C_{IN}	Input Capacitance			2.2		pF
A_{VOL}	Open Loop Gain		80	90		dB
PSRR	Power Supply Rejection Ratio (Note 1)		65	80		dB
CMRR	Common Mode Rejection Ratio	at CMIR	70	85		dB
CMIR	Common Mode Input Range		-14.6		13.8	V
V_{OUTH}	Positive Output Voltage Swing	No load, $R_F = 1k\Omega$	13.6	13.7		V
V_{OUTL}	Negative Output Voltage Swing	No load, $R_F = 1k\Omega$		-13.8	-13.7	V
V_{OUTH2}	Positive Output Voltage Swing	$R_L = 100\Omega$, $R_F = 1k\Omega$	10.2	11.2		V
V_{OUTL2}	Negative Output Voltage Swing	$R_L = 100\Omega$, $R_F = 1k\Omega$		-10.3	-9.5	V
I_{OUT}	Output Short Circuit Current (Note 2)		140	220		mA
I_{SY}	Supply Current			5	6	mA
AC PERFORMANCE - $R_G = 20\Omega$, $C_L = 3pF$						
BW	-3dB Bandwidth, $R_L = 500\Omega$			135		MHz
BW $\pm 0.1dB$	$\pm 0.1dB$ Bandwidth, $R_L = 500\Omega$			26		MHz
BW $\pm 1dB$	$\pm 1dB$ Bandwidth, $R_L = 500\Omega$			60		MHz
Peaking	Peaking, $R_L = 500\Omega$			2.1		dB
SR	Slew Rate ($\pm 2.5V$ Square Wave, Measured 25%-75%)		130	150		V/ μS
OS	Overshoot, 4Vpk-pk Output Square Wave	Positive		1.6		%
		Negative		-4.4		%
T_S	Settling Time to 0.1% of $\pm 1V$ Pulse			48		ns
V_N	Voltage Noise Spectral Density			1.4		nV/ \sqrt{Hz}

Electrical Specifications $V_{S+} = +15V$, $V_{S-} = -15V$, $T_A = 25^{\circ}C$, $R_F = 180\Omega$, $R_G = 20\Omega$, $R_L = 500\Omega$ unless otherwise specified. **(Continued)**

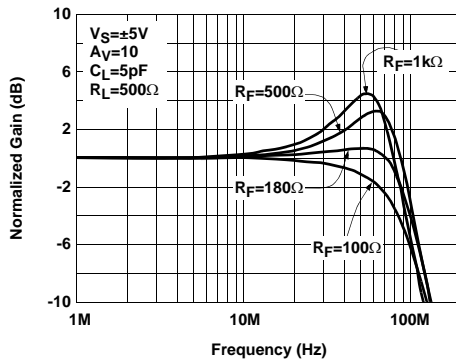
PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
I_N	Current Noise Spectral Density			1.1		pA/ \sqrt{Hz}
HD2	2nd Harmonic Distortion (Note 3)			-72		dBc
HD3	3rd Harmonic Distortion (Note 3)			-73		dBc

NOTES:

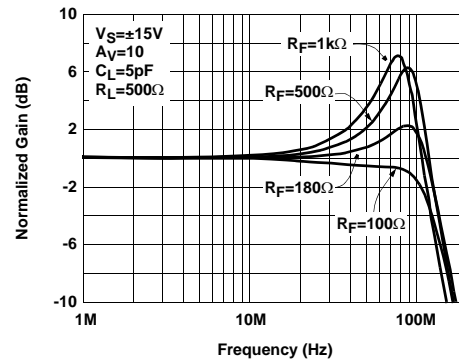
1. Measured by moving the supplies from $\pm 13.5V$ to $\pm 16.5V$
2. Pulse test only and using a 10Ω load
3. Frequency = 1MHz, $V_{OUT} = 2V_{pk-pk}$, into 500Ω and 5pF load

Typical Performance Curves

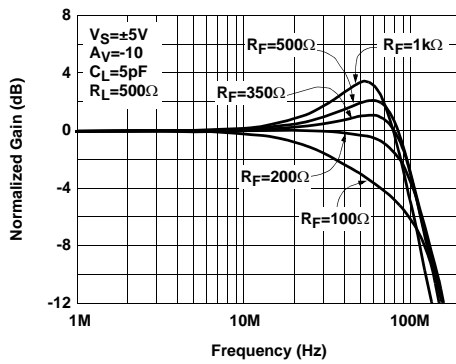
Non-Inverting Frequency Response for Various R_F



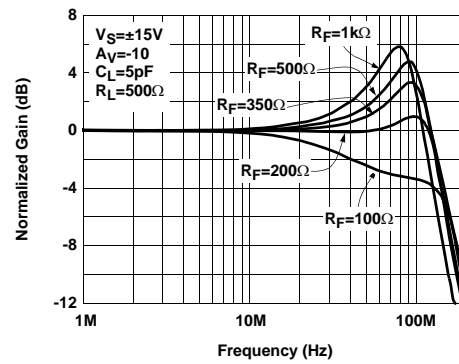
Non-Inverting Frequency Response for Various R_F



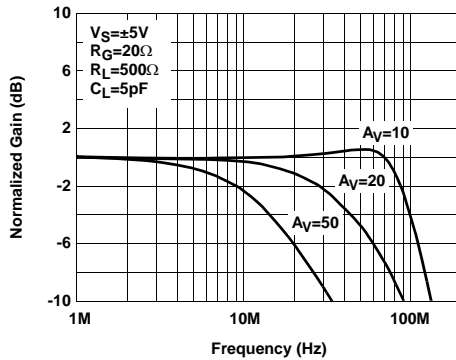
Inverting Frequency Response for Various R_F



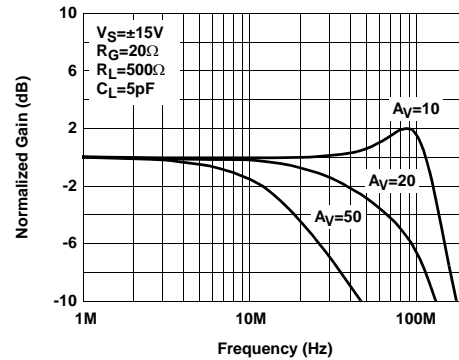
Inverting Frequency Response for Various R_F



Non-Inverting Frequency Response for Various Gain

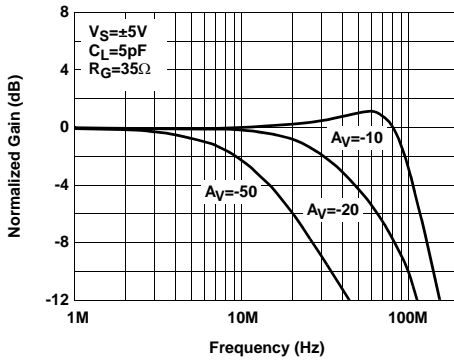


Non-Inverting Frequency Response for Various Gain

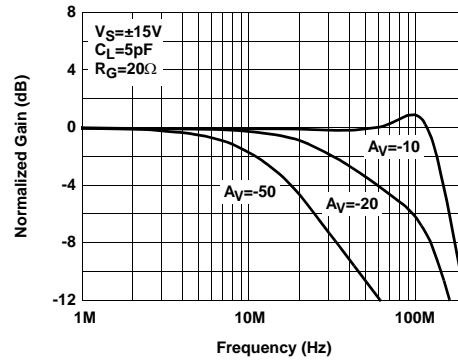


Typical Performance Curves (Continued)

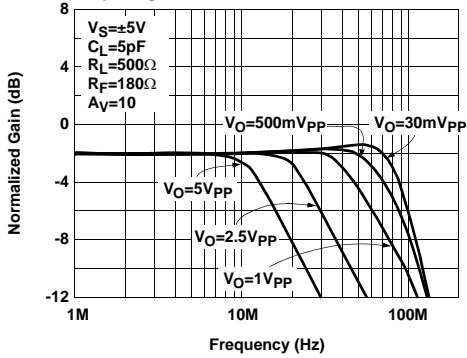
Inverting Frequency Response for Various Gain



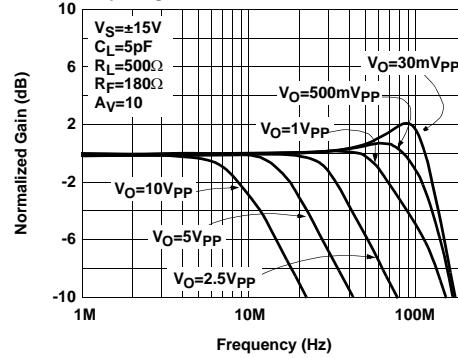
Inverting Frequency Response for Various R_F



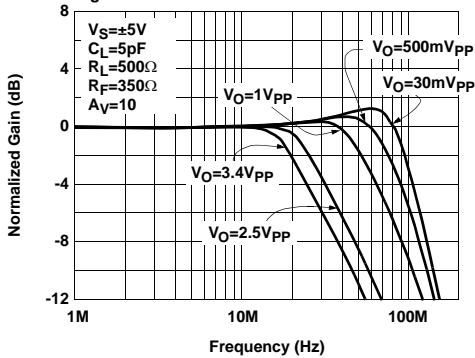
Non-Inverting Frequency Response for Various Output Signal Levels



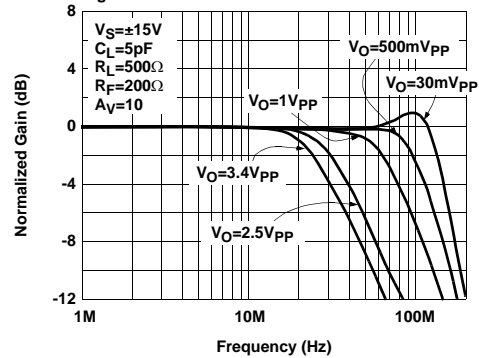
Non-Inverting Frequency Response for Various Output Signal Levels



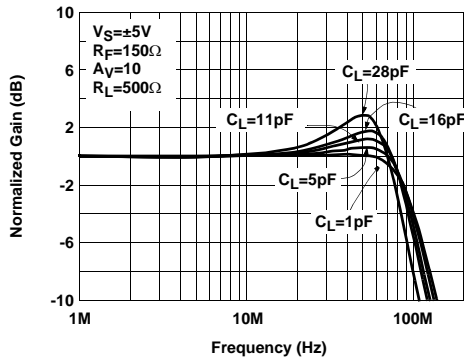
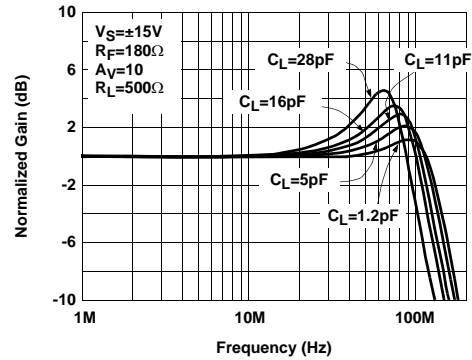
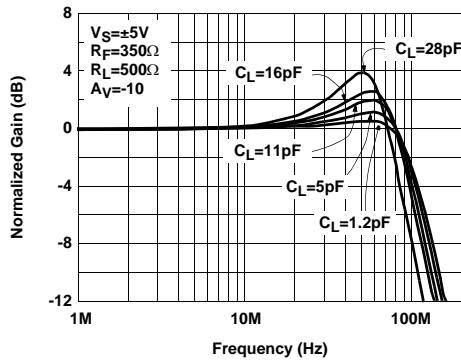
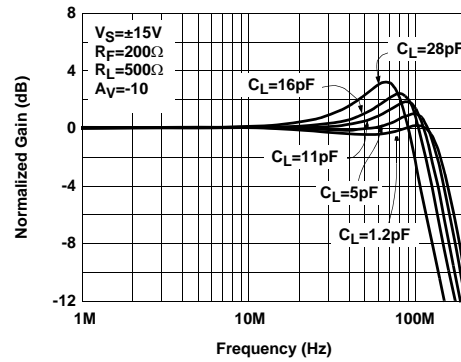
Inverting Frequency Response for Various Output Signal Levels



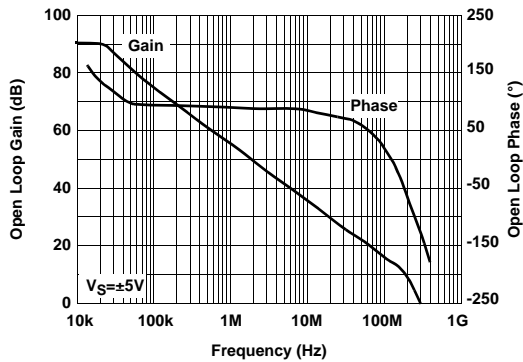
Inverting Frequency Response for Various Output Signal Levels



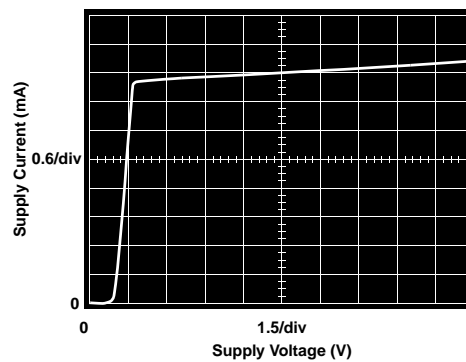
Typical Performance Curves (Continued)

Non-Inverting Frequency Response for Various C_L Non-Inverting Frequency Response for Various C_L Inverting Frequency Response for Various C_L Inverting Frequency Response for Various C_L 

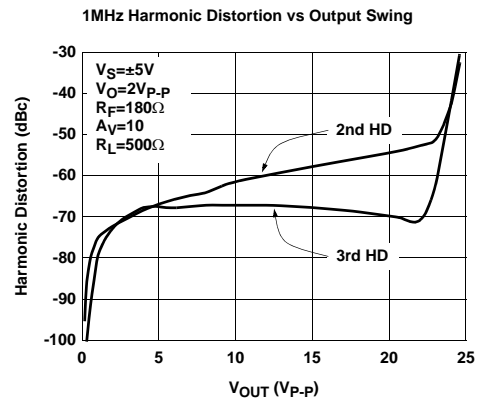
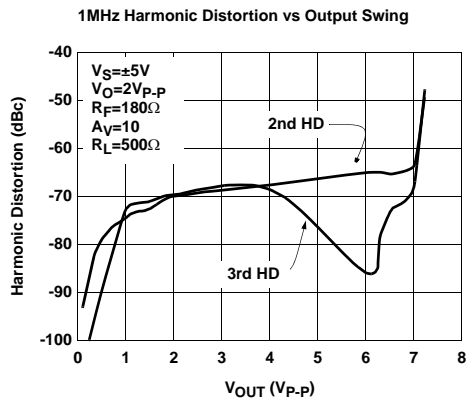
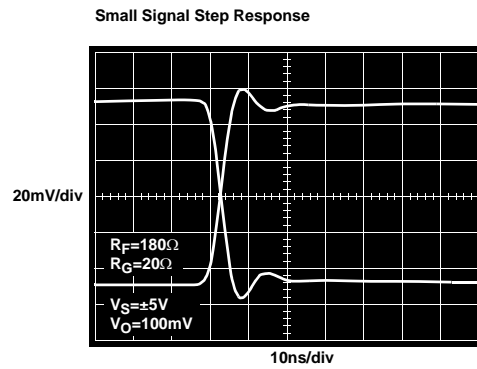
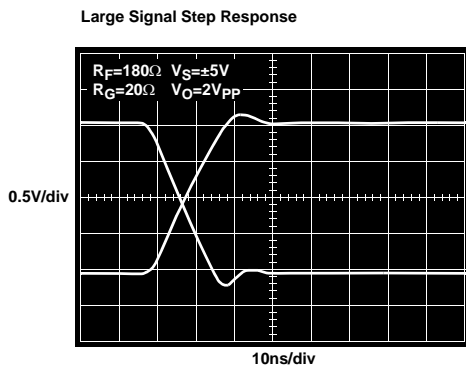
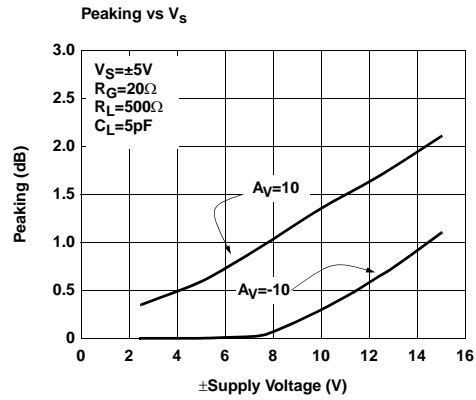
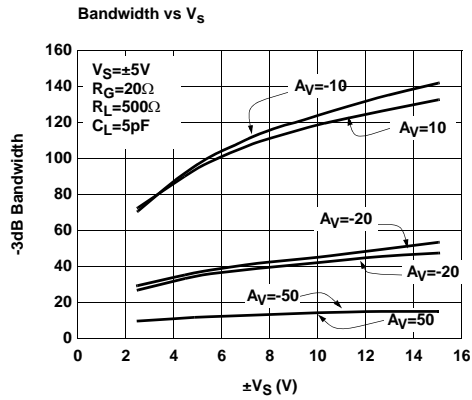
Open Loop Gain/Phase



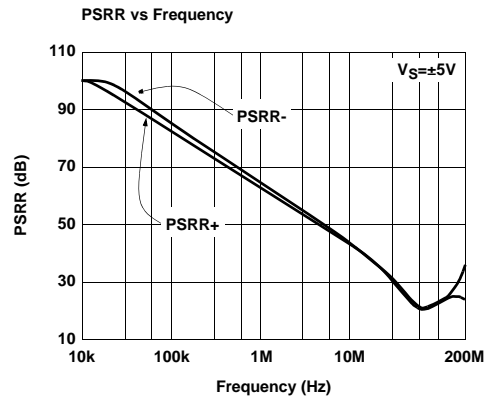
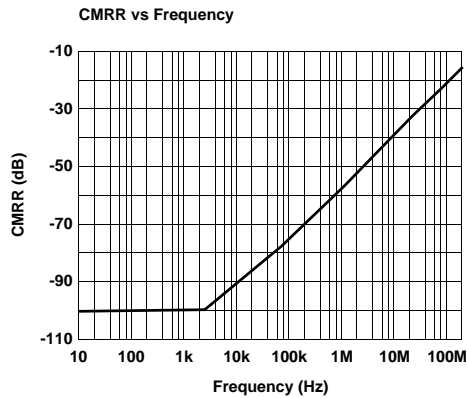
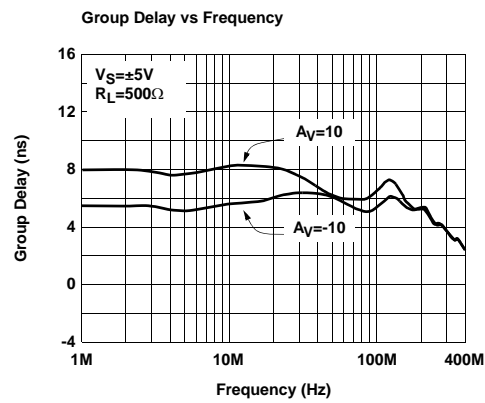
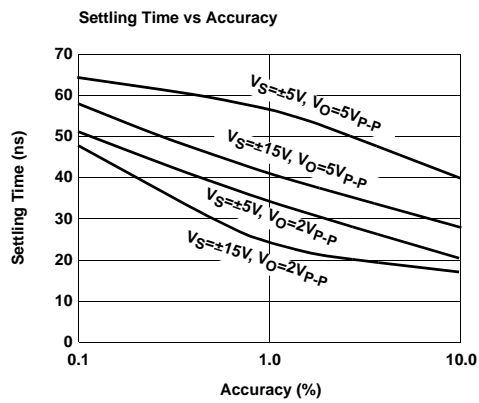
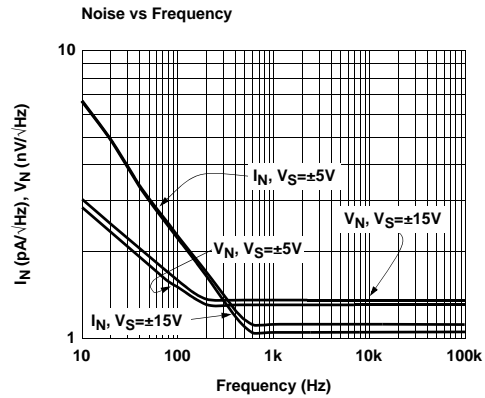
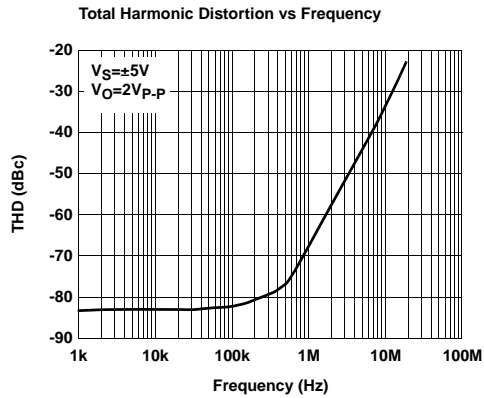
Supply Current vs Supply Voltage



Typical Performance Curves (Continued)

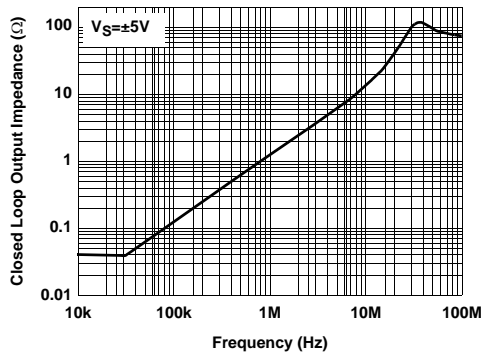


Typical Performance Curves (Continued)

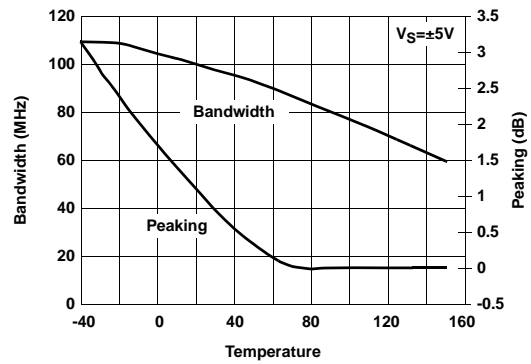


Typical Performance Curves (Continued)

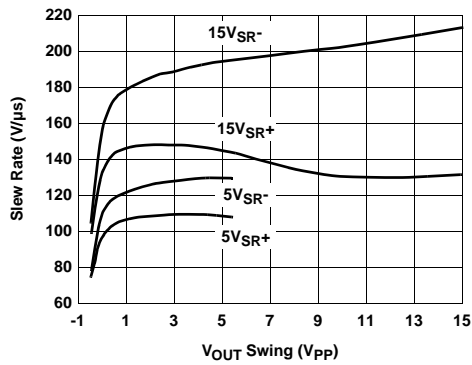
Closed Loop Output Impedance vs Frequency



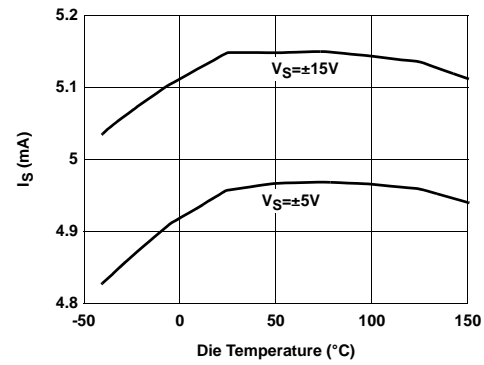
Bandwidth and Peaking vs Temperature



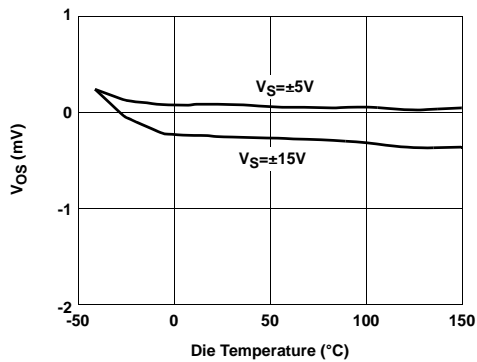
Slew Rate vs Swing



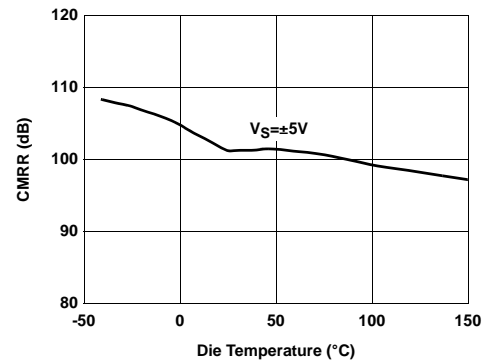
Supply Current vs Temperature



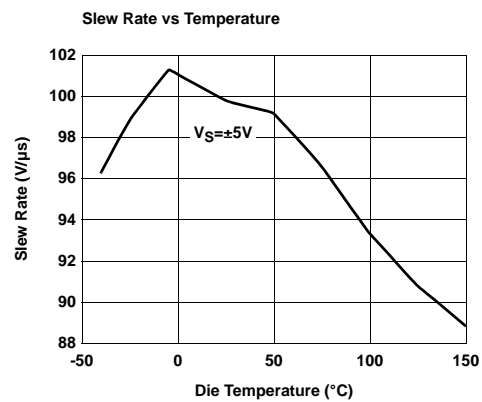
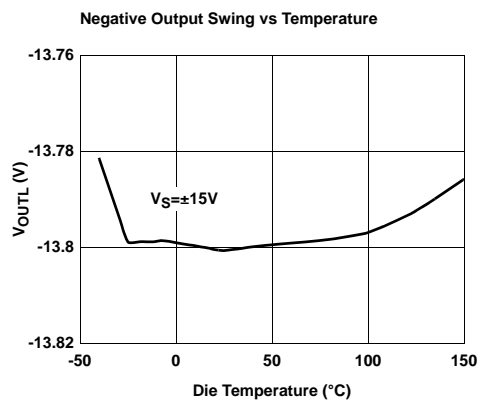
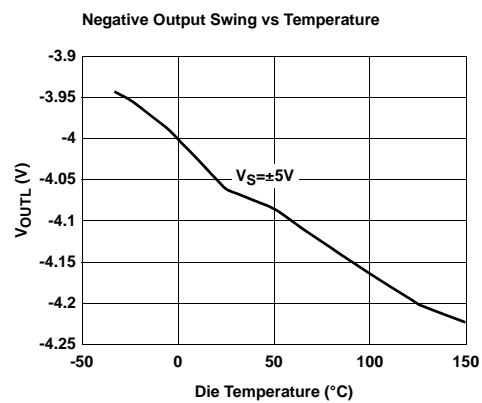
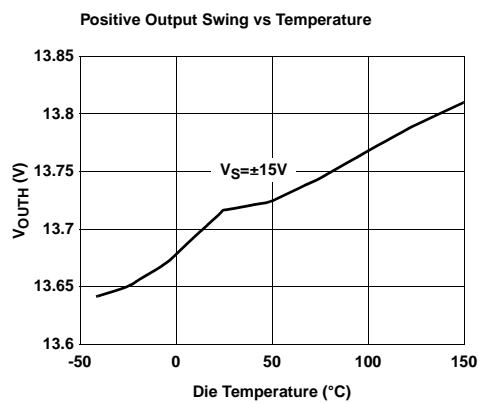
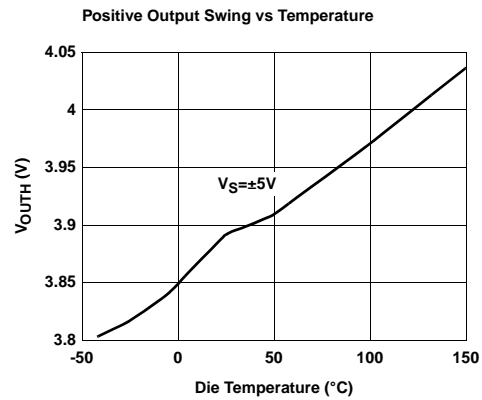
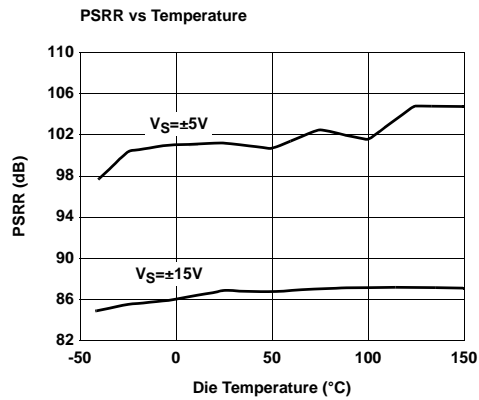
Offset Voltage vs Temperature



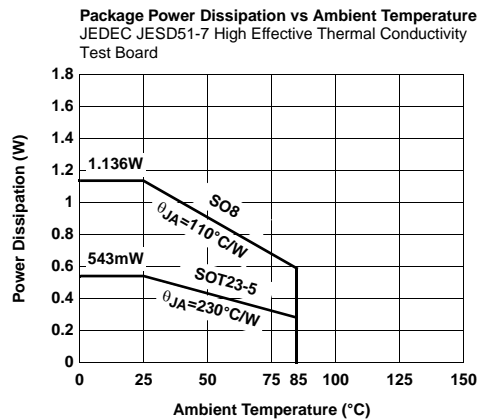
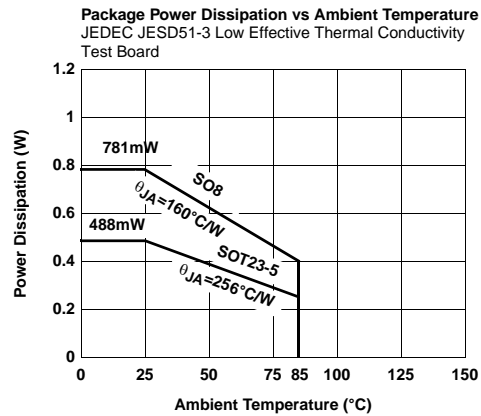
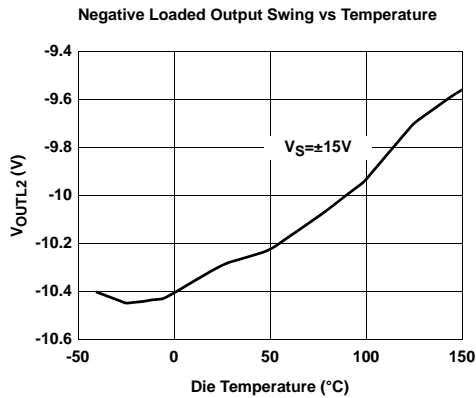
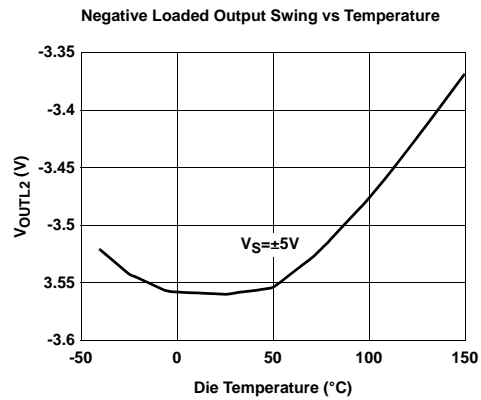
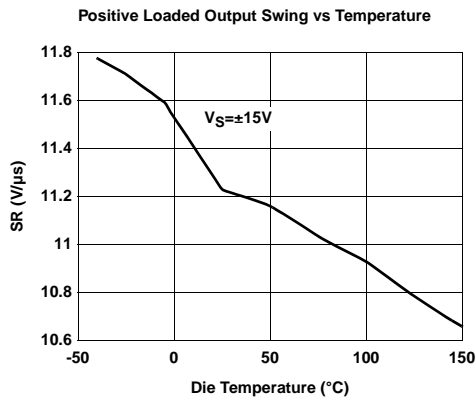
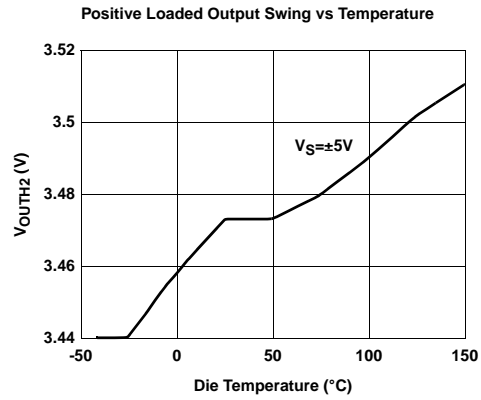
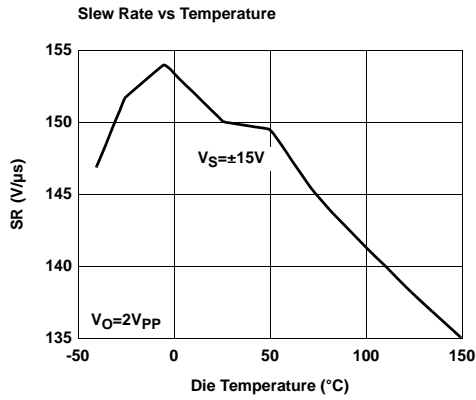
CMRR vs Temperature



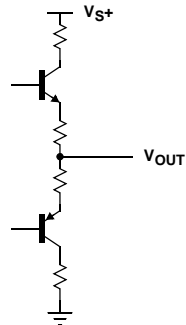
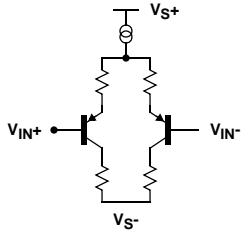
Typical Performance Curves (Continued)



Typical Performance Curves (Continued)



Pin Descriptions

EL2126CW (5-PIN SOT-23)	EL2126CS (8-PIN SO)	PIN NAME	PIN FUNCTION	EQUIVALENT CIRCUIT
1	6	VOUT	Output	 <p>Circuit 1</p>
2	4	VS-	Supply	
3	3	VINA+	Input	 <p>Circuit 2</p>
4	2	VINA-	Input	Reference Circuit 2
5	7	VS+	Supply	

Applications Information

Product Description

The EL2126 is an ultra-low noise, wideband monolithic operational amplifier built on Elantec's proprietary high speed complementary bipolar process. It features 1.3nV/√Hz input voltage noise, 200μV typical offset voltage, and 73dB THD. It is intended for use in systems such as ultrasound imaging where very small signals are needed to be amplified. The EL2126 also has excellent DC specifications: 200μV V_{OS} , 22μA I_B , 0.4μA I_{OS} , and 106dB CMRR. These specifications allow the EL2126 to be used in DC-sensitive applications such as difference amplifiers.

Gain-Bandwidth Product

The EL2126 has a gain-bandwidth product of 650MHz at ±5V. For gains less than 20, higher-order poles in the amplifier's transfer function contribute to even higher closed-loop bandwidths. For example, the EL2126 has a -3dB bandwidth of 100MHz at a gain of 10 and decreases to 33MHz at gain of 20. It is important to note that the extra bandwidth at lower gain does not come at the expenses of stability. Even though the EL2126 is designed for gain ≥ 10. With external compensation, the device can also operate at lower gain settings. The RC network shown in Figure 1 reduces the feedback gain at high frequency and thus maintains the amplifier stability. R values must be less than R_F divided by 9 and 1 divided by $2\pi RC$ must be less than 200MHz.

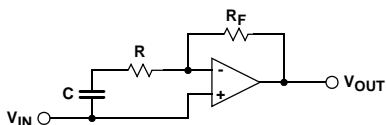


FIGURE 1.

Choice of Feedback Resistor, R_F

The feedback resistor forms a pole with the input capacitance. As this pole becomes larger, phase margin is reduced. This increases ringing in the time domain and peaking in the frequency domain. Therefore, R_F has some maximum value which should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few pF range in parallel with R_F can help to reduce this ringing and peaking at the expense of reducing the bandwidth. Frequency response curves for various R_F values are shown in the typical performance curves section of this data sheet.

$$V_{ON} = \sqrt{BW} \times \sqrt{\left(V_N^2 \times \left(1 + \frac{R_1}{R_2} \right)^2 + I_{N-}^2 \times R_1^2 + I_{N+}^2 \times R_3^2 \times \left(1 + \frac{R_1}{R_2} \right)^2 + 4 \times K \times T \times R_1 + 4 \times K \times T \times R_2 \times \left(\frac{R_1}{R_2} \right)^2 + 4 \times K \times T \times R_3 \times \left(1 + \frac{R_1}{R_2} \right)^2 \right)}$$

FIGURE 3.

Noise Calculations

The primary application for the EL2126 is to amplify very small signals. To maintain the proper signal-to-noise ratio, it is essential to minimize noise contribution from the amplifier. Figure 2 below shows all the noise sources for all the components around the amplifier.

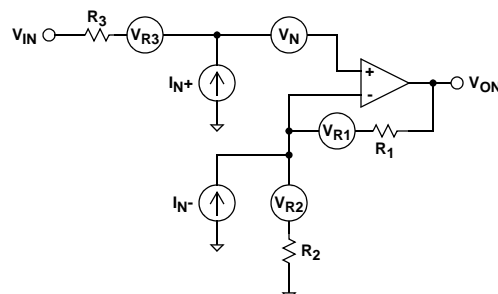


FIGURE 2.

V_N is the amplifier input voltage noise

I_{N+} is the amplifier positive input current noise

I_{N-} is the amplifier negative input current noise

V_{RX} is the thermal noise associated with each resistor:

$$V_{RX} = \sqrt{4kTRx}$$

where:

k is Boltzmann's constant = 1.380658×10^{-23}

T is temperature in degrees Kelvin (273+ °C)

The total noise due to the amplifier seen at the output of the amplifier can be calculated by using the following equation (Figure 3).

As the equation shows, to keep noise at a minimum, small resistor values should be used. At higher amplifier gain configuration where R_2 is reduced, the noise due to I_{N-} , R_2 , and R_1 decreases and the noise caused by I_{N+} , V_N , and R_3 starts to dominate. Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be ignored. This can greatly simplify the formula and make noise calculation much easier to calculate.

Output Drive Capability

The EL2126 is designed to drive low impedance load. It can easily drive 6V_{P-P} signal into a 100Ω load. This high output drive capability makes the EL2126 an ideal choice for RF, IF,

and video applications. Furthermore, the EL2126 is current-limited at the output, allowing it to withstand momentary short to ground. However, the power dissipation with output-shortened cannot exceed the power dissipation capability of the package.

Driving Cables and Capacitive Loads

Although the EL2126 is designed to drive low impedance load, capacitive loads will decrease the amplifier's phase margin. As shown in the performance curves, capacitive load can result in peaking, overshoot and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated with a series resistor between 5Ω to 20Ω . When driving coaxial cables, double termination is always recommended for reflection-free performance. When properly terminated, the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier.

Power Supply Bypassing And Printed Circuit Board Layout

As with any high frequency devices, good printed circuit board layout is essential for optimum performance. Ground plane construction is highly recommended. Lead lengths should be kept as short as possible. The power supply pins must be closely bypassed to reduce the risk of oscillation. The combination of a $4.7\mu\text{F}$ tantalum capacitor in parallel with $0.1\mu\text{F}$ ceramic capacitor has been proven to work well when placed at each supply pin. For single supply operation,

where pin 4 (V_{S-}) is connected to the ground plane, a single $4.7\mu\text{F}$ tantalum capacitor in parallel with a $0.1\mu\text{F}$ ceramic capacitor across pins 7 (V_{S+}) and pin 4 (V_{S-}) will suffice.

For good AC performance, parasitic capacitance should be kept to a minimum. Ground plane construction again should be used. Small chip resistors are recommended to minimize series inductance. Use of sockets should be avoided since they add parasitic inductance and capacitance which will result in additional peaking and overshoot.

Supply Voltage Range and Single Supply Operation

The EL2126 has been designed to operate with supply voltage range of $\pm 2.5\text{V}$ to $\pm 15\text{V}$. With a single supply, the EL2126 will operate from $+5\text{V}$ to $+30\text{V}$. Pins 4 and 7 are the power supply pins. The positive power supply is connected to pin 7. When used in single supply mode, pin 4 is connected to ground. When used in dual supply mode, the negative power supply is connected to pin 4.

As the power supply voltage decreases from $+30\text{V}$ to $+5\text{V}$, it becomes necessary to pay special attention to the input voltage range. The EL2126 has an input voltage range of 0.4V from the negative supply to 1.2V from the positive supply. So, for example, on a single $+5\text{V}$ supply, the EL2126 has an input voltage range which spans from 0.4V to 3.8V . The output range of the EL2126 is also quite large, on a $+5\text{V}$ supply, it swings from 0.4V to 3.8V .

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com