60MHz Rail-to-Rail Input-Output Op Amp

The EL5211A is a low power, high voltage, rail-to-rail input-output amplifier containing two amplifiers. Operating on supplies ranging from 5V to 15V, while consuming only 2.5mA per amplifier, the EL5211A has a bandwidth of 60MHz (-3dB) and provides common-mode input ability beyond the supply rails, as well as rail-to-rail output capability. This enables the EL5211A to offer maximum dynamic range at any supply voltage.

The EL5211A also features fast slewing and settling times, as well as a high output drive capability of 65mA (sink and source). These features make the EL5211A ideal for high speed filtering and signal conditioning application. Other applications include battery-powered, portable devices and anywhere low power consumption is important.

The EL5211A is available in the 8-pin HMSOP package, features a standard operational amplifier pinout, and is specified for operation over a temperature range of -40°C to +85°C.

Ordering Information

PART NUMBER (See Note)	PACKAGE (Pb-Free)	TAPE & REEL	PKG. DWG. #
EL5211AIYEZ	8-Pin HMSOP	-	MDP0050
EL5211AIYEZ-T7	8-Pin HMSOP	7”	MDP0050
EL5211AIYEZ-T13	8-Pin HMSOP	13”	MDP0050

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

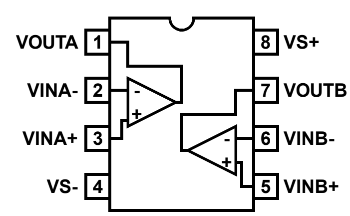
- 60MHz -3dB bandwidth
- Supply voltage = 4.5V to 16.5V
- Low supply current (per amplifier) = 2.5mA
- High slew rate = 75V/µs
- Unity-gain stable
- Beyond the rails input capability
- Rail-to-rail output swing
- ±110mA output short current
- Pb-free plus anneal available (RoHS compliant)

Applications

- TFT-LCD panels
- V_{COM} amplifiers
- Drivers for A-to-D converters
- Data acquisition
- Video processing
- Audio processing
- Active filters
- Test equipment
- Battery-powered applications
- Portable equipment

Pinout

EL5211A
(8-PIN HMSOP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S+ and V_S- . . . .+18V
Input Voltage . . . . V_S- - 0.5V, V_S +0.5V
Maximum Continuous Output Current 65mA
Maximum Die Temperature . . . .+125°C
Storage Temperature . . . .-65°C to +150°C
Ambient Operating Temperature . . . .-40°C to +85°C
Power Dissipation . . . . See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_L = 1kΩ to 0V, T_A = 25°C, unless otherwise specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 1)			7		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	60	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-5.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -5.5V to 5.5V	50	70		dB
A_{VOL}	Open-Loop Gain	-4.5V ≤ V_{OUT} ≤ 4.5V	60	70		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		-4.9	-4.8	V
V_{OH}	Output Swing High	I_L = 5mA	4.8	4.9		V
I_{SC}	Short-Circuit Current			±125		mA
I_{OUT}	Output Current			±65		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from ±2.25V to ±7.75V	60	80		dB
I_S	Supply Current	No load		5	7.5	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 2)	-4.0V ≤ V_{OUT} ≤ 4.0V, 20% to 80%		75		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		80		ns
BW	-3dB Bandwidth			60		MHz
GBWP	Gain-Bandwidth Product			32		MHz
PM	Phase Margin			50		°
CS	Channel Separation	f = 5MHz		110		dB
d_G	Differential Gain (Note 3)	$R_F = R_G$ = 1kΩ and V_{OUT} = 1.4V		0.17		%
d_P	Differential Phase (Note 3)	$R_F = R_G$ = 1kΩ and V_{OUT} = 1.4V		0.24		°

NOTES:

1. Measured over operating temperature range.
2. Slew rate is measured on rising and falling edges.
3. NTSC signal generator used.

Electrical Specifications $V_S+ = +5V$, $V_S- = 0V$, $R_L = 1k\Omega$ to 2.5V, $T_A = 25°C$, unless otherwise specified

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 2.5V$		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 4)			7		µV/°C
I_B	Input Bias Current	$V_{CM} = 2.5V$		2	60	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.5V to 5.5V	45	66		dB
A_{VOL}	Open-Loop Gain	$0.5V \leq V_{OUT} \leq 4.5V$	60	70		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -5mA$		100	200	mV
V_{OH}	Output Swing High	$I_L = 5mA$	4.8	4.9		V
I_{SC}	Short-Circuit Current			±125		mA
I_{OUT}	Output Current			±65		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	60	80		dB
I_S	Supply Current	No load		5	7.5	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 5)	$1V \leq V_{OUT} \leq 4V$, 20% to 80%		75		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		80		ns
BW	-3dB Bandwidth			60		MHz
GBWP	Gain-Bandwidth Product			32		MHz
PM	Phase Margin			50		°
CS	Channel Separation	f = 5MHz		110		dB
d_G	Differential Gain (Note 6)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.17		%
d_P	Differential Phase (Note 6)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.24		°

NOTES:

4. Measured over operating temperature range.
5. Slew rate is measured on rising and falling edges.
6. NTSC signal generator used.

Electrical Specifications $V_S+ = +15V$, $V_S- = 0V$, $R_L = 1k\Omega$ to 7.5V, $T_A = 25°C$, unless otherwise specified

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 7.5V$		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 7)			7		µV/°C
I_B	Input Bias Current	$V_{CM} = 7.5V$		2	60	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+15.5	V

Electrical Specifications
$V_S+ = +15V$, $V_S- = 0V$, $R_L = 1k\Omega$ to 7.5V, $T_A = 25°C$, unless otherwise specified **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.5V to 15.5V	53	72		dB
A_{VOL}	Open-Loop Gain	$0.5V \le V_{OUT} \le 14.5V$	60	70		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		100	200	mV
V_{OH}	Output Swing High	I_L = 5mA	14.8	14.9		V
I_{SC}	Short-Circuit Current			±125		mA
I_{OUT}	Output Current			±65		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	60	80		dB
I_S	Supply Current	No load		5	7.5	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 8)	$1V \le V_{OUT} \le 14V$, 20% to 80%		75		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		80		ns
BW	-3dB Bandwidth			60		MHz
GBWP	Gain-Bandwidth Product			32		MHz
PM	Phase Margin			50		°
CS	Channel Separation	f = 5MHz		110		dB
d_G	Differential Gain (Note 9)	$R_F = R_G = 1k\Omega$ and V_{OUT} = 1.4V		0.16		%
d_P	Differential Phase (Note 9)	$R_F = R_G = 1k\Omega$ and V_{OUT} = 1.4V		0.22		°

NOTES:

7. Measured over operating temperature range
8. Slew rate is measured on rising and falling edges
9. NTSC signal generator used

Typical Performance Curves

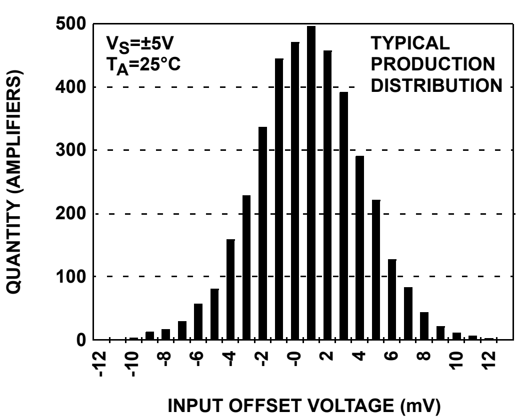


FIGURE 1. INPUT OFFSET VOLTAGE DISTRIBUTION

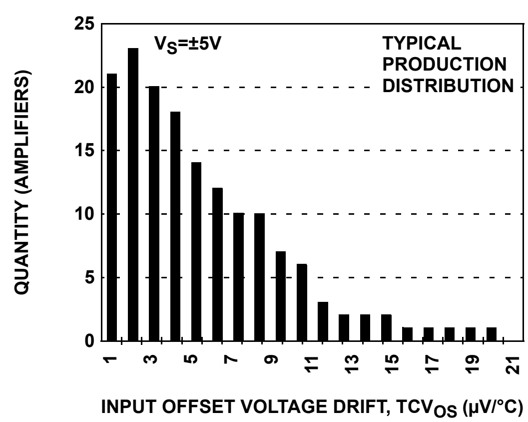


FIGURE 2. INPUT OFFSET VOLTAGE DRIFT

Typical Performance Curves (Continued)

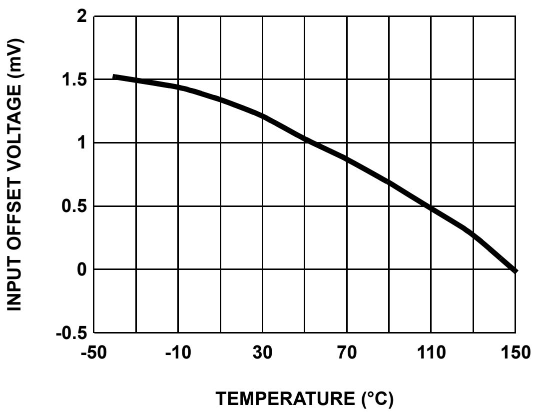


FIGURE 3. INPUT OFFSET VOLTAGE vs TEMPERATURE

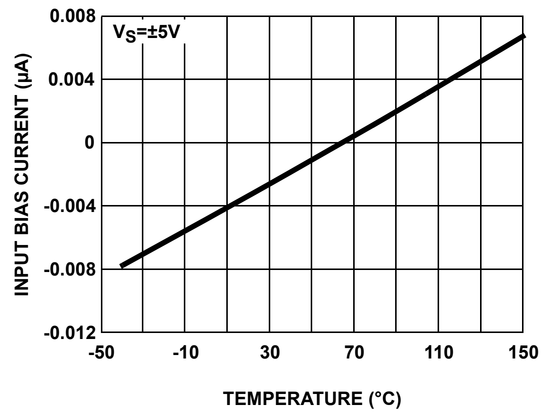


FIGURE 4. INPUT BIAS CURRENT vs TEMPERATURE

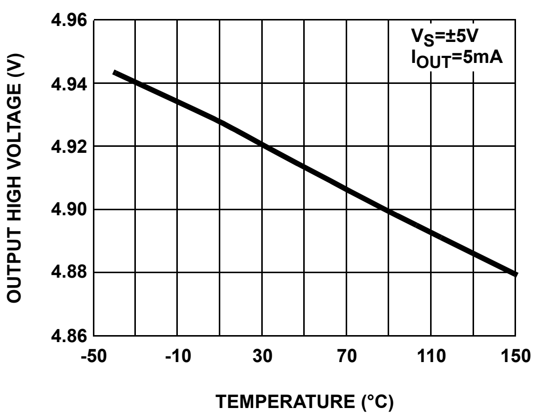


FIGURE 5. OUTPUT HIGH VOLTAGE vs TEMPERATURE

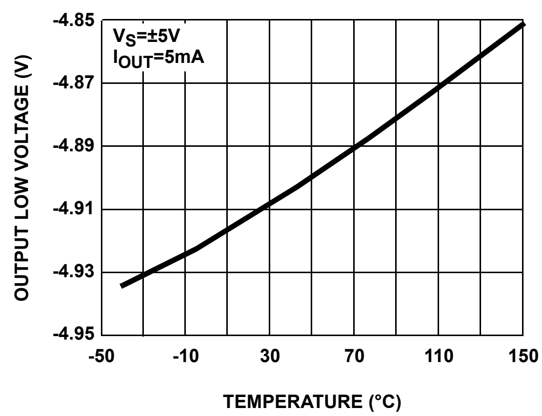


FIGURE 6. OUTPUT LOW VOLTAGE vs TEMPERATURE

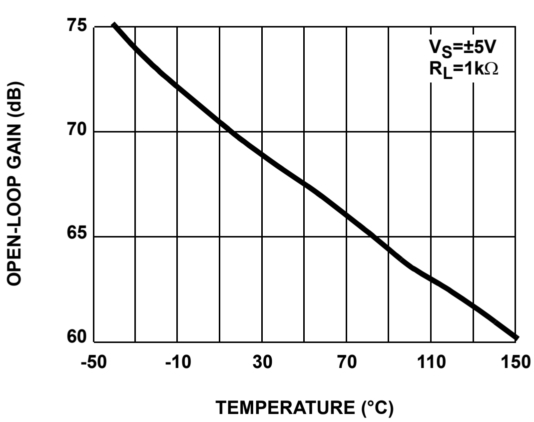


FIGURE 7. OPEN-LOOP GAIN vs TEMPERATURE

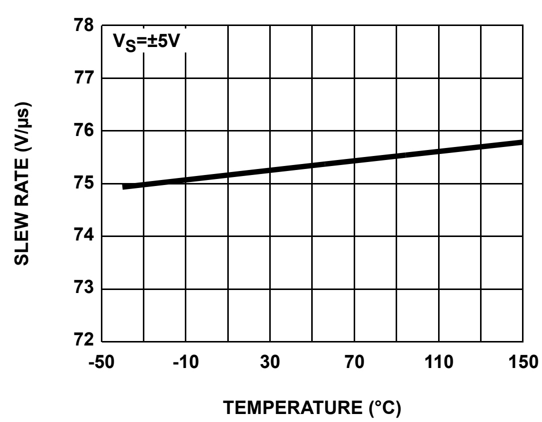


FIGURE 8. SLEW RATE vs TEMPERATURE

Typical Performance Curves (Continued)

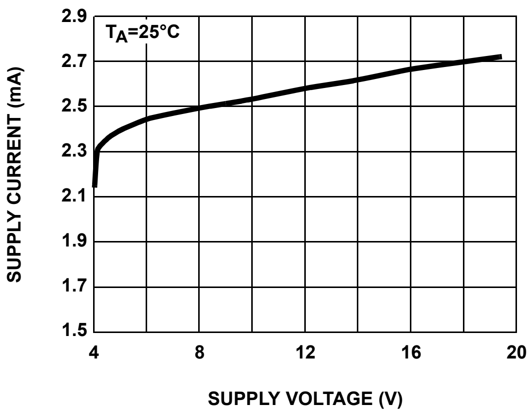


FIGURE 9. SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

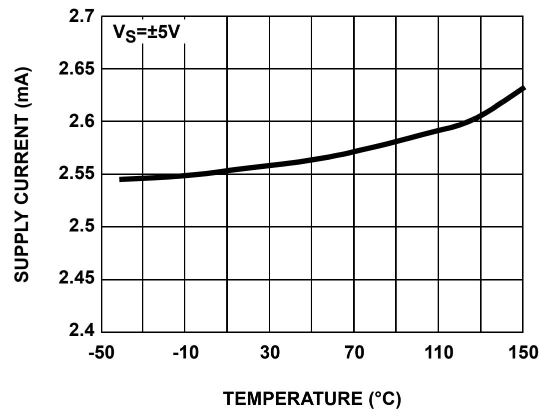


FIGURE 10. SUPPLY CURRENT PER AMPLIFIER vs TEMPERATURE

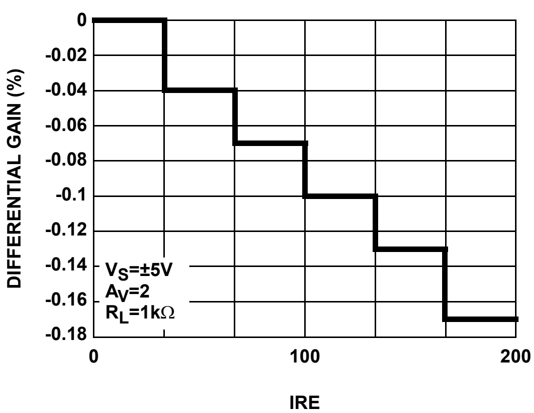


FIGURE 11. DIFFERENTIAL GAIN

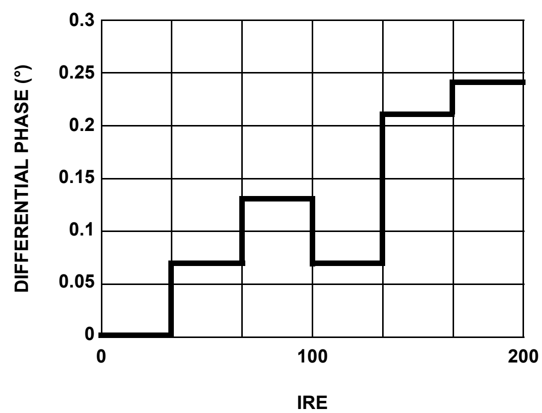


FIGURE 12. DIFFERENTIAL PHASE

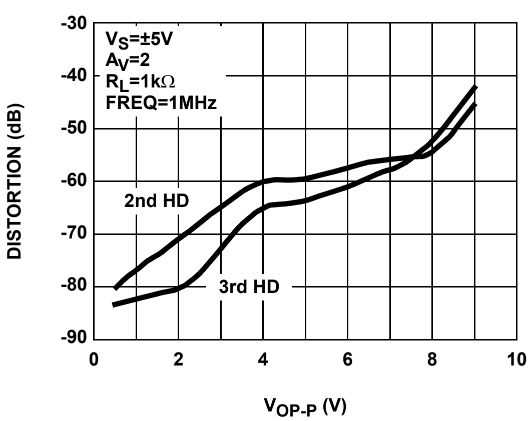


FIGURE 13. HARMONIC DISTORTION vs V_{OP-P}

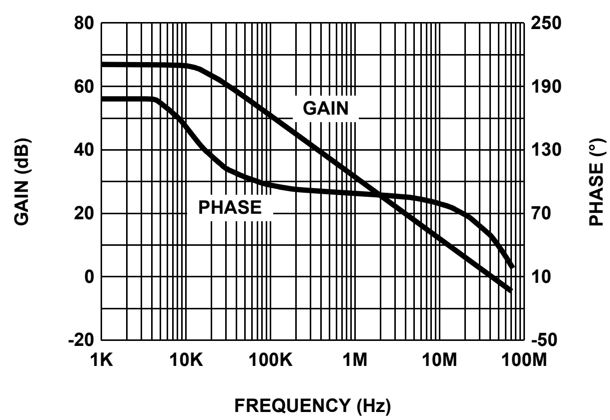


FIGURE 14. OPEN LOOP GAIN AND PHASE

Typical Performance Curves (Continued)

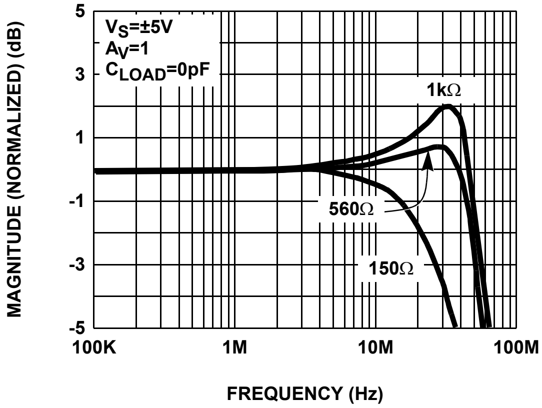


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS R_L

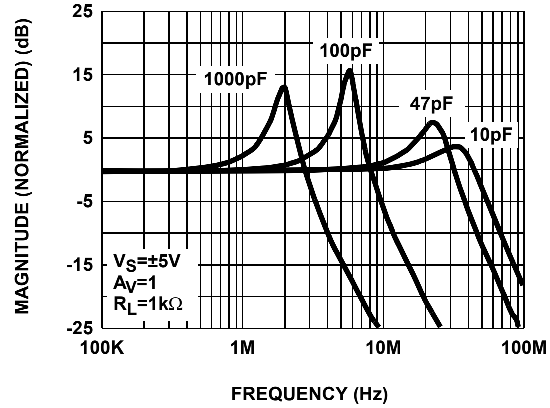


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS C_L

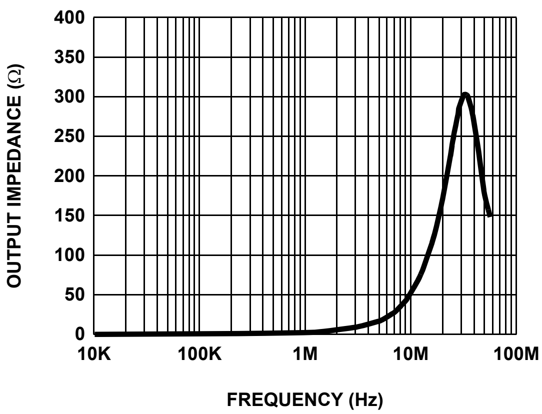


FIGURE 17. CLOSED LOOP OUTPUT IMPEDANCE

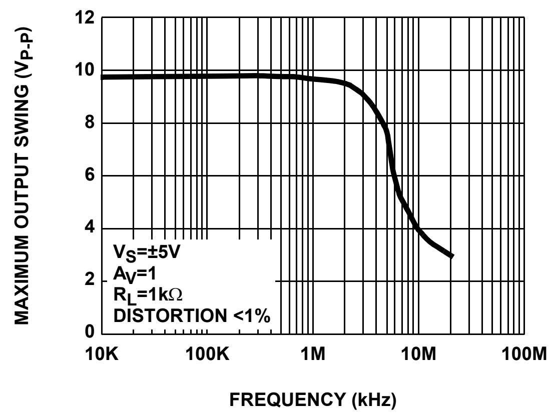


FIGURE 18. MAXIMUM OUTPUT SWING vs FREQUENCY

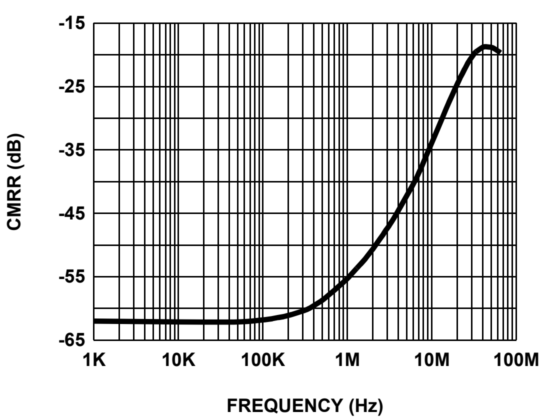


FIGURE 19. CMRR

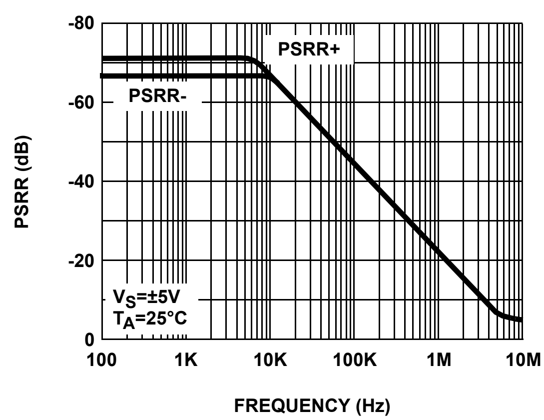


FIGURE 20. PSRR

Typical Performance Curves (Continued)

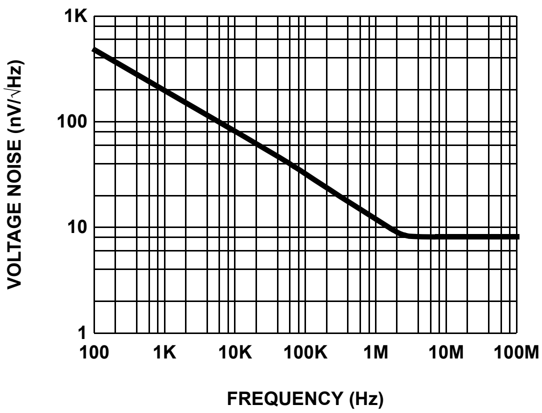


FIGURE 21. INPUT VOLTAGE NOISE SPECTRAL DENSITY

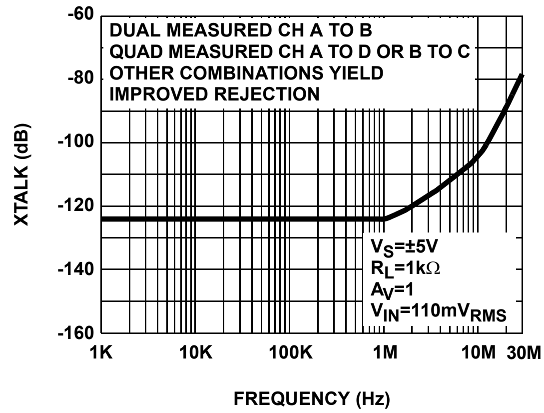


FIGURE 22. CHANNEL SEPARATION

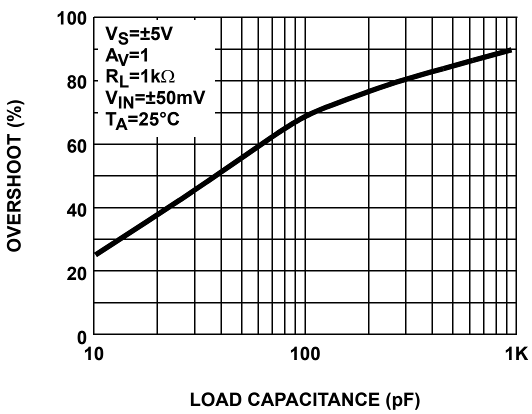


FIGURE 23. SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

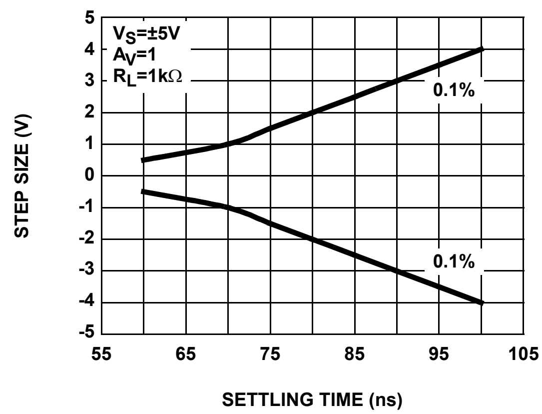


FIGURE 24. SETTLING TIME vs STEP SIZE

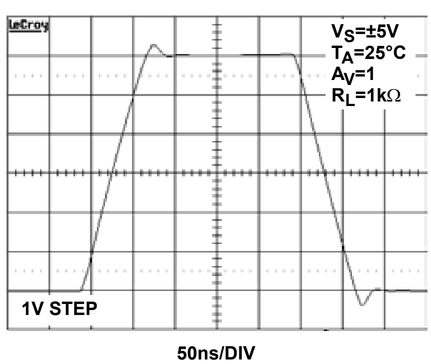


FIGURE 25. LARGE SIGNAL TRANSIENT RESPONSE

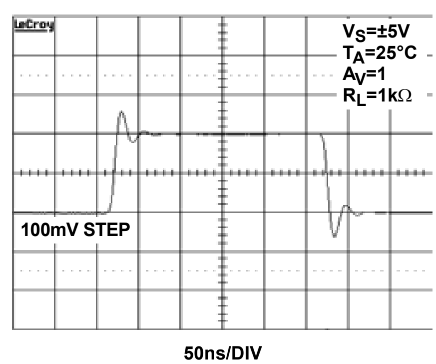
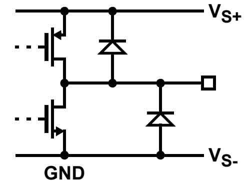
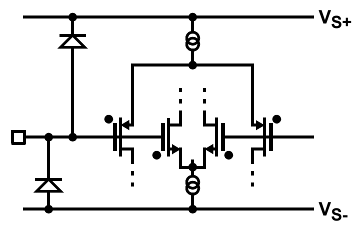


FIGURE 26. SMALL SIGNAL TRANSIENT RESPONSE

Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1	VOUTA	Amplifier A output	 CIRCUIT 1
2	VINA-	Amplifier A inverting input	 CIRCUIT 2
3	VINA+	Amplifier A non-inverting input	(Reference Circuit 2)
4	VS-	Negative power supply	
5	VINB+	Amplifier B non-inverting input	(Reference Circuit 2)
6	VINB-	Amplifier B inverting input	(Reference Circuit 2)
7	VOUTB	Amplifier B output	(Reference Circuit 1)
8	VS+	Positive power supply	

Applications Information

Product Description

The EL5211A voltage feedback amplifier is fabricated using a high voltage CMOS process. It exhibits rail-to-rail input and output capability, is unity gain stable, and has low power consumption (2.5mA per amplifier). These features make the EL5211A ideal for a wide range of general-purpose applications. Connected in voltage follower mode and driving a load of 1kΩ, the EL5211A has a -3dB bandwidth of 60MHz while maintaining a 75V/µs slew rate. The EL5211A is a dual amplifier.

Operating Voltage, Input, and Output

The EL5211A is specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range of 4.5V to 16.5V. Most EL5211A specifications are stable over both the full supply range and operating temperatures of -40°C to +85°C. Parameter variations with operating voltage and/or temperature are shown in the typical performance curves.

The input common-mode voltage range of the EL5211A extends 500mV beyond the supply rails. The output swings of the EL5211A typically extend to within 100mV of positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 27 shows the input and output waveforms for the device in the unity-gain configuration. Operation is from ±5V supply with a 1kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid. The output voltage is approximately $9.8V_{P-P}$.

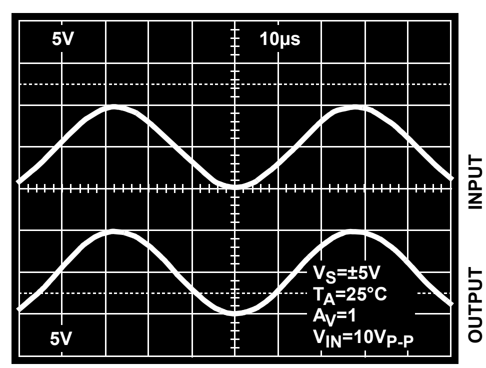


FIGURE 27. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

Short Circuit Current Limit

The EL5211A will limit the short circuit current to ±110mA if the output is directly shorted to the positive or the negative supply. If an output is shorted indefinitely, the power dissipation could easily increase such that the device may be damaged. Maximum reliability is maintained if the output continuous current never exceeds ±65mA. This limit is set by the design of the internal metal interconnects.

Output Phase Reversal

The EL5211A is immune to phase reversal as long as the input voltage is limited from V_S- -0.5V to V_S+ +0.5V. Figure 28 shows a photo of the output of the device with the input voltage driven beyond the supply rails. Although the device's output will not change phase, the input's overvoltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diodes placed in the input stage of the device begin to conduct and overvoltage damage could occur.

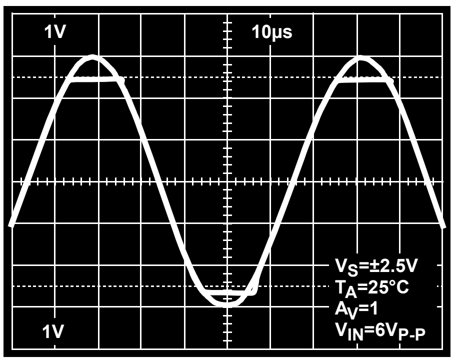


FIGURE 28. OPERATION WITH BEYOND-THE-RAILS INPUT

Power Dissipation

With the high-output drive capability of the EL5211A amplifier, it is possible to exceed the 125°C 'absolute-maximum junction temperature' under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- Θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_S + - V_{OUT}i) \times I_{LOAD}i]$$

when sourcing, and:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_{OUT}i - V_S -) \times I_{LOAD}i]$$

when sinking,

where:

- i = 1 to 2 for dual and 1 to 4 for quad
- V_S = Total supply voltage
- I_{SMAX} = Maximum supply current per amplifier
- $V_{OUT}i$ = Maximum output voltage of the application
- $I_{LOAD}i$ = Load current

If we set the two P_{DMAX} equations equal to each other, we can solve for $R_{LOAD}i$ to avoid device overheat. Figures 29 and 30 provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P_{DMAX} exceeds the device's power derating curves. To ensure proper operation, it is important to observe the recommended derating curves shown in Figures 29 and 30.

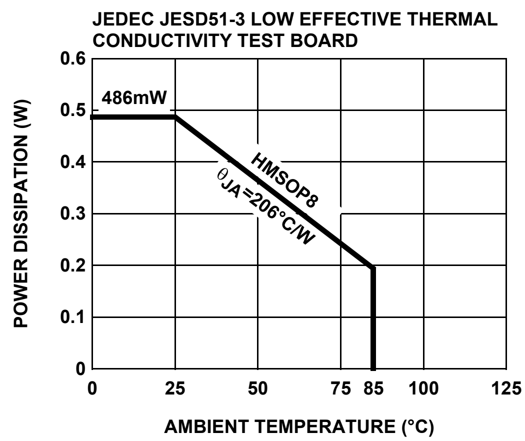


FIGURE 29. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

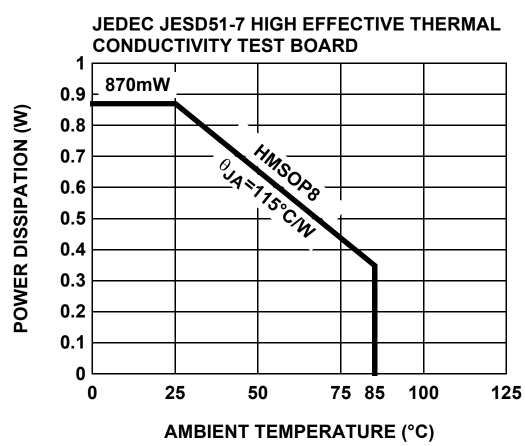


FIGURE 30. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

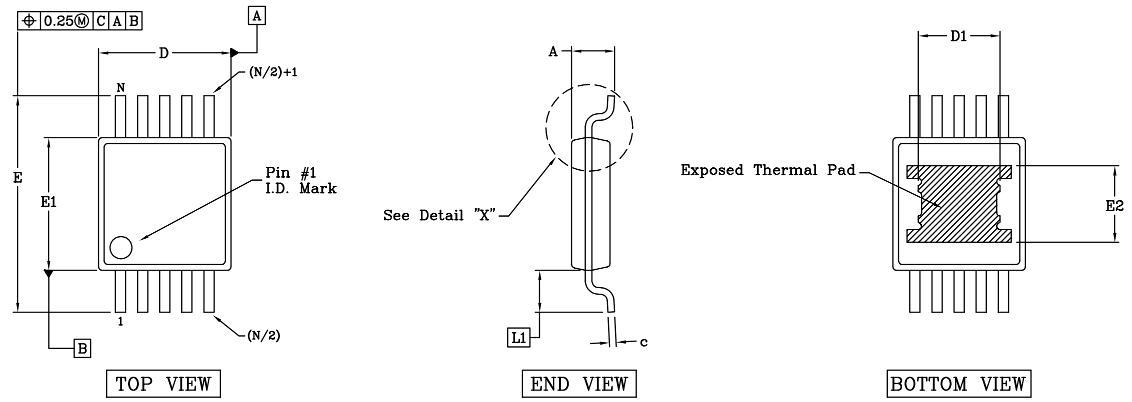
Unused Amplifiers

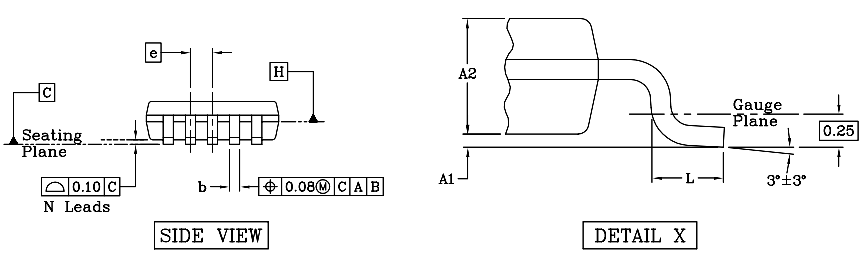
It is recommended that any unused amplifiers in a dual and a quad package be configured as a unity gain follower. The inverting input should be directly connected to the output and the non-inverting input tied to the ground plane.

Power Supply Bypassing and Printed Circuit Board Layout

The EL5211A can provide gain at high frequency. As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to ground, a 0.1µF ceramic capacitor should be placed from V_S+ to pin to V_S- pin. A 4.7µF tantalum capacitor should then be connected in parallel, placed in the region of the amplifier. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

Package Outline Drawing





DIMENSION TABLE			
Symbol	HMSOP8	HMSOP10	Tolerance
A	1.00	1.00	MAX.
A1	0.075	0.075	+0.025/−0.050
A2	0.86	0.86	+/− 0.09
D (1)(3)	3.00	3.00	+/− 0.10
E	4.90	4.90	+/− 0.15
E1 (2)(3)	3.00	3.00	+/− 0.10
L	0.55	0.55	+/− 0.15
L1	0.95	0.95	Basic
b	0.30	0.20	+0.07/−0.08
c	0.15	0.15	+/− 0.05
e	0.65	0.50	Basic
D1	1.85	1.85	Reference
E2	1.73	1.73	Reference
N	8	10	Reference

Drawing #: MDP0050	PACKAGE OUTLINE DRAWING HMSOP (Heat−Sink MSOP) PACKAGE FAMILY
Rev: 0	
Date: 10/17/03	
Units: mm	intersil SOLUTIONS IN SILICON
JEDEC Reg: MO−187	

Notes:
(1) Plastic or metal protrusions of 0.15 mm maximum per side are not included.
(2) Plastic interlead protrusions of 0.25 mm maximum per side are not included.
(3) Dimensions "D" and "E1" are measured at Datum Plane "H".
(4) Dimensioning and tolerancing per ASME Y14.5M−1994.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at http://www.intersil.com/design/packages/index.asp

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