

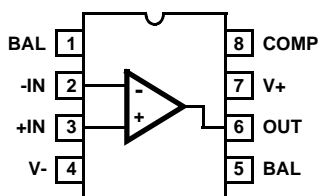
12MHz, High Input Impedance, Operational Amplifier

HA-2515 is a high performance operational amplifier which sets the standards for maximum slew rate, highest accuracy and widest bandwidths for internally compensated devices. In addition to excellent dynamic characteristics, this dielectrically isolated amplifier also offers low offset current and high input impedance.

The $\pm 60\text{V}/\mu\text{s}$ slew rate and 250ns (0.1%) settling time of this amplifier is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2515's superior 12MHz gain bandwidth and 1000kHz power bandwidth is extremely useful in RF and video applications. For accurate signal conditioning this amplifier also provides 10nA offset current, coupled with 100M Ω input impedance, and offset trim capability.

Pinout

HA-2515 (PDIP)
TOP VIEW



Features

- Slew Rate 60V/ μs
- Fast Settling 250ns
- Full Power Bandwidth 1MHz
- Gain Bandwidth 12MHz
- High Input Impedance 100M Ω
- Low Offset Current 10nA
- Internally Compensated for Unity Gain Stability

Applications

- Data Acquisition Systems
- RF Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Part Number Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA3-2515-5	0 to 75	8 Ld PDIP	E8.3

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
 Differential Input Voltage 15V
 Peak Output Current 50mA

Operating Conditions

Temperature Range
 HA-2515-5 0°C to 75°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W) θ_{JC} (°C/W)
 PDIP Package 120 N/A
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C

Electrical Specifications $V_{SUPPLY} = \pm 15V$

PARAMETER	TEMP (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	25	-	5	10	mV
	Full	-	-	14	mV
Offset Voltage Average Drift	Full	-	30	-	$\mu V/^{\circ}C$
Bias Current	25	-	125	250	nA
	Full	-	-	500	nA
Offset Current	25	-	20	50	nA
	Full	-	-	100	nA
Input Resistance (Note 2)	25	40	100	-	M Ω
Common Mode Range	Full	± 10.0	-	-	V
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Notes 3, 6)	25	7.5	15	-	kV/V
	Full	5	-	-	kV/V
Common Mode Rejection Ratio (Note 4)	Full	74	90	-	dB
Gain Bandwidth Product (Note 5)	25	-	12	-	MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 3)	Full	± 10.0	± 12.0	-	V
Output Current (Note 6)	25	± 10	± 20	-	mA
Full Power Bandwidth (Notes 6, 11)	25	600	1000	-	kHz
TRANSIENT RESPONSE					
Rise Time (Notes 3, 7, 8, 9)	25	-	25	50	ns
Overshoot (Notes 3, 7, 8, 9)	25	-	25	50	%
Slew Rate (Notes 3, 7, 9, 12)	25	± 40	± 60	-	V/ μs
Settling Time to 0.1% (Notes 3, 7, 9, 12)	25	-	0.25	-	μs
POWER SUPPLY CHARACTERISTICS					
Supply Current	25	-	4	6	mA
Power Supply Rejection Ratio (Note 10)	Full	74	90	-	dB

NOTES:

2. This parameter value is based on design calculations.
3. $R_L = 2k\Omega$.
4. $V_{CM} = \pm 10V$.
5. $A_V > 10$.
6. $V_O = \pm 10V$.
7. $C_L = 50pF$.
8. $V_O = \pm 200mV$.
9. See Transient Response Test Circuits and Waveforms.
10. $\Delta V = \pm 5V$.
11. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \text{Slew Rate} / 2\pi V_{PEAK}$.
12. $V_{OUT} = \pm 5V$.

Test Circuits and Waveforms

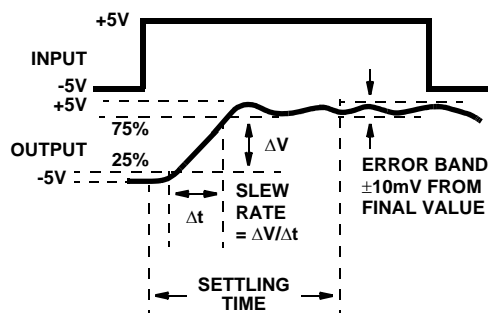
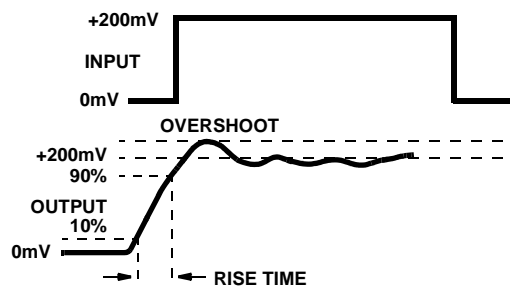


FIGURE 1. SLEW RATE AND SETTLING TIME



NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

FIGURE 2. TRANSIENT RESPONSE

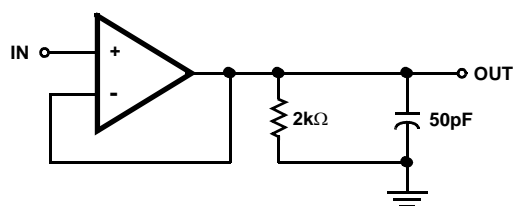
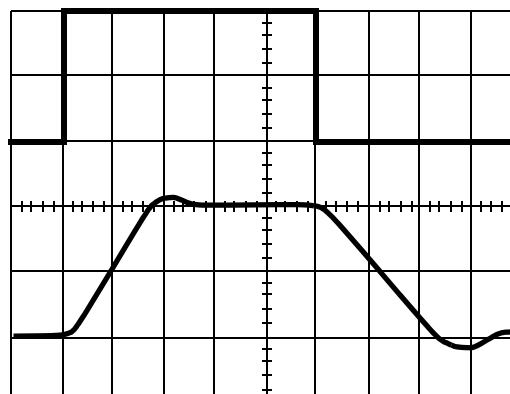
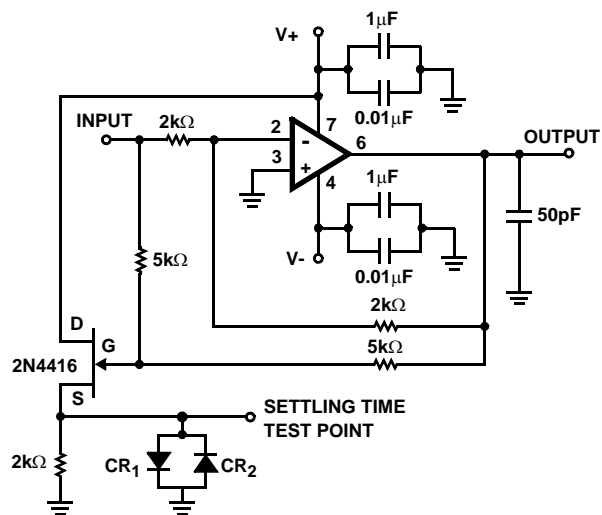


FIGURE 3. SLEW RATE AND TRANSIENT RESPONSE



$R_L = 2k\Omega$, $C_L = 50pF$
 Upper Trace: Input
 Lower Trace: Output
 Vertical = 5V/Div.
 Horizontal = 200ns/Div.
 $T_A = 25^\circ C$, $V_S = \pm 15V$

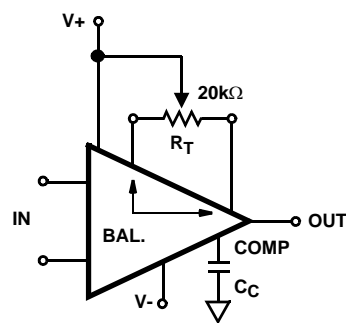
FIGURE 4. VOLTAGE FOLLOWER PULSE RESPONSE



NOTES:

13. $A_V = -1$.
14. Feedback and summing resistor ratios should be 0.1% matched.
15. Clipping diodes CR_1 and CR_2 are optional. HP5082-2810 recommended.

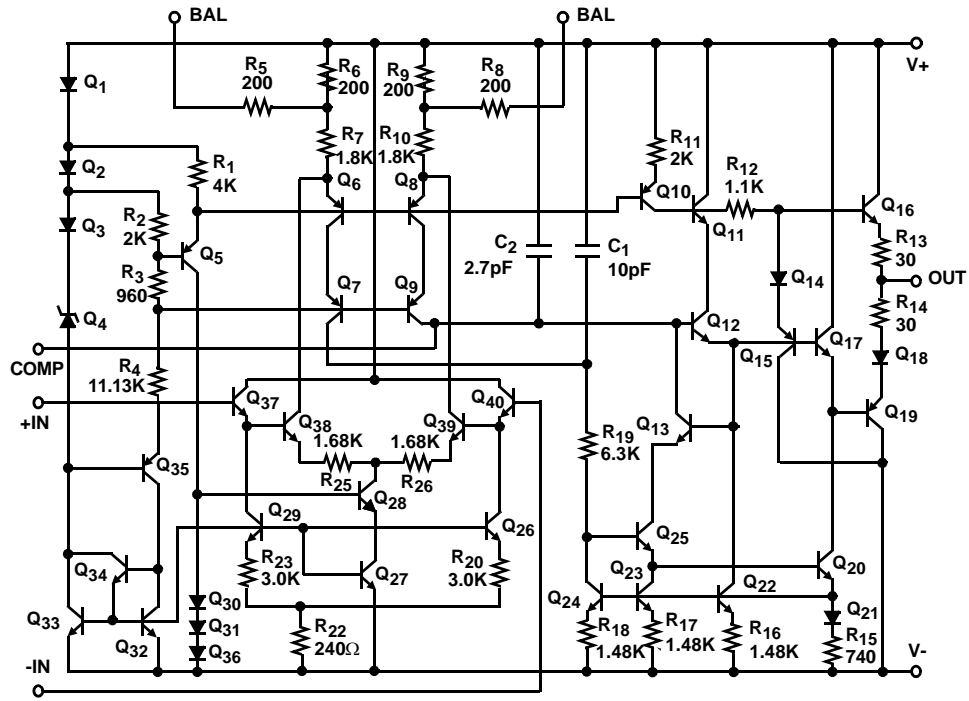
FIGURE 5. SETTLE TIME TEST CIRCUIT



NOTE: Tested offset adjustment range is $IVOS + 1mV$ minimum referred to output. Typical ranges are $\pm 6mV$ with $R_T = 20k\Omega$.

FIGURE 6. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK UP

Schematic



Typical Performance Curves

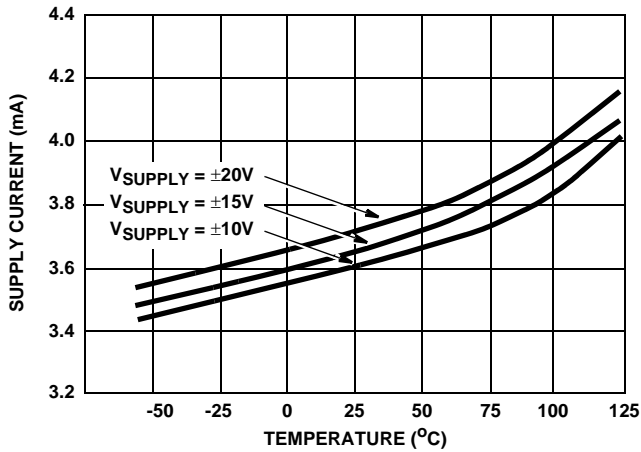


FIGURE 7. POWER SUPPLY CURRENT vs TEMPERATURE

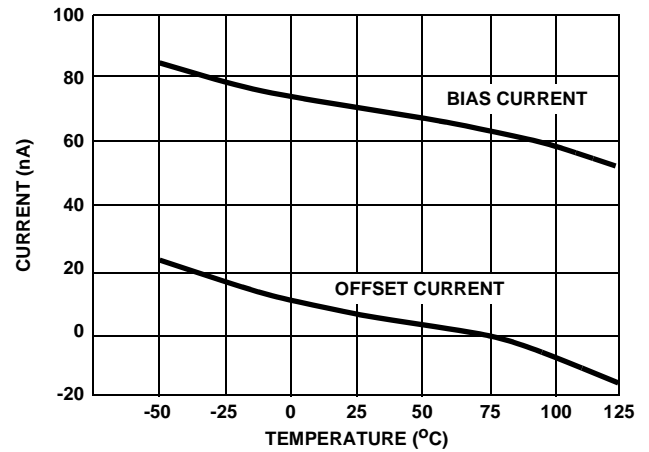


FIGURE 8. INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

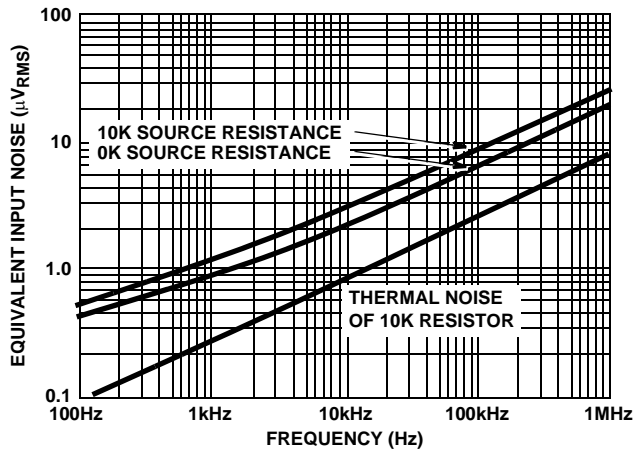


FIGURE 9. EQUIVALENT INPUT NOISE vs BANDWIDTH (WITH 10Hz HIGH PASS FILTER)

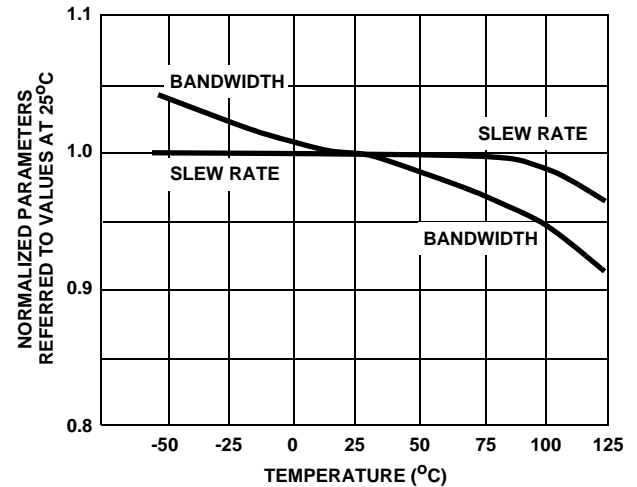


FIGURE 10. NORMALIZED AC PARAMETERS vs TEMPERATURE

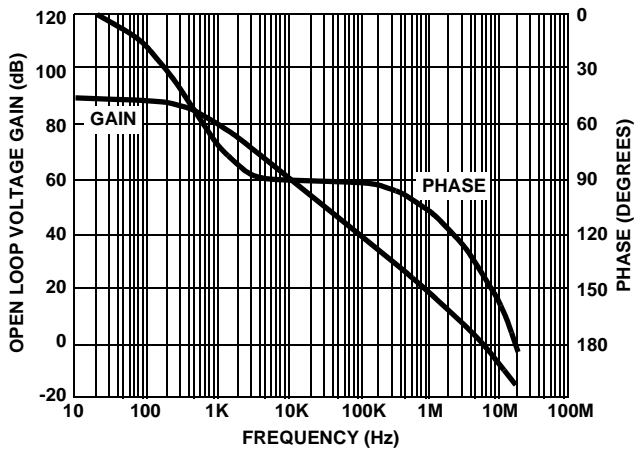


FIGURE 11. OPEN LOOP GAIN AND PHASE RESPONSE

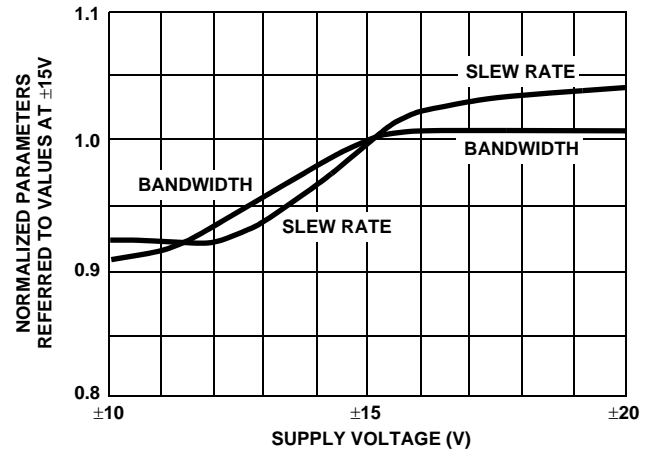


FIGURE 12. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT 25°C

Typical Performance Curves (Continued)

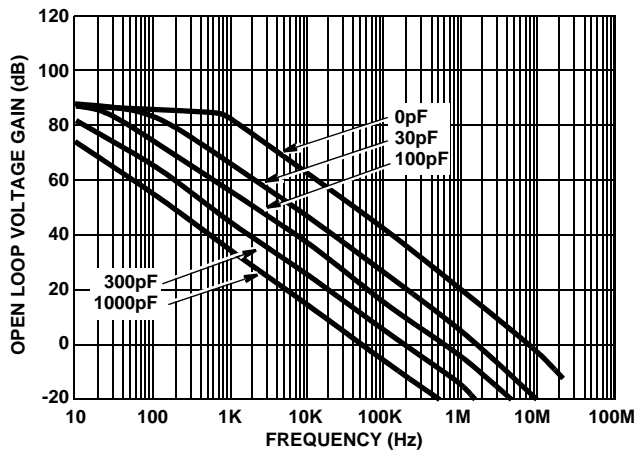


FIGURE 13. OPEN LOOP GAIN RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

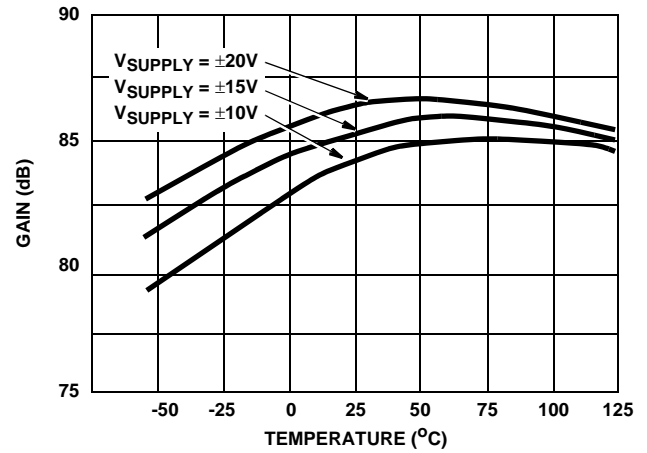


FIGURE 14. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

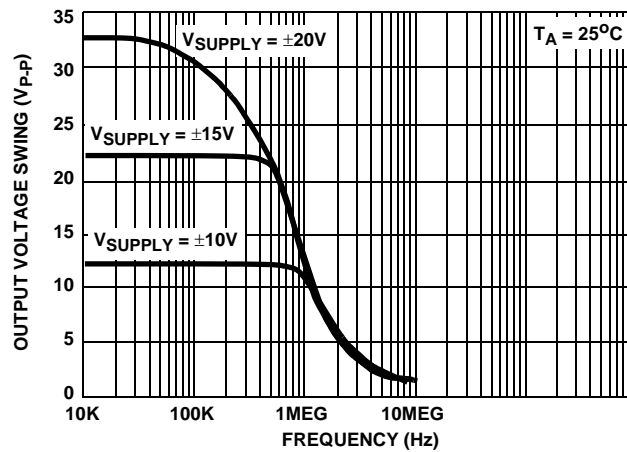


FIGURE 15. OUTPUT VOLTAGE SWING vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

65 mils x 57 mils x 19 mils
1650 μ m x 1450 μ m x 483 μ m

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16k \AA \pm 2k \AA

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2 , 5% Phos.)
Silox Thickness: 12k \AA \pm 2k \AA
Nitride Thickness: 3.5k \AA \pm 1.5k \AA

SUBSTRATE POTENTIAL (Powered Up):

Unbiased

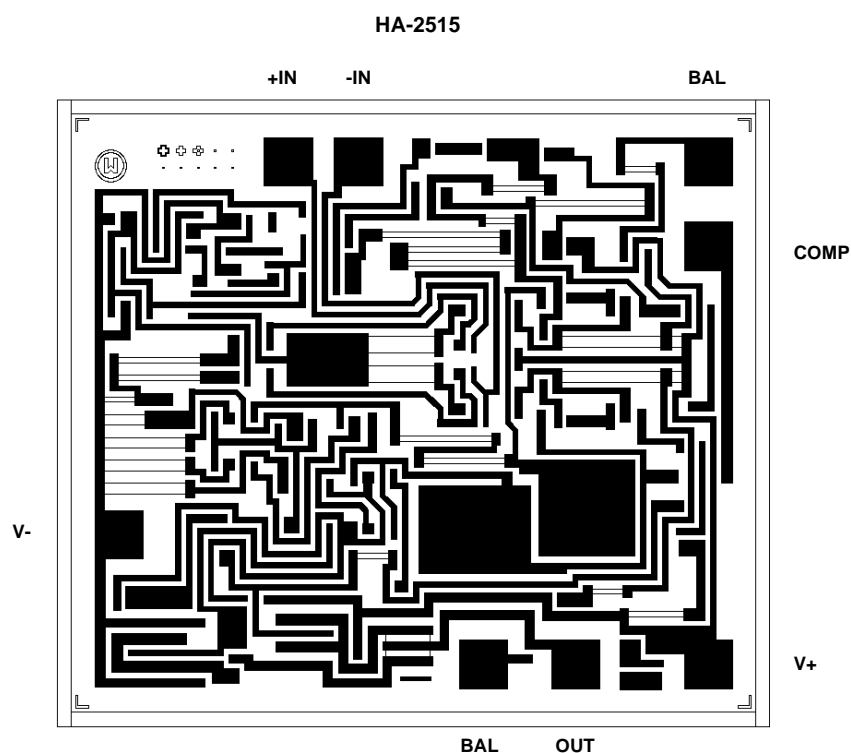
TRANSISTOR COUNT:

40

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

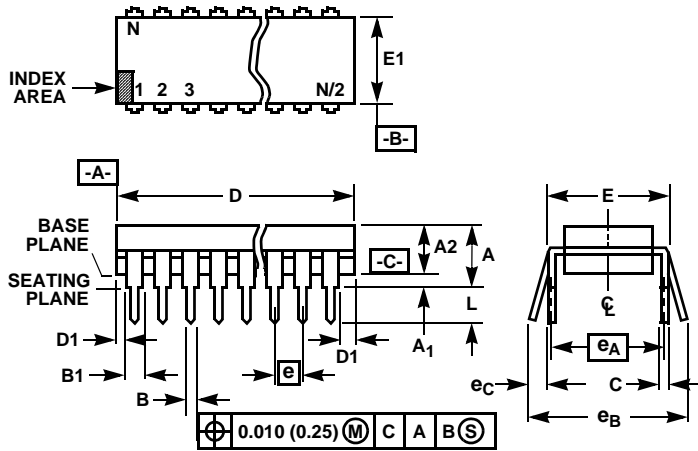


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Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and eA are measured with the leads constrained to be perpendicular to datum -C-.
7. eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D) 8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		6
eB	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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